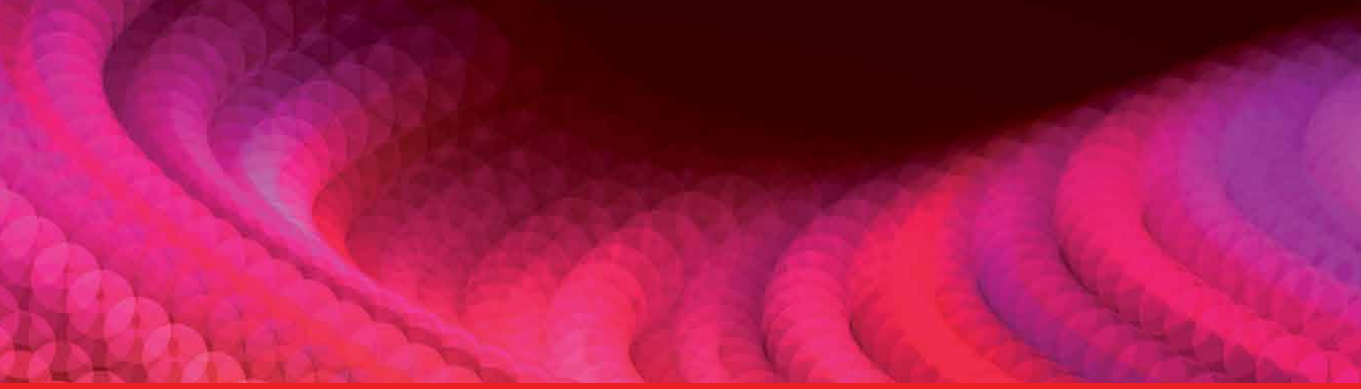

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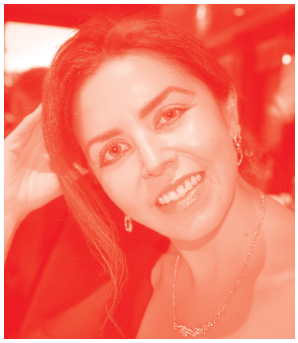

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Meet the editor

Dr. Alex P. James works in the areas of artificial intelligence (AI), neuromorphic systems (software and hardware), Very Large Scale Integration (VLSI), and image processing. He completed his PhD in two years at Griffith University, Queensland, Australia. He is currently a full professor and the professor in charge of the Maker Village project at the Indian Institute of Information Technology & Management – Kerala (IIITM-K), one of the largest electronics incubator facilities in India. He is a member of the technical committee on nonlinear circuits and systems of the Institute of Electrical and Electronics Engineers Circuits and Systems Society (IEEE CASS). He was the founding chair of the IEEE CASS Kerala chapter and a member of the IET Vision and Imaging Network. He was an editorial board member of the journal *Information Fusion* and currently serves as associate editor of *IEEE Access*, *Human-centric Computing and Information Sciences*, and *IEEE Transactions on Circuits and Systems I*. He is a senior member of IEEE, a lifetime member of Association for Computing Machinery (ACM), and a senior fellow of Higher Education Academy(HEA).

Contents

Preface

This edited volume is a collection of reviewed and relevant research chapters concerning developments within the field of memristor devices. The book includes scholarly contributions by various authors and edited by a group of experts pertinent to Engineering. Each contribution comes as a separate chapter complete in itself but directly related to the book's topics and objectives.

The book is divided into two sections: "Memristor Introduction and System Models" and "Applications." The first section includes chapters on the challenges in neuro-memristive circuit design, memristor synapses for neuromorphic computing, and coexistence of bipolar and unipolar memristor switching behavior. The second section includes chapters on memristive grids for maze solving, mathematical analysis of memristor cellular neural networks, memristor behavior under dark and violet illumination in thin films, and application of probe nanotechnologies for memristor structure formation and characterization. The target audience comprises scholars and specialists in the field.

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Section 1

Memristor Introduction and System Models

Chapter 1

Introductory Chapter: Challenges in Neuro-Memristive Circuit Design

Alex James

1. Introduction: what makes memristors attractive for neural networks?

The ability of the memristors to change its conductance i.e. behaves like a resistor, and yet be able to remain in that conductive state, be able to change the state based on a control voltage makes it resemble like a neuron. The spiking neurons in the brain respond to the stimuli in different ways. The continuous application of stimuli and the changing response of the neuron to this is related to learning. In the same way, by application of voltage pulses of certain amplitude and frequency can cause a change in conductance state, reflecting as changing the amplitude of the current outputs through a memristor [1–3]. The voltage pulse trains below a threshold voltage for a given conductance state produces a current signal output that follows the input voltages reflecting learning ability. As such this idea can be translated to emulate spiking neurons with memristors [4, 5].

Another major design use case for memristor is the crossbar arrangement of the memristors. The memristors are arranged in a crossbar architecture, with each memristor being able to be accessed with rows and columns. The memristors are programmed using the transistor switch control, or selector switch control often referred to as ITIM or 1S1M configuration [6, 7]. Multiple transistors are usually required in the practical control circuits and depending on the complexity of the task such as the need to access multiple conductance states, the design aspects become complicated [8]. Nonetheless, a single crossbar can emulate a single dot product matrix computation that is required for weighted summation of inputs in a neural network layer. From a design perspective, at a higher level the simplification of multiply and accumulate operation is simplified, and it can reduce the design complexity.

The neuro-memristive system requires architectural level combinations of crossbars and memristor neurons, and be able to fabricate along with CMOS devices. Usually, sensors, control circuits and memories, would be required for the neural network to be scaled to a large network. The larger the network or deeper the number of layers in the neural network, the complexity of implementing increases. Large crossbar arrays suffer from the sneak path currents and non-idealities of the devices, which introduces errors in the dot-product computations, that propagate from one layer to another. While to some extent these errors can be compensated with learning algorithms, they do not fully compensate for the changes in real-time conditions. Online learning is possibly a way to compensate for real-time errors, however, online learning systems are not easy to realise for analog circuits and often consume a large amount of area on-chip and power. For digital implementations, in general, online learning circuits consume larger area and higher delays, than the crossbar based analog counterparts.

2. Main challenges

2.1 Modelling issues

Modelling realistic memristors devices is a challenging task [3]. There have been arguments for and against the existence of "ideal" memristor devices, based on electrical, physical, chemical and philosophical arguments [9, 10]. From a neural circuit design perspective, the arguments on the existence of such idealistic devices are practically not relevant. The more important question for the circuit designer is the accurate modelling of the practical device that can be either used as a spiking neuron or can be used in a crossbar.

When the models can incorporate into a simulator, it is important that the models represent accurately the true behaviour of the device and also are fast in terms of computation [3]. The ability for the models to be easily integrated into SPICE like simulators, that can enable simulations of millions of neurons are important for building neural networks [11]. Currently, the simulations with memristor models are extremely slow for deep neural networks, and often require the use of scripting languages such as Python to get around this issue.

2.2 Lack of design tools

There is limited availability of physical design kits (PDK) for use in standard design tools such as provided by Cadence [12], Mentor Graphics [13], Silvaco [14] etc. The support for memristor PDK suitable for integration with CMOS is largely an open problem. The accuracy of the design files is not comparable with CMOS processes, and the variability data is not very well disclosed. The design tools that can accurately translate the realistic memristor devices are not very common and is an active topic of study.

2.3 Reliability issues of memristors

The memristor devices suffer from a range of reliability issues. Some of the main issues include:

Ageing – the devices when switched ON and OFF for a long period of time suffer from the loss of conductance state. This creates a major problem in analog dot product computations with crossbar architecture. Ageing has better tolerance to binary neural networks [15, 16].

Noise – the electrical and thermal noise can play with the changes in output response of the memristors, which can interact with the design of the neurons. The exact interplay of the device noise within different configurations of the network is largely an open question [17].

Variability – the variability of the conductance due to process and fabrication challenges can create design challenges for the crossbars. The neural network design has shown to be tolerant to large variations in conductance [18–20]. The signal integrity and electromagnetics issues related to packaging also need to be taken into account in this challenge.

2.4 Complexity issues for programming memristors

Programming the memristors requires applying a series of voltage pulses for a sustained period of time until the conductance of the memristor changes to the desired value. The state changes are based on the magnitude of the voltages applied. The issue with the realistic design is the voltage control across several memristors is

not an easy task. The memristors in crossbar are prone to non-idealities and often faced with variable threshold voltages. This makes the design of the programing logic complex [21, 22]. The ability to program memristor devices in parallel with low cost on the power, and area on-chip, is a challenging program, especially if the design is for analog neural networks [23].

2.5 Architectural challenges

There are several types of neural networks. Many designs have multiple layers and they involve convolution layers that involve dendrite logic [24]. This makes the architecture design complex for generalisation. While crossbar-based designs can be used for a large number of neural network architectures, optimising the design for hardware is a totally different problem [6, 25]. The architectural changes need to be aligned with the circuit design challenges, especially, when the design constraints are with chasing accuracy and system-level performance metrics. The architectural designs also need to take care of a wide range of generalisation issues including those related to hardware-software co-design, and system of chip solutions [25].

2.6 Scaling and 3D integration

Scaling the CMOS circuits, and improving the packing density of the memristors are not a well-studied problem. There have been several suggestions on using 3D technologies and using vertical devices for very-large-scale integration [26, 27]. The main challenge in this regard has been the variability of the devices that prevent the large-scale 3D integration of crossbar-based designs. There are yet not full-proof solutions to scaling up in density and scaling up in size. The best architecture level scale-up is the use of modular designs that make use of several small crossbars to create larger ones [28, 29]. However, these designs are yet to be fully tested in a realistic commercial application.

2.7 Neuron model

There are several types of neurons in the human brain [30–40]. The cognition is a result of interactions between varied types of neurons in the cortex. Most neural networks inspire from the cortical neural networks and often are oversimplifications of the biological networks. The exact form of how intelligence over a life-time of human are not very well understood to completely build an equivalent machine intelligence. At best what we have achieved today in neuro-chips is weak intelligence, being able to implement some specific functionality of the human brain, that too not in its entirety. The journey of hardware AI research is its very early stages, with a scalable design similar to the human brain practically limited by the chemistry of how neurons work. The organic nature of the brain offers several advantages over the silicon neuron. The electrical models are many, but they all tend to be bulky and complex when implemented in silicon. Having a functionally complex neuron with simplistic implementation complexity is a major challenge in the system design of memristive neural networks.

3. Discussions and future outlook

While these challenges exist, the practical use of neural networks build with crossbar and that using memristive spiking neurons are many. Several problems having a few sets of sensors such as in biomedical sensing applications only need

smaller neural networks to make the sensor intelligent. Likewise, many time-series based prediction problems use one-dimensional data that again only need simple recurrent neural networks.

The practical implementation of large scale networks is required to match the neural network scale and size of the human brain [41–46]. Packing billions of neurons into a single chip is a major challenge, that requires to match the energy benchmarks and complexity. Current circuit implementations fail to match up with the energy benchmarks of the human brain, mainly as the scaling of power supply on chips are practically limited by electrical design and device constraints. In addition to this, packaging and electromagnetic effects also play a major role in building systems with neural chips. The precision engineering of these chips for reliable use is important for long term acceptability in higher intelligence tasks. Further, the data processing with the neurochips can be prone to adversarial attacks, which means the system needs to be made secure using dedicated cryptographic coprocessors. Going further, it will be also important to see the applications of these neurochips in human-machine interfaces, and for building connected and collective intelligence solutions.

Ageing is a time-dependent process, where the conductance of the memristors changes over a period of time and use [15, 16, 47–49]. The more the memristors are used, i.e., writing and reading, the ability to keep the expected conductance levels diminishes. This is wearing out the phenomenon that the memristor devices face due to continuous electrical stress on the devices impacting the chemistry and physics of the device. Over a period of time, the multiple conductance states get combined, or disappeared, making the reliability of programming memristors challenging. This makes fine-tuning as an essential part of memristor programming and test stages. Any changes in the conductance values introduce undesirable errors in the output of the crossbar arrays, which is far from expected ideal behaviour. This is a serious issue when the multiple conductance states are extensively used for building analog neural networks with crossbar arrays. The conductance of the memristors is equated to weights in the analog neural network, and hence if a conductance state goes missing it makes the training more complicated. Additional, rules need to be framed to the pre-trained network models to further adjust the weight values to achieve convergence. Learning and self-tuning in this sense is an online process for analog neural networks with memristor crossbar arrays. Nonetheless, the advantages of the analog neural networks with crossbar outweigh the digital-only counterpart, for smart sensor integration and edge AI computing [50–59].

When the noise gets added to the signals at input, in-network layers or outputs of the analog neural network, it introduces errors in the layers of the neural networks. The noise can originate in different ways, such as due to thermal effects, electromagnetic effects, or through external sources. Noise is typically seen as a problem in circuits, however, with neural networks this may have some advantages to offer, such as with avoiding overfitting during training. The role of noise in the human brain is immense and it plays some major role in the way intelligence and perception is shaped [60, 61].

4. Conclusions

There are several open challenges in neuro-memristive circuit design. The design challenges go from classical circuit analysis to computer-aided design issues. The major bottleneck with creating a billion-neuron chip is the limitations imposed at the device and at architecture levels. There are yet no practical tools that can help address all the design challenges in a systematic way. Unlike software tools, where

debugging is a well-detailed topic of study, the neuro-memristive hardware design is not easy to debug due to a variety of non-idealities of crossbar and memristor devices. There have been several proofs of concepts of circuit designs and a growing body of literature on architectures that aim to address these very challenges. However, there is a long way to go before many of these designs can be put for commercial use on a large scale. The digital designs of neural networks are much more feasible than analog neural networks at this point in time. In the future, it is expected that analog neural networks will have a much more important role to play in making sensors smarter and make intelligent computing energy-efficient.

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Chapter 2

Memristor Synapses for Neuromorphic Computing

Sanghyeon Choi, Seonggil Ham and Gunuk Wang

Abstract

Neuromorphic computing, which imitates the principle behind biological synapses with a high degree of parallelism, has recently emerged as a promising candidate for novel and sustainable computing technologies. The first step toward realizing a massively parallel neuromorphic system is to develop an artificial synapse capable of emulating synapse functionality, such as analog modulation, with ultralow power consumption and robust controllability. We begin this chapter with a simple description of neuromorphic systems and memristor synapses. Further, we introduce and evaluate the state-of-the-art neuromorphic hardware technology in terms of novel functional materials and device architectures toward the implementation of fully neuromorphic computers, which have been extensively explored in recent years. Finally, we briefly describe artificial neural networks based on memristor synapse in forms of crossbar arrays.

Keywords: memristor, artificial synapse, neuromorphic, bio-inspired, memristive systems

1. Introduction

Modern computers and electronics, such as smartphones and supercomputers, have been developed in accordance with Moore's law [1], which implies improvement in cost, speed, and power consumption by scaling down devices. However, the fundamental physical limits and increased fabrication costs pose a hindrance to sustainable development of computing technology [2, 3]. Moreover, with the advent of the big data era, unstructured data and data complexity explosively increases, imposing constraints on the conventional computing technology owing to the von Neumann bottleneck [4, 5]. Neuromorphic systems [6, 7], which mimic the nervous system in the brain, have recently become known as strong candidates to overcome these technical and economic limitations owing to their proficiency in cognitive and data-intensive tasks, together with their low power consumption. To successfully implement these neuromorphic systems, it is of utmost importance to research and develop artificial synapses capable of synapse functions, high reliability, low energy consumption, etc. [8, 9]. In the plethora of possible devices, memristors have gained the spotlight because of their desirable characteristics as artificial synapses [10–12], including device speed [13], footprint [14], low energy consumption [15], and analog switching [16, 17].

In this chapter, we introduce the basic concepts of neuromorphic systems and memristor synapses. We also describe diverse examples for state-of-the-art artificial synapses in terms of novel functional materials and device architecture. We then briefly review the implemented neuromorphic systems based on memristor synapses.

2. Neuromorphic systems and memristor synapses

2.1 Neuromorphic systems

Conventional computing architecture, that is, von Neumann architecture, forms the groundwork for modern computing technologies [3, 18]. Despite tremendous growth in computing performance, classical architecture currently suffers from the von Neumann bottleneck, which results from data movements between the processor and the memory unit [4, 5]. The memory wall issue, causing high power consumption and low speed, hinders the continuous development of computing technologies [4, 5, 9]. Moreover, artificial neural network (ANN) algorithms, such as deep learning [19], deal with image classification [20, 21], sound recognition [22, 23], specific complex tasks (e.g., the AlphaGo [24]) and so on. Although the ANN algorithms have exhibited superior performance over the conventional computing technologies, they are, at present, constructed on the von Neumann architecture; hence, considerable time and energy resources are required for their operation [8, 9]. Neuromorphic architecture [6, 7], a bio-inspired computing architecture, is one of the most promising candidates to resolve these problems. The neuromorphic systems take advantage of the cerebral nervous system, which consists of a massive parallel connectivity between the neurons (i.e., processor) and the synapses (i.e., memory), indicating the absence of the von Neumann bottleneck [8, 9]. **Figure 1** shows the shift of the computing architecture from von Neumann architecture (**Figure 1a**) to neuromorphic architecture (**Figure 1b**). The von Neumann architecture shows that the processor and memory are separate, leading to the von Neumann bottleneck. In contrast, in the case of neuromorphic architecture, the neurons and synapses are combined, alleviating the bottleneck issue. The neurons are uncomplicated computing units, the synapses are local memory units, and the communication channels (red line) connect numerous neurons and synapses. It should be noted that the practical purpose of neuromorphic systems is not to replace the von Neumann architecture completely, but to supplement the conventional architecture to make up its leeway, especially for intelligent tasks such as image recognition and natural language processing.

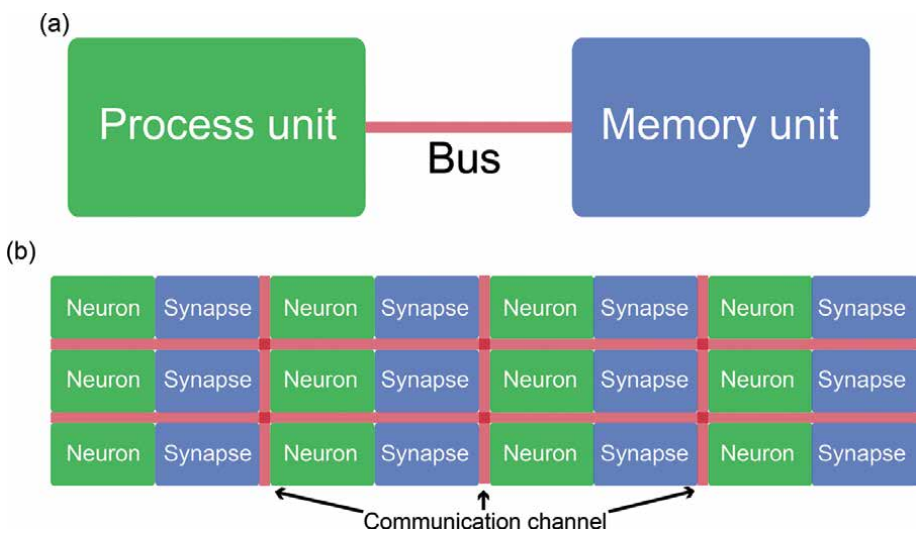

Figure 1.
(a) Conventional computing architecture (von Neumann architecture). Data transfer is performed through the bus (memory wall). (b) Neuromorphic architecture. In contrast to von Neumann architecture, von Neumann bottleneck does not exist.

2.2 Memristor synapses

Memristors that consist of a storage layer inserted between the top and bottom electrodes can undergo dynamic reconfiguration within the storage layer with the application of electrical stimuli, resulting in resistance modulation referred to as memory effect [16, 17]. The changed resistance state can be retained even after electrical inputs are removed, and memristors are based on the history of applied electrical stimuli. These capabilities lead to analog switching, which resembles biological synapses where the strength (or synaptic weight) can increase or decrease depending on the applied action potential [25, 26]. When neuromorphic architecture is implemented on the conventional computing architecture, the synaptic weights are stored in the memory unit and are continuously read into the processor unit to transfer information to post-neurons. In other words, practically, the von Neumann bottleneck still remains challenged. However, in case of memristor synapse-based neuromorphic systems, the synapses can not only store a specific weight but also naturally transmit information into post-neurons, overcoming the von Neumann bottleneck and improving system efficiency [8, 9]. In addition to analog switching, memristors have exhibited desirable device properties, including nanoscale footprint [14], long endurance and retention [17, 27], nanosecond switching speed [13, 15], and low power consumption [15]. Owing to these characteristics, memristors have emerged as promising candidates for artificial synapses. However, it should be noted that no specific material/device system has shown all-encompassed characteristics so far.

2.3 Switching mechanisms

Depending on their storage layer and electrode, memristors can be broadly classified into two categories: cation-based devices and anion-based devices. It is widely believed that cation-based devices are based on migration of metallic cations (see **Figure 2a**) [17, 28]. They employ electrochemically active materials such as Ag or Cu as an electrode [29–32]. The counter electrode is usually an electrochemically inert material, such as Pt, Au, or W, and the storage layer consists of a solid-electrolyte like Ta_2O_5, SiO_2, or Cu_2S. For example, when a positive voltage is applied to an Ag top electrode, the atoms from this electrode are electrochemically oxidized to Ag^+ cations because of anodic reaction, which are then dissolved into a solid-electrolyte layer. The Ag^+ cations migrate across the solid-electrolyte layer toward the counter electrode (e.g., Pt) depending on electric field. At the Pt electrode, the Ag^+ cations are electrochemically reduced to Ag atoms because of cathodic reaction and are deposited on its surface. Thus, conductive filaments grow toward the Ag top electrode, and eventually the filaments bridge the anode and the cathode, indicating that the device switches into ON state (low resistance state) as shown in **Figure 2a**. In contrast, when a negative voltage is applied to the Ag top electrode, the Ag filament begins to dissolve anodically, starting from the interface of the Ag top electrode/Ag filament, which results in OFF state (high resistance state). Owing to this process, cation-based devices are referred to as electrochemical metallization memories and conductive bridging random access memories. It should be noted that the initial formation of conductive filaments is called the electroforming process, which needs a voltage higher than a switching voltage.

Anion-based devices usually require the initial electroforming process and are switched depending on the O^{2-} anions (or positively charged oxygen vacancy V) induced into the storage layer by soft-breakdown (see **Figure 2b**). These devices consist of a sub-stoichiometric storage layer made of HfO_x [33, 34], TaO_x [35, 36], WO_x [37, 38], etc. When a positive forming voltage is applied to the top electrode,

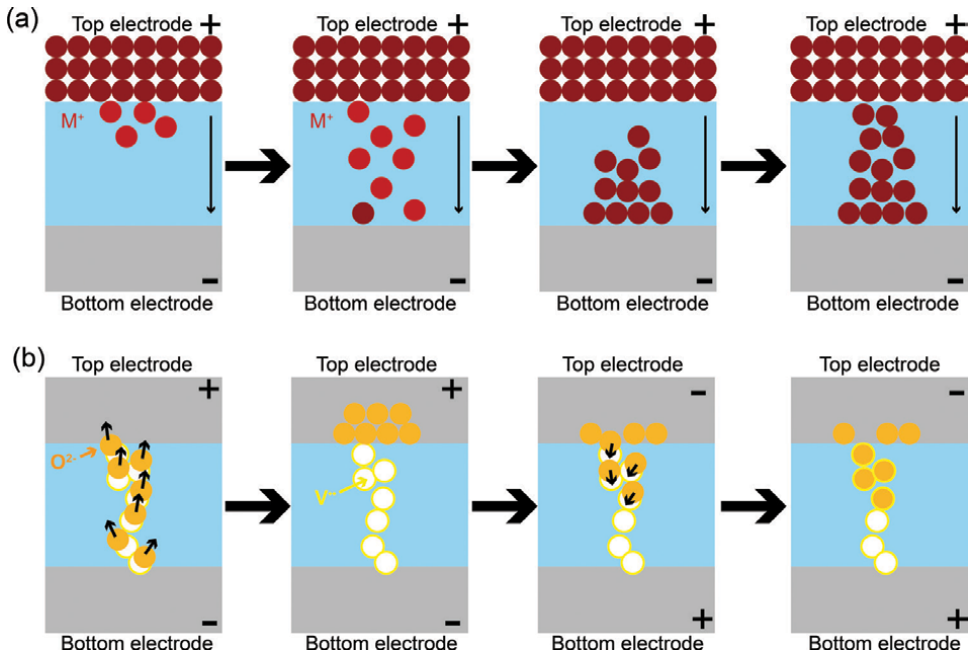

Figure 2.
(a) Cation-based devices: Through electrochemical reaction, metal cations M^+ migrate toward the counter electrode and form conductive filaments between the top and bottom electrodes. (b) Anion-based devices: During electroforming, the soft-breakdown leads to O^{2-} ions (oxygen vacancies V), and the oxygen vacancies form conductive filaments between the top and bottom electrodes.

the induced O^{2-} ions migrate toward it. This anion motion causes a change in the valence state of the cation to keep the charge neutral; hence, these devices are also referred to as valance change memories. Throughout the process, the oxygen vacancies continue to form conductive filaments in the storage layer. When the filaments bridge the top and bottom electrodes, current flows through the filaments, with the result that the device switches to ON state. Contrastingly, when a negative voltage is applied to the top electrode, the O^{2-} ions either recombine with oxygen vacancies present in the filaments or oxidize the cation precipitates, with the result that the device switches to OFF state. Thus, memristors could be understood to some extent based on cation- and anion-based mechanisms. However, identifying the precise mechanism of a specific device is a challenge because of the presence of mingled mechanisms and different driving forces or locations. Therefore, further studies are necessary for a deeper understanding of the switching mechanism.

2.4 Desirable properties of memristor synapses

Various properties of memristor synapses that affect the performance of neuromorphic computing need to be discussed in detail. Among them, representative characteristics such as the linearity in weight update, multilevel states, dynamic range (ON/OFF ratio), variation, retention, endurance, and footprint will be addressed in this section as they can substantially affect computing achievements [8, 35]. The linearity of the weight update indicates the linear relationship between synaptic weight change (Δw) and programming pulse. In other words, the conductance of the memristor synapse changes linearly in accordance with the number of programming pulses, which is associated with the mapping of weight in the algorithms for conductance in memristor synapses. Hence, the linearity of weight update affects the performance (e.g., accuracy). Notably, most memristor synapses

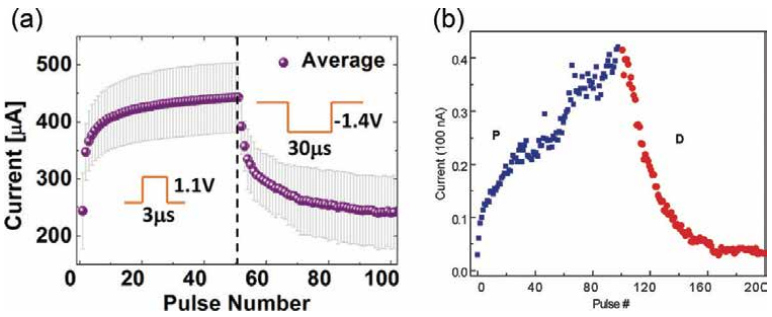

Figure 3.
(a, b) Nonlinearity of weight update. Current abruptly changes in initial pulses and gradually saturates. Most memristors exhibit a nonlinear relationship. All figures are reproduced with permission from Ref [39, 10], respectively. Copyright (2017, 2010) American Chemical Society.

show a nonlinear weight update, where the conductance change gradually saturates, as shown in **Figure 3**. Hence, the nonlinearity of weight update should be improved to achieve highly efficient computing.

The resolution capability of storage is influenced by multilevel states and dynamic ranges because numerous conductance states can distinguishably store individual pixels of input patterns. Moreover, variations, including cycle-to-cycle and device-to-device variations, could degrade neuromorphic computing, particularly in large-scale systems. However, considering that neuromorphic computing exhibits the fault-tolerant property, neuromorphic architectures could be immune to the variation to some extent, and this is supported by several papers [8, 35, 52]. In addition, memristor synapses are repeatedly updated during the training process and should retain the trained weights (i.e., final conductance). Subsequently, the larger the endurance cycles and retention time, the better are the achievements of the neuromorphic network. Last but not least, it is desirable that device's footprint is below sub-10 nm because high density leads to more synaptic devices that store learned information under a specific area [8].

Furthermore, it is efficient to improve the characteristics of memristor synapses depending on individual neuromorphic networks, because a desirable memristor synapse capable of being employed into neuromorphic systems is yet to be reported. Supervised learning-based networks [35, 40–44], for example, are less vulnerable to cycle-to-cycle and device-to-device variations. This is because memristor synapses are updated according to calculated errors under known target values. By contrast, the networks based on unsupervised learning [39, 45–47] are directly affected by the variation owing to unknown target values. Therefore, memristor synapses need to be designed or selected depending on individual neuromorphic networks.

3. Artificial synapses in terms of device architecture and novel functional materials

Memristors for synaptic devices with two-terminal (e.g., vertical/planar-type and gap-type) and three-terminal (e.g., field-effect transistor and lateral coupling type) structures are manufactured by well-established processing technologies [7–12, 35, 39–55].

In the case of a two-terminal structure, when different voltages are applied to each of the two electrodes, resulting in current flow through the insulator, varying the conductance of the device enables emulation of biological synapse functions such as synapse plasticity [10–12, 16, 35, 48]. In particular, the crossbar array of

two-terminal devices has received attention because of its characteristics relevant to synaptic devices, such as scalability for high density, simple fabrication process, low cost of fabrication, parallel connection structure, low power, fault-tolerance, and compactness. Thus, they are expected to provide an appropriate structure to support synaptic electronics. The type of two-terminal memristors that are being reffered to as the artificial synapses includes resistive random-access memory, phase change memory, conductive bridge memory, and spin-based memory. Although two-terminal devices are attracting much attention because of their ease of implementation of crossbar arrays, a two-terminal device, as a matter of fact, requires a select device to eliminate the sneak path that occurs in a crossbar array configuration. Additionally, it is difficult to imitate complex synaptic functions such as hetero-synaptic plasticity (e.g., modulatory input-dependent plasticity).

Three-terminal structures (e.g., field effect transistor memory and floating/gate transistor memory) with tunable conductance of channels between the source and the drain are also considered as synaptic devices [49–51]. The gate electrode acts as the pre-synapse, transferring the stimulus to the insulating layer, indicating the cleft of the synapse, and modulates the conductance of the channel representing the synaptic strength. Although the three-terminal structure is more complicated than the two-terminal structure and is disadvantageous in terms of density, the terminal for the signal transmission process and the learning terminal are separated such that simultaneous signal processing is possible, and complex synapse functions such as hetero-synaptic plasticity can be mimicked. Moreover, they do not require an additional selector device to reduce sneak current in an integrated array architecture.

Recently, going beyond simply implementing a synapse function, researchers have demonstrated advanced concepts of synapse device functions, including self-rectification, photo-assisted synaptic plasticity and neuromodulation to achieve more delicate imitation of the human brain and learning-and energy-efficiency in neurocomputing.

In [35], Choi et al. fabricated a self-rectifying memristor synapse through a two-terminal structure (Pt/TaO_y/nanoporous TaO_x/Ta), which is capable of suppressing unwanted leakage pathways and then a 16 x 16 crossbar array using only the devices without an additional selector (see **Figure 4a** and **b**). The mechanism of memristive switching and synaptic functions, including long-term potentiation (LTP), STDP (spike-timing dependent plasticity), and long-term depression (LTD) were caused by the migration of O^{2-} ions with oxygen vacancies V by applied electric field in the TaO_x. In addition, the asymmetric interface contacts of Pt/TaO_y and TaO_x/Ta prevent the undesired signal by performing the self-rectification function without the selector.

In [51], Huh et al. reported a synapse device that performs the neuromodulator function of a barristor structure using 2D material as shown in **Figure 4c**. The three-terminal device consisted of a vertically integrated monolithic tungsten oxide memristor, and a variable-barrier tungsten selenide/graphene Schottky diode, termed as a "synaptic barrister." This synaptic barristor could implement fundamental synaptic functions, including short-term plasticity (STP), paired pulse facilitation (PPF), LTP, and LTD, with external gate controllability, termed as a neuromodulator in bio-synapse. This architecture potentially offers considerable power-saving benefits while significantly tuning the synaptic weights and intrinsically modifying the synaptic plasticity, in comparison with conventional two-neuronal-based synaptic architectures.

In [52], Ham et al. fabricated an organo-lead halide perovskite (OHP)-based photonic synapse in which the synaptic plasticity is modified by both electrical pulses and light illumination. The switching mechanism originates from the presence of a conductive filament by iodine-vacancy mediator, with its switching states controlled by electric-field domination (see **Figure 4d**). Using diverse electrical stimuli and

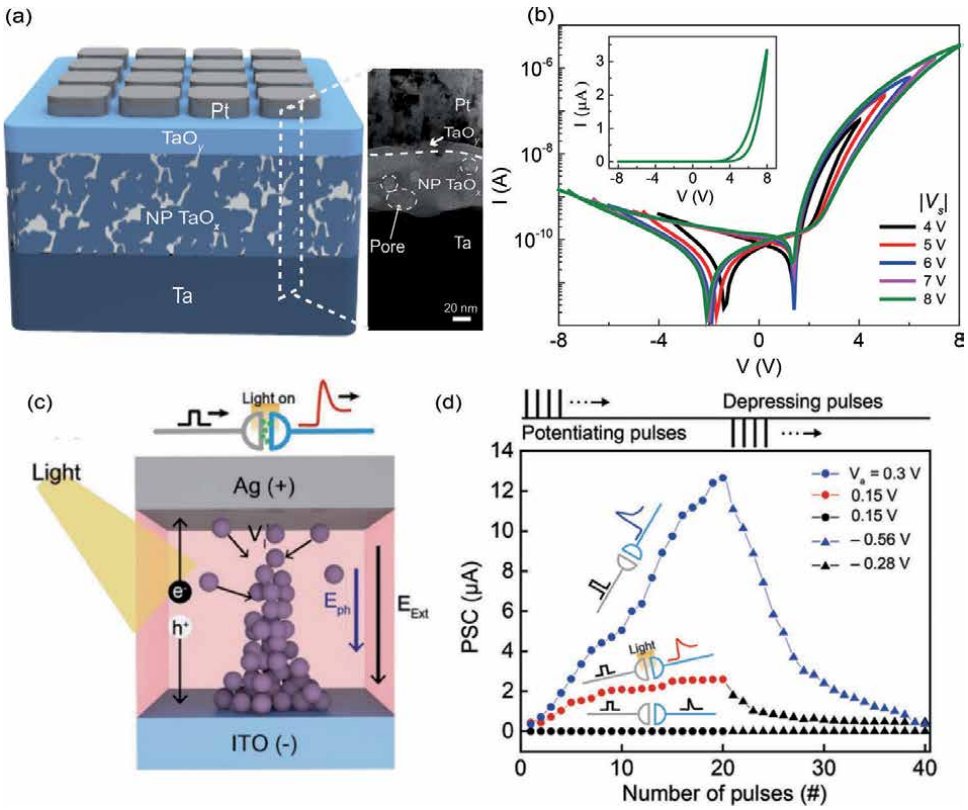

Figure 4.
(a) Schematic of a self-rectifying memristor with a Pt/TaO$_y$/nanoporous TaO$_x$/Ta and cross-sectional image of a memristor synapse. (b) I-V curves of the self-rectifying memristor synapse. (a, b) are reproduced with permission from Ref [35] under a Creative Commons Attribution 4.0 International License. (c) Schematics of the suggested mechanism of how a conductive switching filament is formed by the iodine vacancy migration in the presence of light. (d) Synaptic potentiation and depression behavior of the OHP-based synaptic device. (c and d) are reproduced with permission from Ref [52]. Copyright (2018) John Wiley and Sons.

relative timing between the input pulses, essential synaptic functionalities such as STP, LTP, and LTD were successfully demonstrated. In addition, owing to the accelerated migration of the iodine vacancy inherently existing in the coated OHP film under light illumination, the OHP synaptic device exhibits light-tunable synaptic functionalities with very low programming inputs (≈0.1 V) as shown in **Figure 4d**. The ability of high-order tuning of the photo-assisted synaptic plasticity in an artificial synapse can offer significant improvements in the processing time, low-power recognition, and learning capability in a neuro-inspired computing system (**Figure 4e**).

In [12], Wang et al. designed a diffusive memristor for STP synapses and threshold neurons. The devices contain a switching layer doped with Ag nanoclusters (MgO_x:Ag, SiO_xN_y:Ag, and HfO_x:Ag) using the co-sputtering method. The switching mechanism is based on the growth and relaxation of Ag nanoclusters depending on whether the voltage pulse is applied, which was experimentally verified by in-situ high-resolution transmission electron microscopy (HRTEM). The designed device mimicked STP under PPF and PPD. Moreover, the device was used as a threshold neuron along with drift memristor synapse based on TaO_x to emulate STDP learning rule. Because the conductance of the device gradually increases according to applied voltage and then abruptly decreases under no applied voltage, the device can be used as a threshold neuron. The results give a potential application for simple artificial neurons as compared with CMOS artificial neurons [53, 54].

4. Neuromorphic systems based on crossbar array of memristor synapses

Prezioso et al. experimentally demonstrated neuromorphic networks based on memristor synapses (see [55]). In their paper, Al_2O_3/TiO_{2-x} memristor was used to fabricate a 12 × 12 crossbar array to implement a single-layer network [56]. The single-layer network architecture was schematically described as shown in **Figure 5a**, where 10 input neurons and 3 output neurons are fully linked by 10 × 3 = 30 synaptic weights ($W_{i,j}$). Notably, this ANN architecture naturally corresponds to a crossbar array [9, 35]. Input voltages ($V_{i\,=\,1...9}$) assigned from pixels of the 3 × 3 input images (see **Figure 5b**) were applied to each input neuron. After being applied into the network, the input voltages were individually weighted depending on each synaptic weight. Note that V_{10} is a bias voltage to control the degree of activation of the output neurons. The output neurons received each weighted voltage through linked weights and then integrated the weighted voltages ($\sum W_{i,j}V_j$), where j and i represent the input (j = 1–9) and output (i = 1–3) neurons respectively. The output neurons converted each integrated voltage into output (f_i) ranging from −1 to 1 according to the nonlinear activation function: $f_i = \tanh(\beta I_i)$, where β adjusts the nonlinearity of the activation function and $I_i = \sum W_{i,j}V_j$. The activation function can be considered as the threshold firing function in a biological neuron. The synaptic weights were represented by a pair of adjacent memristors ($W_{i,j} = G_{i,j}^{+} - G_{i,j}^{-}$) for the effectiveness of weight update. The number of selected memristor synapses in 12 × 12 array were 30 × 2 = 60, due to a pair of memristors (**Figure 5c**). When the network was under the training process, as shown in **Figure 5d** and **e**, memristor synapses between input and output neurons were updated based on the Manhattan update rule, which is classified as supervised learning: $\Delta W_{i,j} = \eta \mathrm{sgn}\sum[(t_i(\mathrm{n}) - f_i(\mathrm{n})) \times \mathrm{d}f/\mathrm{d}I \times V_j(\mathrm{n})]$,

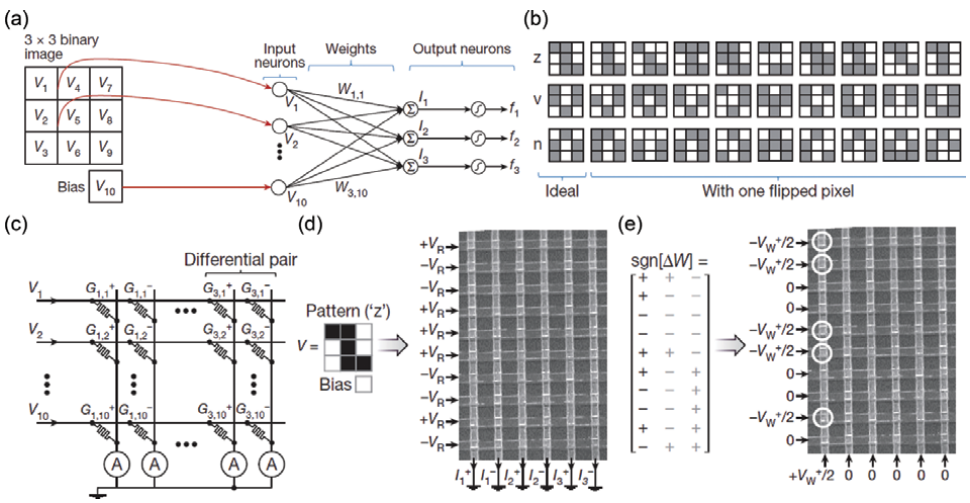

Figure 5.
(a) Input voltages corresponding to an input image ($V_{i\,=\,1...9}$) and a bias voltage (V_{10}). These voltages are fed into the single-layer network where 10 input neurons and 3 output neurons are linked by synaptic weights. (b) The "z," "v," and "n" input images. Aside from ideal images, other images contain one noise pixel. (c) The schematic of implemented 10 × 6 crossbar array, a pair of adjacent memristors provide one synaptic weight. (d) When an image (e.g., "z") is fed into network, pixels for black give V_R (read voltage) to the network, otherwise, $-V_R$ is applied into the network. (e) An instance of weight update according to Manhattan update rule. The synaptic weights corresponding to sign + should be increased, so that the memristors representing $G_{1,1}^{+}$, $G_{1,2}^{+}$, $G_{1,5}^{+}$, $G_{1,6}^{+}$, and $G_{1,9}^{+}$ are applied by set voltage. All figures are reproduced with permission from Ref [55]. Copyright (2015) Springer Nature.

where η is the learning rate, t_i(n) is the target value, f_i(n) is the output value, and n is the nth input image. After the training process was complete, the memristor synapses retained their final conductance, and the test process was performed without weight update (see **Figure 5d**). From the test process, the neuromorphic network exhibited perfect classification for the first time in 21 epochs (note that one epoch indicates one training process). Although simple and few input images were used to train/test the neuromorphic network, this work greatly contributed to neuromorphic systems based on memristor synapses in terms of experimental demonstration using crossbar arrays.

It should be noted that the circuit that acquires $\mathrm{sgn}[f_i(\mathrm{n})] = \mathrm{sgn}[\sum W_{i,j}V_j] = \mathrm{sgn}[\sum(G_{i,j}^{+} - G_{i,j})V_j]$ could be implemented by a virtual ground circuit and a differential amplifier [43, 57]. Then, the output value is compared with the target value by circuits using a comparator. According to calculated $\Delta W_{i,j}$, programming memristors of the array, for example, could be performed as shown in **Figure 6** [39]. The test board contains four digital-to-analog converters (DACs) providing voltage pulses through the DACs. The DACs 1–4 represent the chosen bottom line, the unchosen bottom line, the chosen top line, and the unchosen top line, respectively. Using matrix switches (Switch 1 and 2), individual memristor is assigned to the corresponding DAC. The multiplexer (MUX) is operated to obtain currents that flow through memristors in the array by delivering the currents into the analog-to-digital converter (ADC). The ADC obtains the applied voltage of the resistor (1 kΩ), and the voltage is changed into the current. The arrows of **Figure 6** represent the current flowing through a chosen memristor in case of write, erase, and read processes. Notably, there are non-idealities such as sneak currents and wire resistance in array-level, which could degrade the performance of neuromorphic computing [35, 44, 58–60]. The sneak currents affect learning accuracy and epochs because of undesired information, especially large-scale array. In **Figure 6**, in order to avoid sneak currents during read process, unchosen rows and columns are grounded [39]. Moreover, wire resistance consumes input voltages, so that memristors far from points of input voltage could be applied by smaller voltage than input voltage.

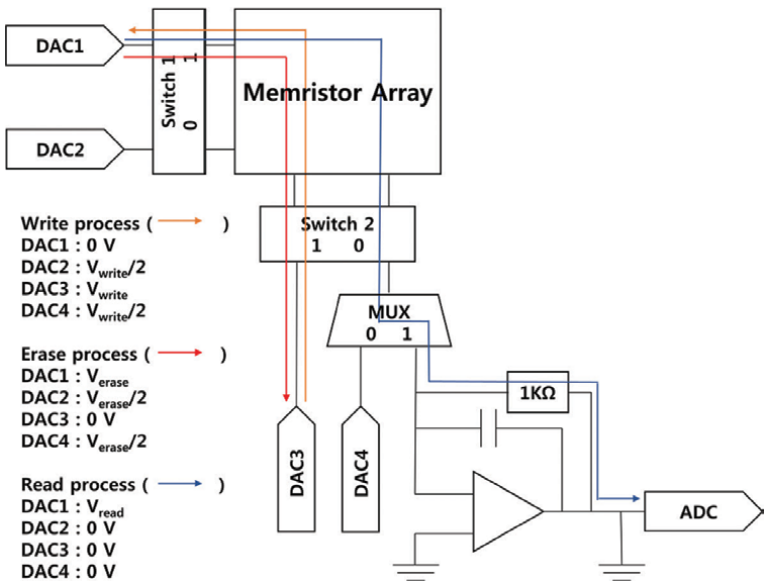

Figure 6.
Circuit scheme for write, erase, and read processes. The figure is reproduced with permission from Ref [39]. Copyright (2017) American Chemical Society.

This influences output currents, leading to degradation of learning performance. The non-idealities in array-level could be overcome by device functions [35, 44], operational scheme [39, 58–60], or learning algorithms [35, 40–44] to some degree.

5. Conclusion

Neuromorphic systems are one of the most promising candidates to deal with the von Neumann bottleneck caused by the memory wall between memory and process units. Using memristor synapses simply classified into cation- and anion-based devices can resolve this bottleneck owing to their storage and transmittance capabilities. To obtain higher performance of neuromorphic systems, representative characteristics, including the linearity of weight update, large multilevel states and dynamic range (ON/OFF ratio), variation and endurance, and retention need to be improved. In this context, different memristor synapses based on novel materials and device structures were introduced. Finally, we have briefly explained neuromorphic networks based on crossbar arrays of memristor synapses, and the network demonstrated perfect classification after 21 epochs. We believe that this chapter offers a deep understanding of the field of memristor synapses.

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Conflict of interest

The authors declare no competing interests.

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Chapter 3

Coexistence of Bipolar and Unipolar Memristor Switching Behavior

Sami Ghedira, Faten Ouaja Rziga, Khaoula Mbarek and Kamel Besbes

Abstract

The memristor has been theoretically investigated as one of the fundamental electrical elements by Pr. Leon Chua in 1971. Meanwhile, its electrical characteristics are not yet fully understood. The nonlinear characteristics and the ability to examine large-scale amounts of storing data of this device reveal an interesting development in emerging electronic systems. Research on memristor modeling based on SPICE tools has grown rapidly. This leads us to study the behavior of such devices. Our aim is to simulate different types of memristor behavior. The adjustment of the model is based on the implementation of several parameters, which enables the switching of this device. In this chapter, we prove the flexibility and the correlation of memristor model with different memristive characterization data, by applying different voltage bias, sinusoidal and with a repetitive sweeping. Moreover, we demonstrate the memristor behavior as four types of switching. This includes bipolar switching, unipolar switching, bipolar switching with forgetting effect, and a reversible process between bipolar and unipolar switching. In order to validate this study, we compare our simulation results with experimental data and we prove a good agreement. The SPICE model used in our simulations shows a special advantage for its flexibility and simplicity.

Keywords: memristor, I-V characteristics, SPICE model, switching behavior, hysteresis loop, bipolar behavior, unipolar behavior

1. Introduction

Significant interest has been focused on the development of memristor-based systems. It has been first developed on symmetry consideration by Prof. Leon Chua in 1971 [1, 2]. In addition, it has been admitted physically by the HP Labs Team in 2008 [3]. This device does have a great potential to be the future memory cell, due to the small feature size and ability to retain the content (nonvolatile). The identity of such device is obvious on the *I-V* characteristics, i.e., its "pinched hysteresis loop." Thus, the choice of the model and the structure are necessary to achieve

better endurance and performance. Hence, the correlation of one model to other memristive devices is an interesting development to further research.

In the literature, memristor models studied in [3–10] have been published for basic mathematical functioning properties of the memristor, which have been proposed by HP Labs in [3]. Other models [11–14] focus on extracting the *I-V* characteristic of the model with other mathematical method using boundary conditions. They differ in complexity, materials, and accuracy. Thus, since our interest is in the behavior of the memristor, we choose to explore and investigate a simple SPICE model, which has been proposed by the present authors in [11]. The main differences are displayed in the implementation of parameters such as the state variable of the device. However, so far, no SPICE model could be correlated to several characterizations data of memristive devices. Our goal is to use a memristor model to analyze its functioning for different voltage bias. We study the dynamical behavior of memristor and we demonstrate that this model accounts for four different types of a memristor cited as the following: the bipolar behavior of memristor, the unipolar behavior, the bipolar with forgetting effect, and the reversible process between the bipolar and the unipolar behavior of memristor. Those types of memristor change under distinct stimulus such as sinusoidal, triangular, and repetitive DC sweeping voltage.

2. Theoretical principles

The wide variety in memristor structure and composition has led to the development of many different memristor modeling techniques. Some of them have been designed to represent a specific device for a specific type of application, such as AHaH [12], ANN [15, 16], Slime mold [17], and neuromorphic applications [5]. Implementation of the memristor could be generated on several tools of simulation, such as SPICE [18–25], Matlab [26–32], Verilog-A [33], and VHDL-AMS [34–37]. Resistive switching behavior is one of the fundamental properties showed in memristors; the well-known HP lab model of a memristor [3] shown in **Figure 1(a)** consists of a thin TiO_2 double-layer of width D between a pair of platinum

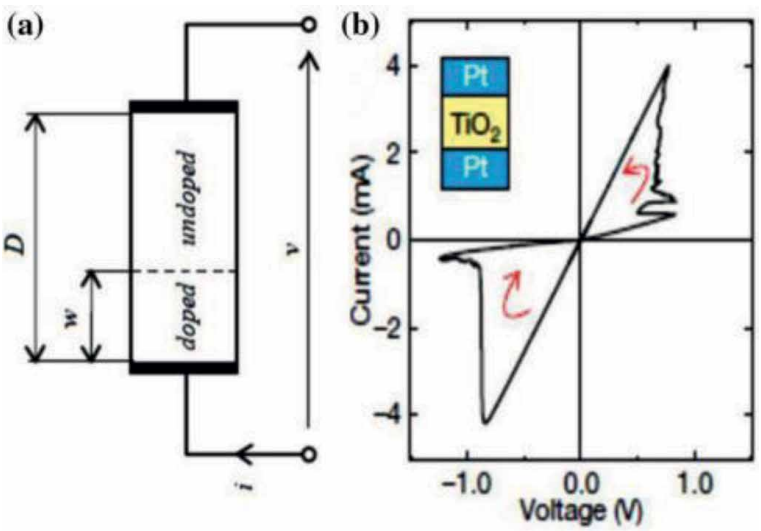

Figure 1.
Physical model of memristor [3]. (a) Memristor thin film. (b) Memristor hysteresis loop.

electrodes. One of the TiO_2 layers of width w is doped with oxygen vacancies. The second, undoped layer of width *w-D* has insulating properties. As a result of complex processes in the device, the width w of the doped layer varies by applying a voltage or current to the electrodes of the memristor, and there will be dramatic changes in resistance. Therefore, the boundary, defined as the state variable $x = w/D$, between the two layers moves simultaneously. The well-known characteristic of the memristor is shown in **Figure 1(b)**, the pinched hysteresis loop, which indicates the switching behavior of memristive devices. An application of a positive bias voltage to the electrodes of the device leads to the switching between Off and On states, and this switching is labeled SET. A RESET switching corresponds to the exchange between On and Off states. As current flows through the device, the cross section between the regions moves. As a result, the doped and the undoped regions have resistance R_{on} and R_{off} when each of them reaches the (D-w) and the full-length D, respectively. Also, the width w of the doped region of the memristor increases by applying a positive voltage bias, which causes the total resistance of the device to decrease. The same process is carried out by applying a negative voltage to the opposite side of the device. Moreover, there are two methods of the behavior of resistive switching for memristors: static and dynamic switching.

2.1 Static characteristics

The characteristic of a static switching behavior is obtained with a slow sweep of the voltage applied to the terminals of the device between the minimum and maximum values eligible (typically a triangular signal).

2.2 Dynamic characteristics

In dynamic switching, voltage pulses are applied to the device and the current rises under the constant voltage bias during the pulsing interval.

A comprehensive mathematical illustration of a SPICE memristor model has been reported in [11], which will be used later on for our simulation results. This model can illustrate the static and dynamic switching behavior, which will be studied in the next section. Thus, this model is based on the assumption that the switching behavior of the memristor is small or fast, below or above a threshold voltage V_{SET} or V_{RESET}, respectively, which is considered as the minimum voltage required to impose a change on the physical structure and thus the memristance of the device. This assumption is encapsulated in the use of the multiple implemented parameters, which are included in the set of equations below:

$$\mathrm{I(t)} = \begin{cases} a_1 x(\mathrm{t}) \sinh(\mathrm{bV(t)}), & V(\mathrm{t}) > 0 \\ a_2 x(\mathrm{t}) \sinh(\mathrm{bV(t)}), & V(\mathrm{t}) < 0 \end{cases} \tag{1}$$

The relationship between the memristor voltage and the memristor current is given by Eq. (1), and it comprises three main parameters: a_1, a_2, and b. These parameters are responsible for the modeling of the nonlinear phenomenon of the pinched hysteresis loop. a_1 and a_2 are the magnitude parameters that vary according to the polarity of the input voltage; it is also related to the thickness of the dielectric layer of the memristor. Meanwhile, b is defined as the control parameter, which refers to the amount of oxygen deficiencies presented in the device, and it controls the conductivity of the device. The main voltage equation is defined by the relation $g(t)$ defined below:

$$g(t) = \begin{cases} A_p\left(e^{V(t)} - e^{V_p}\right), & V(t) > V_p \\ -A_n\left(e^{-V(t)} - e^{V_n}\right), & V(t) < -V_n \\ 0, & -V_n \le V(t) \le V_p \end{cases} \tag{2}$$

Equation (2) incorporates the threshold voltage with V_p and V_n which refers to the positive and negative polarizations, respectively, which makes a change in the switching behavior for value below the external voltage of the memristor. A_p and A_n are fitting parameters that affect the conductivity of the device. Accurately, it controls the speed of the oxygen deficiencies motion. The demonstration of the linearity of the model is described by parameters included in the following equations:

$$f(x) = \begin{cases} e^{-\alpha_p(x - x_p)} w_p(x, x_p), x \ge x_p \\ 1, \quad x < x_p \end{cases} \tag{3}$$

$$f(x) = \begin{cases} e^{\alpha_n(x + x_n - 1)} w_n(x, x_n), x \le 1 - x_n \\ 1, \quad x > 1 - x_n \end{cases} \tag{4}$$

The physical parameters x_p and x_n have been defined in Eqs. (3) and (4); it represents the value of the state variable, which is responsible for the linearity of the device. Fitting parameters α_p and α_n are also included in these equations; are responsible for the linearity of the device; and they determine the degree of motion including the amortization of the state variable. The parameters w_n and w_p are defined by Eqs. (5) and (6), respectively. Those functions are used to shape the intensity of the state variable dynamics, i.e., the rate of memristance change.

$$w_p(x, x_p) = \frac{x_p - x}{1 - x_p} + 1 \tag{5}$$

$$w_n(x, x_n) = \frac{x}{1 - x_n} \tag{6}$$

Equation (7) represents the modeling function of the state variable. The fitting parameter η represents the direction of the movement of the state variable depending on the polarity of the input voltage. When $\eta = 1$, a positive voltage greater than the threshold voltage will increase the value of the state variable; and when $\eta = -1$, a positive voltage will decrease the value of the state variable.

$$\frac{dx}{dt} = \eta g(V(t)) f(x(t)) \tag{7}$$

Each pair of the parameters indicates the variation in the positive and negative region of the polarization. These multiple parameters make it possible for this device to be adaptable to a variety of characterization data of memristive devices, which we will discuss in the next section.

3. Analysis of the *I-V* characteristics

In our previous work [38], we illustrated a methodology for a simple memristor model to automatically adjust other behaviors of memristive devices. It effectively

demonstrates the basic *I-V* characteristics of a memristive device. In addition, it acts differently in the positive and negative regions of the applied voltage, and the implemented parameters of the device take account on this, which makes the analysis of the pinched hysteresis loop simple and coherent for the positive and the negative regions independently. Therefore, we analyze the fundamental fingerprint of the macromodel and its memristance switching behavior. In the simulation results of **Figure 2(a)**, we used a sinusoidal voltage 0.46 V with a frequency of 100 Hz, **Figure 2(b)** shows the resultant pinched hysteresis loop, which correlates the characterization data of the proposed model [11]. Thereby, our results agree well with the experimental results already published in [11], and we prove the linearity property of the device for a higher value of frequency. The next simulation results reveal the richness of memristor's switching behavior confirming the usefulness of the specific design approach. The effect of memristive switching is inspected by varying the implemented parameters of the model such as the magnitude of the voltage bias, the initial charge, and the state variable.

This changes the operating regime so the memristance value may not remain constant and the memristor operates in different segments or takes different memristance values. This sudden jump of memristance is called "memristive switching" or "resistive switching."

In this case, memristive switching depends on the bias of the applied voltage across the device, which is represented in **Figure 3(a)**, the curve of the state variable motion at memristor boundaries. We consider the memristor in an Off state, as an initial state of the device, switching the device to On state, requires a positive bias across the device. While switching it to Off state requires negative bias.

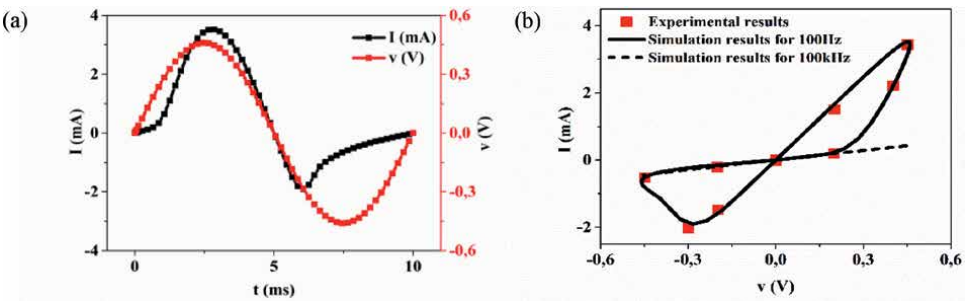

Figure 2.
(a) Curve of current and voltage applied to the terminals of the memristor. (b) Represents the resultant hysteresis loop at 100 Hz and 100 kHz where the deviates linear.

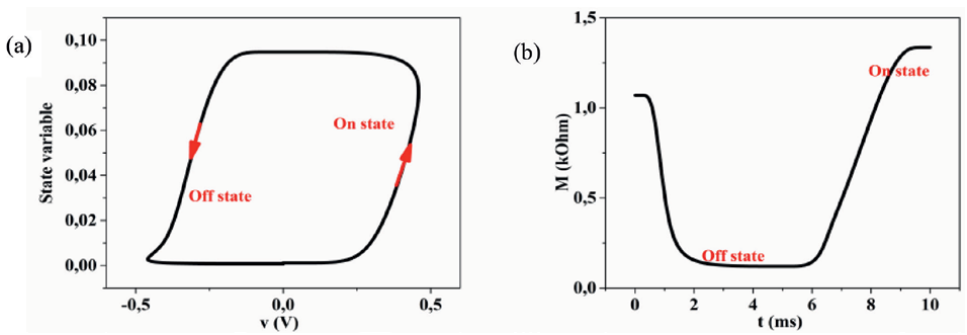

Figure 3.
(a) The state variable motion at memristor boundaries according to the applied voltage and (b) memristance behavior over time.

Figure 3(b) represents the curve of the memristance or the resistance of the memristor on the On and Off states. From this results, R_{on} and R_{off}'s value estimated by 1.3 *k*Ω and 1.1 *k*Ω, respectively.

4. Correlation of different memristive devices

In this section, we present our simulation results, in which we implement the different values of parameters on PSPICE, to fit a set of memristive devices studied for different types of applications. Those results describe the static and dynamical characteristics of the model. Thus, we prove that the SPICE model fits well with the characterization data of memristors defined in [8, 15, 17, 25, 39–44]. The polarization voltages studied are either sinusoidal pulses or repetitive DC sweeping voltage to represent the different switching resistive levels of the memristor. The simulation results of the proposed model [11] shown in **Figure 4**, which indeed shows the characterization data of several memristive devices. In these simulation results, we adjust the different implement parameters on the SPICE model to fit the experimental results presented in [11]. Thus, it describes the *I-V* characteristics for devices defined in [8, 9, 40–43], which has been correlated by the SPICE model.

a. **Figure 4(a)** describes the simulation results of the device published by the State University of Boise in [40].

b. **Figure 4(b)** describes the simulation results of the device published by the Tel Aviv University in [9, 41].

c. **Figure 4(c)** describes the simulation results of the device published by the University of Michigan in [8].

d. **Figure 4(d)** describes the simulation results of the device published by the state University of Iowa in [42].

e. **Figure 4(e)** describes the simulation results of the device published by the University of Michigan in [43].

4.1 Memristive device of the laboratory of slime mold

We adjust the implemented parameters to find the appropriate shape of *I-V* characteristics of the Slime mold device [17] shown in **Figure 5**, our results fits well the experimental results described in [17]. The application of Slime mold is a group of bacteria that lives mainly in the soil, which has the ability to change its shape by sliding every 50 s (by extension and retraction). This outcome contributes to the development of bioelectronics circuits of self-growth. The *I-V* characteristics curve for a DC voltage and a repetitive sweeping and the curve of the resistance of the device shown in **Figure 5(a)–(c)**, respectively. These results present the functionality of this model by applying a repetitive DC sweeping voltage to present the various resistance switching states.

4.2 Memristive device of Strachan of the HP laboratory

Another memristive device based on TaO_x was proposed by the team of HP Labs in [44]; we adjust the fitting parameters with the characterization data of this

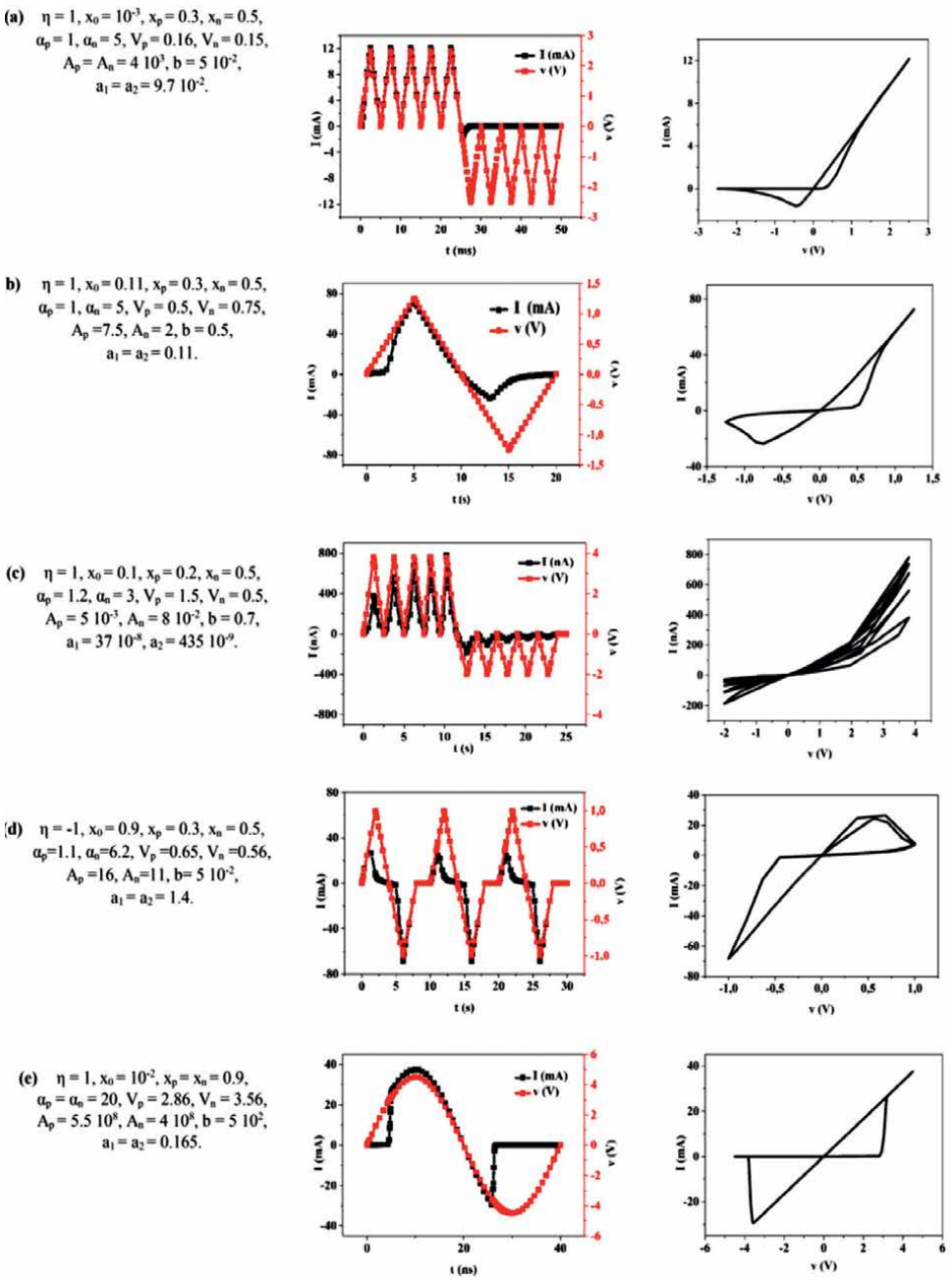

Figure 4.
(a) I-V curve of memristive device proposed by the State University of Boise [40], (b) I-V curve of memristive device proposed by the Tel Aviv University [41], (c) I-V curve of memristive device proposed by the University of Michigan in 2010 [8], (d) I-V curve of the device proposed by the State University of Iowa in 2010 [42], and (e) I-V curve of the device proposed by the University of Michigan [43] including the parameter values.

device. The results are shown in **Figure 6**; it agrees with the experimental results represented in [44]. The *I-V* characteristic curve for a DC voltage and a repetitive sweeping and the curve of the resistance of the device are shown in **Figure 6(a)–(c)**, respectively. The simulation results present the functionality of this model by applying a repetitive DC sweeping voltage to present the several resistance switching states.

4.3 Memristor of Nugent for AHaH applications

Our model also fits well a learning AHaH application accomplished by Nugent in [12]. After the application of a sinusoidal signal to the memristor with amplitude 0.25 V for a period 10 *m*s, we found the resultant *I-V* characteristics shown in **Figure 7(a)**, which seems compatible with the *I-V* characterization profile and it fits well the experimental results revealed in [12]. This model works well for a repetitive DC sweeping voltage which is represented by the *I-V* characteristics curves and the curve of the resistance of the device shown in **Figure 7(b)**, **(c)**. The simulation results present the functionality of this model by applying a repetitive DC sweeping voltage to present the several resistance switching states.

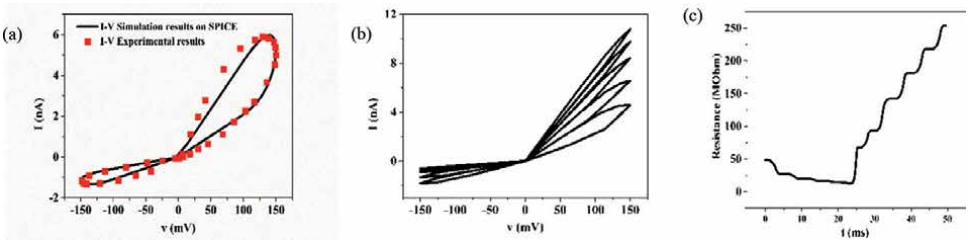

Figure 5.
Simulation results of the memristor model adapted to the I-V *characteristics profile of Slime mold memristive device, the Simulation value:* $\eta = 1$, $x_o = 0.11$, $x_p = 0.35$, $x_n = 0.55$, $\alpha_p = 1$, $\alpha_n = 5$, $V_p = 0.1$, $V_n = 0.1$, $A_p = A_n = 4\ 10^3$, $b = 2\ 10^{-5}$, $a_1 = a_2 = 17\ 10^5$.

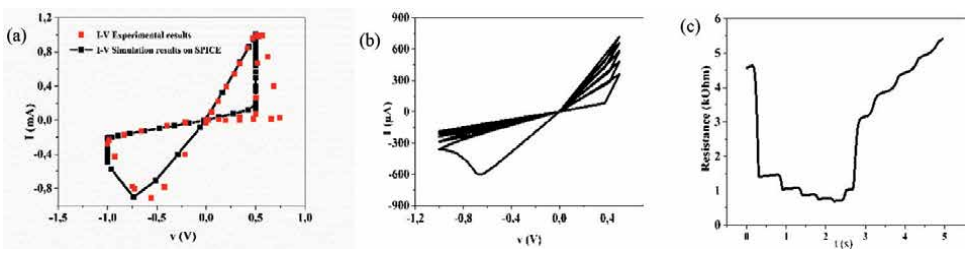

Figure 6.
Simulation results of the model adapted to the I-V characteristics profile of the memristive device of Strachan, the simulation value: $\eta = 1$, $x_o = 99 \times 10^{-3}$, $x_p = 0.3$, $x_n = 0.63$, $\alpha_p = 0.1$, $\alpha_n = 20$, $V_p = 0.49$, $V_n = 0.6$, $A_p = 400$, $A_n = 25$, $b = 1.3 \times 10^{-3}$, $a_1 = 1.7$, $a_2 = 1.2$.

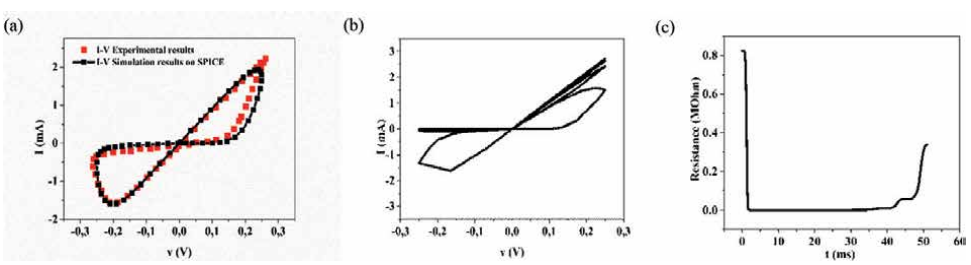

Figure 7.
Simulation results of the model adapted to the I-V *characteristics profile of the memristive device of Nugent, the simulation value:* $\eta = 1$, $x_o = 1.1 \times 10^{-4}$, $x_p = 0.3$, $x_n = 0.8$, $\alpha_p = 1$, $\alpha_n = 5$, $V_p = 0.1$, $V_n = 0.13$, $A_p = A_n = 4 \times 10^3$, $b = 6.5 \times 10^{-2}$, $a_1 = a_2 = 0.17$.

4.4 Memristive device of the University of Pittsburgh

The device represented by Zhang in [39] is based on TaO_x material. The simulation results of this device are represented in **Figure 8(a)** by applying a triangular voltage with a sweeping of the magnitude, 0.74 V for the positive region, and −1.25 V for the negative region. After adjustment of the parameters, we have a nonlinear *I-V* curve which seems to be compatible with the *I-V* characterization profile recorded in the experiments of HP labs in [39]. In addition, we proved the functioning of this device with a repetitive DC sweeping voltage to present several resistance switching states shown in **Figure 8(b)** and **(c)**.

4.5 Memristive device for ANN learning application

Meanwhile, we also simulated the model with a square wave excitation shown in **Figure 9**. This excitation method is used as a learning method, which presents the behavior of this model as an artificial neural network ANN [15]. We follow the learning experience carried out in [16]. As shown in **Figure 9(c)**, the memristance of the device increases along with the applied voltage. However, this behavior response is different from the other previous excitation, and this depends on the type of excitation and the followed current. The current curve decreases with each pulse of the excitation voltage positive and negative.

In conclusion, we notice that this SPICE model is a general model that can be applied in multiple domains. Furthermore, according to the simulation results of both devices Slime mold and HP Labs, we notice that the hysteresis loop of the memristor maintains its nonlinear shape even for a remarkable range of the values of the parameters. The speed of movement for the memristive devices of Slime mold and Nugent are faster compared to the other memristive devices since A_p and

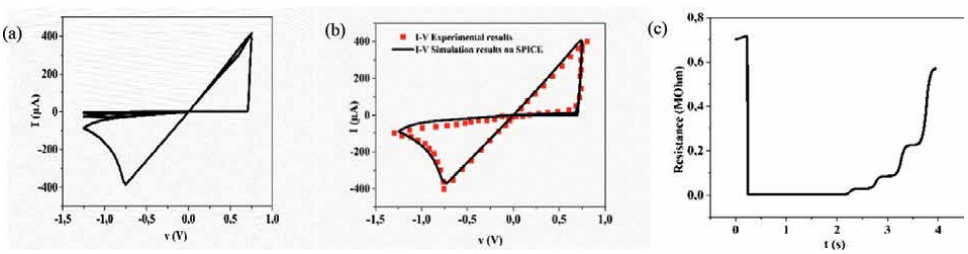

Figure 8.
Simulation results compared to the simulation result of Zhang, the simulation value: $\eta = 1$, $x_o = 55 \times 10^{-4}$, $x_p = 0.32$, $x_n = 0.1$, $\alpha_p = 1$, $\alpha_n = 5$, $V_p = 0.7$, $V_n = 0.75$, $A_p = 4 \times 10^3$, $A_n = 500$, $b = 11 \times 10^{-4}$, $a_1 = 0.17 \times 10^3$, $a_2 = 1.1 \times 10^3$.

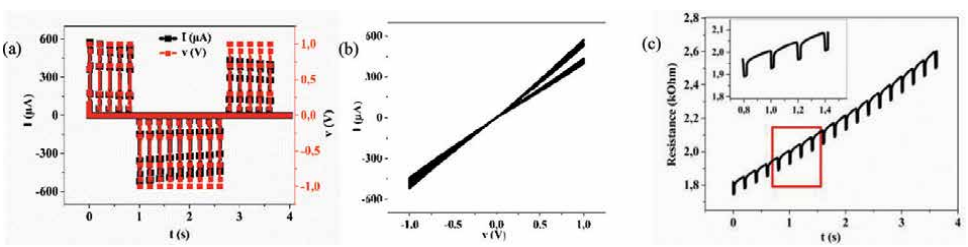

Figure 9.
Simulation results of the model adapted to learning application, the simulation value: $\eta = 1$, $x_o = 0.11$, $x_p = 0.3$, $x_n = 0.5$, $\alpha_p = 1$, $\alpha_n = 5$, $V_p = V_n = 1$, $A_p = A_n = 4$, $b = 0.5$, $a_1 = a_2 = 0.01$.

A_n have higher values. Thus, the memristive devices of Slime mold and Zhang application have the lowest values of b, which decrease its conductivity. The ANN learning application presents another type of excitation, which largely affects the dynamic of the memristor's behavior. Thus, we will deal later with the use of different memristor switching behavior, we demonstrate not only bipolar, but also the unipolar switching behavior of memristors, which differs from bipolar memristors in the fact that only the magnitude of the voltage across the device determines the change in the resistance.

5. Behavior of the SPICE model for different types of memristors

Memristor models, in literature, have different responses, which are generated for four different types of a memristor, i.e., bipolar, bipolar with a forgetting effect, unipolar and reversible behavior between the bipolar, and the unipolar memristor. For our simulation results, we used a SPICE model that can not only describe the basic memory ability of memristor, but also be able to capture all of the four types of memristor switching behavior.

Models with bipolar switching [45, 46] distinguishable by the memristance which increases and decreases by different polarity voltages. Models with unipolar switching behavior [45, 46] are distinguishable by its memristance, which can increase and decrease by the same polarity voltage. The bipolar with forgetting effect [47, 48] is distinguishable by its memristance which increases and decreases by a different polarity voltage, but memristance can spontaneously decrease at the same time, even with no voltage applied. The reversible bipolar and unipolar switching behavior [49], here the memristor will behave like a bipolar memristor at first, but after a few iterations, it will turn to a unipolar memristor.

In the same context, we use different polarization voltages, either sinusoidal or repetitive DC sweeping voltage, exploited in order to present the different states of resistance of the memristor, and thus it shows the behavior of the four different types of a memristor. Those results reveal the richness of memristor's dynamical behavior confirming the usefulness of the specific model approach.

To verify the memristive characteristics and the coexistence of different switching behavior of our proposed model, we employed different excitations presented in the following figures of the rest of the paper. In fact, to characterize different types of memristors, we need to verify the behavior of the model for the well-known fundamental switching behavior in both bipolar and unipolar switching behavior. In this case, we have adapted our model according to the experimental results demonstrated in [50]. These observations are consistent and in very good qualitative agreement with the experimental results of the memristor switching behavior already published in [50].

In addition, **Figure 10** shows the dynamical characteristics of a bipolar memristor behavior. The sweeping voltage bias approaches a set value v = 1.8 V

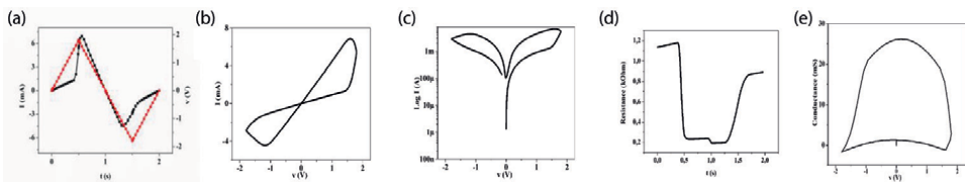

Figure 10.
Memristor SPICE model response for a bipolar switching behavior.

with current value I = 7 *m*A. Reversing the voltage polarity, the device switches to a reset value at v = −1.8 V with current value I = −4.5 *m*A. The attained pinched hysteresis *I-V* curves are shown in **Figure 10(b)**, **(c)**, which are the typical fingerprint of bipolar resistive switching. The corresponding resistance response is illustrated in **Figure 10(d)**, which was measured according to voltage sweeping with a maximum value of 1.2 *k*Ω and a lower value of 0.9 *k*Ω in the negative and positive voltage application respectively. In addition, **Figure 10(e)** confirms that hysteresis takes place in both *I-V* and *C-V* relationships of the device, and it shows a closed switching cycle in the bipolar switching behavior for a maximum value of 25 *m*S.

Memristor behavior for a bipolar switching with forgetting effect is shown in **Figure 11**. An obvious overlap of the *I-V* curve is shown in **Figure 11(b)**, **(c)**, due to the repetitive sweeping of the applied voltage. The sweeping voltage bias approaches a set value v = 1.2 V with a maximum current value I = 6 *m*A. Reversing the voltage polarity, the device switches to a reset value at v = −1.2 V with a maximum current value I = −5 *m*A. Also, it can be seen from these curves, an accumulation of the current on each pulse. The corresponding resistance response is illustrated in **Figure 11(d)**, which was measured according to voltage sweeping with a maximum value of 1.8 *k*Ω decreasing to a lower value of 0.3 *k*Ω in the positive voltage application, on the opposite side of the negative voltage application the resistance response shows an increase from 0.3 to 0.9 *k*Ω. The curve in **Figure 11(e)** shows five switching cycles for a maximum value of 35 *m*S. This *C-V* curve shows that the memristance not only increases and decreases by a different polarity voltage, but it also can spontaneously decrease at the same time, even with no voltage applied, and this is a unique switching behavior of memristor. In fact, these curves show the operation of the model as a bipolar memristor with forgetting effect.

Furthermore, the simulation results for the unipolar behavior of memristor are shown in **Figure 12**, which show that another switching behavior is characterized by the memory devices and also that the memristance of the device can increase and decrease by the same polarity of the voltage. For this type of memristor, we use a positive voltage excitation for a value of 2 V and maximum current value I = 17 *m*A, which is shown in the curve (**Figure 12(a)**), we notice a slight accumulation of the current on each pulse. The characteristics shown in **Figure 12(d)**, **(e)** describe the resistance and the conductance curve of the memristor. The resistance was

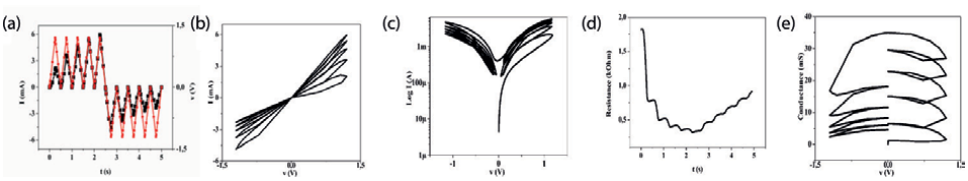

Figure 11.
Memristor SPICE model response to a bipolar with forgetting effect.

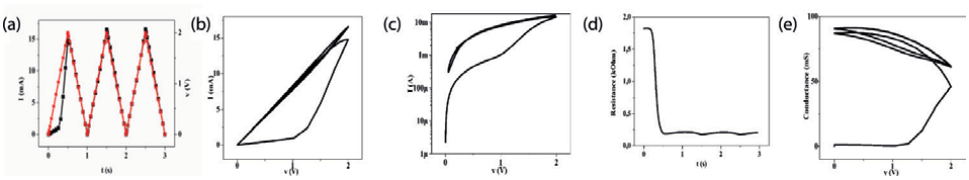

Figure 12.
Memristor SPICE model response to a unipolar behavior switching.

measured with a maximum value of 2.8 *k*Ω decreasing to a lower value of 0.25 *k*Ω. However, the conductance curve (**Figure 12(e)**) shows three switching cycles related to voltage sweeping for a maximum value of 80 *m*S. In fact, this *C-V* curve shows that the conductance change in response to three positive pulses, it initially increases (during each pulse stimulus) and subsequently decays toward its original value (between stimuli).

In the end, we represent the results of memristor under a reversible state between the bipolar and the unipolar behavior in **Figure 13**. The sweeping voltage bias, shown in **Figure 13(a)**, approaches a set value v = 5 V with a maximum current value I = 60 *m*A. Reversing the voltage polarity, the device switches to a reset value at v = −5 V with a maximum current value I = −10 *m*A.

An obvious overlap of the *I-V* curve in **Figure 13(b), (c)** occurs due to the repetitive sweeping of the applied voltage. The corresponding resistance response is illustrated in **Figure 13(d),** which occurs in a different switching behavior; the rise and fall of the resistance exist but with a large gap between high and low values. The conductance curve in **Figure 13(e)** shows four switching cycles for a maximum value of 100 *m*S. This *C-V* curve shows that the first cycle of the switching behavior differs to the other cycles of the switching behavior of the memristor. In fact, the first cycle that can be seen from these curves shows bipolar operation, but after the second pulse, it automatically turned to a unipolar memristor behavior. These characteristic curves are shown, respectively, in **Figures 10–13**. The operation of the memristor model as a bipolar memristor behavior is shown in **Figure 10**. The response to a bipolar with forgetting effect is shown in **Figure 11**. The response to a unipolar memristor behavior is shown in **Figure 12**. And, the memristor model response to a reversible bipolar and unipolar behavior is shown in **Figure 13**. We can conclude that our simulation results are consistent and in very good qualitative agreement with the results already published in [15]. A detailed comparison between our work model and other popular memristor models (the Chua [1], the Strukov (HP) [3], Vourkas [45], and the Chen [15]) is shown in **Table 1**. We can notice that the SPICE model gets a special advantage on describing various

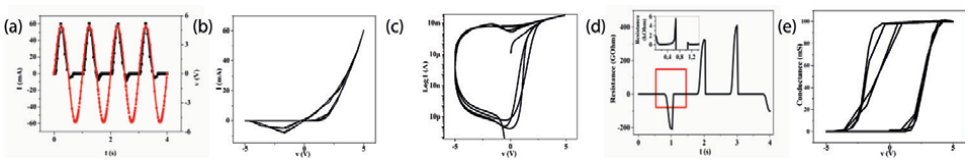

Figure 13.
Memristor SPICE model response to reversible bipolar and unipolar behavior.

Memristor models	Mechanism	High frequency	Low complexity	Unipolar	Bipolar	Forgetting effect	Reversible effect	Parameters
Chua [1]	Yes	No	Yes	No	Yes	No	No	—
Strukov (HP) [3]	Yes	No	Yes	No	Yes	No	No	5
Vourkas [45]	Yes	Yes	Yes	No	Yes	No	No	12
Chen [15]	Yes	Yes	No	Yes	Yes	Yes	Yes	13
This work	Yes	Yes	Yes	Yes	Yes	Yes	Yes	13

Table 1.
Comparing memristor models.

memristors models with an average number of parameters, and for its flexibility, and low complexity.

6. Conclusion

The consideration of the SPICE memristor model as a simple and flexible model was proved to explain the memristor switching, not only processing the general memristor properties, but also catching the different types of memristor behavior: the bipolar, unipolar, the bipolar with forgetting effect, and the reversible process between the bipolar and the unipolar behavior. Our simulation results demonstrate that for the bipolar memristor, a regular hysteresis curve can be obtained. For the bipolar memristor with forgetting effect, an obvious overlap between the neighbor loops of the *I-V* curve, and for the unipolar memristor, a positive voltage is applied, but the conductance will increase only when the voltage is over 1 V. Also, for the reversible process between bipolar and unipolar behavior, the memristor firstly behaves as a bipolar switching, and its conductance increases and decreases according to the polarity of the voltage. However, after applying a second pulse, it will turn to behave as a unipolar switching. This chapter provides a practical memristor model that can be simulated with different types of stimulus, and further studies are aimed at integrating the memristor model into a computing design with complementary metal-oxide-semiconductor (CMOS) circuits that can perform the necessary functions on a chip.

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Section 2

Applications

Chapter 4

Memristive Grid for Maze Solving

Arturo Sarmiento-Reyes and Yojanes Rodríguez Velásquez

Abstract

Memcomputing represents a novel form of neuro-oriented signal processing that uses the memristor as a key element. In this chapter, a memristive grid is developed in order to achieve the specific task of solving mazes. This is done by resorting to the dynamic behavior of the memristance in order to find the shortest path that determines trajectory from entrance to exit. The structure of the maze is mapped onto the memristive grid, which is formed by memristors that are defined by fully analytical charge-controlled functions. The dependance on the electric charge permits to analyze the variation of the branch memristance of the grid as a function of time. As a result of the dynamic behavior of the developed memristor model, the shortest path is formed by those memristive branches exhibiting the fastest memristance change. Special attention is given to achieve a realistic implementation of the fuses of the grid, which are formed by an anti-series connection of memristors and CMOS circuitry. HSPICE is used in combination with MATLAB to establish the simulation flow of the memristive grid. Besides, the memristor model is recast in VERILOG-A, a high-level hardware description language for analog circuits.

Keywords: memristive grids, symbolic memristor modeling, maze-solving, analog processors

1. Introduction

For thousands of years, mazes have intrigued the human mind [1]. The labyrinths have been used in research with laboratory animals, in order to study their ability to recognize their environment [2–4]. In the 1990s, artificial intelligence of robots was studied by examining their ability to traverse unfamiliar mazes [5–7]. Maze exploration algorithms are closely related to graph theory and have been used in both mathematics and computer science [8, 9].

There are several algorithms for maze solving in the literature, they can be classified in two very well-defined groups: the algorithms used by a traveler in the maze without knowledge of a general view of the maze, and the algorithms used for a program that can have a whole view the whole maze. Some examples of the first ones are the wall follower, random mouse, pledge algorithm [10], and Trémaux's algorithm [11]. In the second group, shortest path algorithms are most useful, because they can find the solution not only for a simple connected maze, but also for multiple-solution mazes.

In this chapter, we put a main idea into practice, namely that the topology of a maze can be mapped onto a memristive grid. By exploiting the analog computations performed by solving Kirchoft's Current Laws (KCL) in a parallel manner, memristive grids have demonstrated their ability for computing shortest paths in a

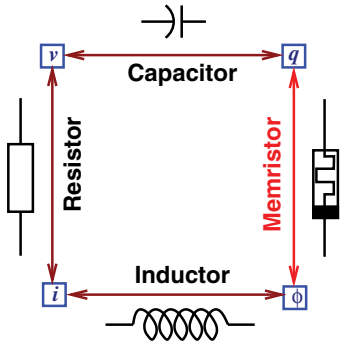

Figure 1.
Basic circuit elements.

given maze, levering on the dynamic adjustment of their intrinsic memristance [12, 13].

The parallel solution of KCL introduces a resemblance of the memristive grid as an analog processor [14] in counterposition to a digital approach in which the processing can also be done in parallel way, but the overhead in additional conversion circuitry is too high.

Two important milestones appear in the history of the memristor. The first one in 1971 when professor Leon O. Chua introduced the memristor as the fourth basic circuit element in his seminal paper [15]. It established that the memristor completes the number of possible relationships between the four fundamental circuit variables: current, voltage, magnetic flux, and electric charge—as depicted in **Figure 1**. Later, an extension to memristive systems was published in [16].

The second milestone occurred in 2008, when a team at Hewlett-Packard Laboratories fabricated a device whose behavior exhibited the memristance phenomenon [17]. Since the advent of the memristor as an actual device, research and technological development in several areas related to memristive applications have been increased.

In the field of signal processing, the memristor has special preponderance in neuro-computing and artificial neural networks because it allows new architectures and processing paradigms with important features based on biological neuronal systems [18–22]. In summary, a novel form of neuro-computing is on scene, namely memcomputing [23].

Memristive grids represent a family of neuro-computing systems that are able of achieving in a very flexible way several tasks for analog applications. In the next paragraphs, we present a specially tailored memristive grid that is focused on solving mazes.

The rest of the manuscript is organized as follows: in Section 2, the developed models are recast in a set of fully analytical expressions for the memristance, which are given as charge-controlled functions that are further used in this application. The components of the memristive grid are introduced in Section 3. The maze-solving procedure is introduced in Section 4 by explaining the simulation flow of the memristive grid. Subsequently, several mazes are solved in order to illustrate the operation of the memristive grid in Section 6. Finally, a series of conclusions is drawn.

2. Development of a charge-controlled memristor model

In this section, a charge-controlled memristor model is introduced. The model has been developed by solving the ordinary differential equation (ODE) that

describes the nonlinear drift mechanism, with a homotopy perturbation method that yields an analytical expression for the memristance [24–27].

In order to obtain a charge-dependent memristance model, the nonlinear drift differential equation is expressed in terms of the electric charge:

$$\frac{dx(q)}{dq} = \eta \kappa f_w(x(q)) \tag{1}$$

where η defines the direction of the drift and it can be ± 1. Besides, f_w is the window function used to define the nonlinear and bounded behavior of the state variable $x(q)$, and it is given as [28]:

$$f_w = 1 - (2x - 1)^{2k} \tag{2}$$

Figure 2 shows the resulting window plots for various values of k. In addition, κ is given as:

$$\kappa = \frac{\mu R_{on}}{\Delta^2} \tag{3}$$

where μ, R_{on}, and Δ are the mobility, the ON-state resistance, and the dimension of the device.

The main goal is to obtain a solution to Eq. (1) in the form of an analytical expression x(q). Once, this is done, this solution is substituted into the coupled resistor equivalent of **Figure 3** which is expressed as [17]:

$$M(t) = R_{on}x(q) + R_{off}[1 - x(q)] \tag{4}$$

where $M(t)$ is the total memristance. Besides, R_{on} and R_{off} are the on-state and the off-state resistances respectively.

In order to obtain an analytical solution to Eq. (1), we resort to the methodology reported in [24, 29], which is based on the homotopy perturbation method (HPM). HPM finds $x(q)$ for a given order of the homotopy method as well as the integer value of exponent of the window function (k). Furthermore, it should be also pointed out that the charge may be positive or negative.

As a result, the sign of the charge as well as the direction of the drift (η) allows us to introduce two operators that are used to simplify the final expressions for the solution. These operators are denoted as Λ and Θ. **Table 1** shows how they are defined depending on the signs of the charge and η.

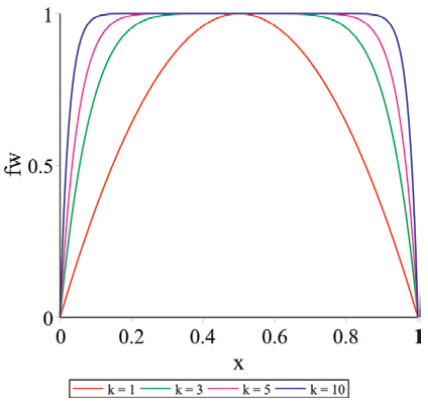

Figure 2.
Window function for different values of k.

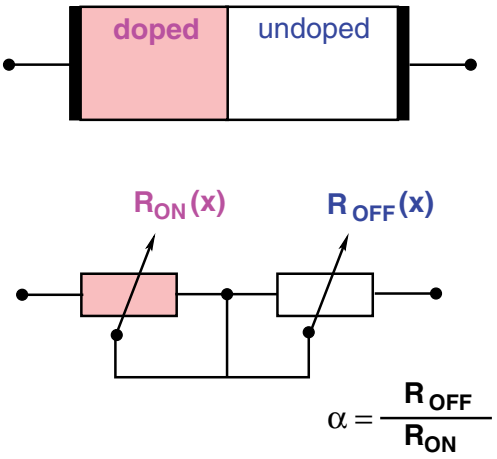

Figure 3.
Coupled series equivalent of the memristor.

	$q \geq 0$	$q < 0$
η^+	$\Lambda = -1$ $\Theta = 1$	$\Lambda = 1$ $\Theta = 0$
η^-	$\Lambda = -1$ $\Theta = 0$	$\Lambda = 1$ $\Theta = 1$

Table 1.
Operators for the signs of η and q.

As a matter of an example, the expression of $x(q)$ for order-1 with $k = 1$ is given as:

$$X_{O1K1}(q) = \Theta\left[1 + (X_0 - 1)^2 e^{8\Lambda\kappa q} - (X_0 - 1)(X_0 - 2)e^{4\Lambda\kappa q}\right] + (1 - \Theta)X_0\left[-X_0 e^{8\Lambda\kappa q} + (X_0 + 1)e^{4\Lambda\kappa q}\right] \tag{5}$$

After substituting Eq. (5) in Eq. (4), it results in the memristance expression:

$$\begin{aligned} M_{O1K1} = {} & \Theta\left[R_d(Xo - 1)\left[(X_0 - 2)e^{\Lambda 4\kappa q} - (Xo - 1)e^{\Lambda 8\kappa q}\right] + R_{ON}\right] \\ & + (1 - \Theta)\left[R_d X_0\left[X_0 e^{\Lambda 8\kappa q} - (X_0 + 1)e^{\Lambda 4\kappa q}\right] + R_{off}\right] \end{aligned} \tag{6}$$

where the variable R_d is given as:

$$R_d = R_{off} - R_{on} \tag{7}$$

For order-2 and $k = 1$, the solution to Eq. (1) is given as:

$$\begin{aligned} X_{O2K1}(q) = {} & \Theta\left[1 + (X_0 - 1)(X_0^2 - 3X_0 + 3)e^{4\Lambda\kappa q} - (X_0 - 1)^2(2X_0 - 3)e^{8\Lambda\kappa q} + (X_0 - 1)^3 e^{12\Lambda\kappa q}\right] \\ & + (1 - \Theta)\left[X_0(X_0^2 + X_0 + 1)e^{4\Lambda\kappa q} - X_0^2(2X_0 + 1)e^{8\Lambda\kappa q} + X_0^3 e^{12\Lambda\kappa q}\right] \end{aligned} \tag{8}$$

Again, after substituting the expression above in Eq. (4) and after some reductions, it is possible to obtain the memristance for order-2 and $k = 1$ as:

$$\begin{aligned} M_{O2K1} = {} & M_{O1K1} + Rd\left[\Theta(Xo - 1)^3(-e^{\Lambda 4\kappa q} - 2e^{\Lambda 8\kappa q} - e^{\Lambda 12\kappa q})\right. \\ & \left. + X_0^3(-e^{\Lambda 12\kappa q} - 2e^{\Lambda 8\kappa q} - e^{\Lambda 4\kappa q})(1 - \Theta)\right] \end{aligned} \tag{9}$$

In a similar way, an expression for the memristance for order-3 and $k = 1$ can be obtained:

$$\begin{aligned} M_{O3K1} = M_{O2K1} + Rd\Big[&\Theta(Xo-1)^4\left(-e^{\Lambda 4\kappa q} - 3e^{\Lambda 8\kappa q} - 3e^{\Lambda 12\kappa q} - e^{\Lambda 16\kappa q}\right) \\ &+X_0^4\left(-e^{\Lambda 16\kappa q} - 3e^{\Lambda 12\kappa q} - 3e^{\Lambda 8\kappa q} - e^{\Lambda 4\kappa q}\right)(1-\Theta)\Big] \end{aligned} \tag{10}$$

It can be noticed that HPM produces nested expressions of the memristance, that is to say, a given memristance of a given order is expressed as function of the memristance of lower orders.

For order-1 and $k = 2$, the memristance is given as follows:

$$\begin{aligned} M_{O1K2} = R_d\Theta&\left[\begin{array}{c} \frac{4}{3}\left(X_0^2+1\right)\left(X_0^2-2X_0+2\right)e^{8\Lambda\kappa q} - 3\left(2X_0^2-2X_0+1\right)e^{16\Lambda\kappa q} \\ +2\left(3X_0^2-3X_0+1\right)e^{24\Lambda\kappa q} - \left(\frac{4}{3}X_0^4 - \frac{8}{3}X_0^3 + 4X_0^2 - \frac{8}{3}X_0 + \frac{2}{3}\right)e^{32\Lambda\kappa q} - 1 \end{array}\right] \\ + R_d&\left[\begin{array}{c} -\frac{1}{3}X_0\left(2X_0^3 - 6X_0^2 + 9X_0 + 3\right)e^{8\Lambda\kappa q} \\ +3X_0^2e^{16\Lambda\kappa q} - 2X_0^3e^{24\Lambda\kappa q} + \frac{2}{3}X_0^4e^{32\Lambda\kappa q} \end{array}\right] + R_{off} \end{aligned} \tag{11}$$

In a similar way, the memristance for order-2 and $k = 2$ is given:

$$\begin{aligned} M_{O2K2} = M_{O1K2} + R_d&\left[\begin{array}{c} \Theta\left(\begin{array}{c} \mathcal{P}_1e^{8\Lambda\kappa q} + \mathcal{P}_2e^{16\Lambda\kappa q} + \mathcal{P}_3e^{24\Lambda\kappa q} + \mathcal{P}_4e^{32\Lambda\kappa q} \\ +\mathcal{P}_5e^{40\Lambda\kappa q} + \mathcal{P}_6e^{48\Lambda\kappa q} + \mathcal{P}_7e^{56\Lambda\kappa q} \end{array}\right) \\ -\frac{1}{45}X_0^3\mathcal{P}_8e^{8\Lambda\kappa q} + 2X_0^3\mathcal{P}_9e^{16\Lambda\kappa q} - X_0^3\mathcal{P}_{10}e^{24\Lambda\kappa q} \\ +\frac{8}{9}X_0^4\mathcal{P}_{11}e^{32\Lambda\kappa q} - 13X_0^5e^{40\Lambda\kappa q} + \frac{24}{5}e^{48\Lambda\kappa q} - \frac{8}{9}e^{56\Lambda\kappa q} \end{array}\right] \\ \mathcal{P}_1 &= -\frac{128}{45}X_0^6 + \frac{128}{15}X_0^5 - \frac{89}{9}X_0^4 + \frac{50}{9}X_0^3 + \frac{11}{3}X_0^2 - \frac{226}{45}X_0 + \frac{106}{45} \\ \mathcal{P}_2 &= 4X_0^4 - 8X_0^3 - 22X_0^2 + 26X_0 - 10 \\ \mathcal{P}_3 &= 8X_0^6 - 24X_0^5 + 36X_0^4 - 32X_0^3 + 75X_0^2 - 63X_0 + 19 \\ \mathcal{P}_4 &= -\frac{16}{9}X_0^6 + \frac{16}{3}X_0^5 - \frac{488}{9}X_0^4 + \frac{896}{9}X_0^3 - \frac{400}{3}X_0^2 + \frac{760}{9}X_0 - \frac{184}{9} \\ \mathcal{P}_5 &= 65X_0^4 - 130X_0^3 + 130X_0^2 - 65X_0 + 13 \\ \mathcal{P}_6 &= \left(2X_0^2 - 2X_0 + 1\right)\left(X_0^4 - 2X_0^3 + 5X_0^2 - 4X_0 + 1\right) \\ \mathcal{P}_7 &= \frac{56}{9}X_0^6 - \frac{56}{3}X_0^5 + \frac{280}{9}X_0^4 - \frac{280}{9}X_0^3 + \frac{56}{3}X_0^2 - \frac{56}{9}X_0 + \frac{8}{9} \\ \mathcal{P}_8 &= 40X_0^4 - 204X_0^3 + 495X_0^2 - 630X_0 + 405 \\ \mathcal{P}_9 &= 2X_0^2 - 6X_0 + 9 \\ \mathcal{P}_{10} &= 4X_0^3 - 12X_0^2 + 18X_0 + 9 \\ \mathcal{P}_{11} &= 2X_0^3 - 6X_0^2 + 9X_0 + 18 \end{aligned} \tag{12}$$

Eqs. (6), (9)–(12) are indeed the analytical expressions that constitute memristor models. References [29, 30] contain a proper characterization of the resulting models.

3. Implementing the memristive grid

A memristive grid is a rectangular array of memristive branches, as shown in **Figure 4**. Herein, the memristive branches have been denoted as *bricked* circuit elements called memristive fuses. In addition, a memristive fuse is composed of a series connection of two memristors in anti-series and a switching device [14].

The switch is used to define the structure of the labyrinth, if the switch is in the ON-state, then the way is free, while if the switch is in the OFF-state then a wall is encountered. **Figure 5** shows the equivalent of the memristive fuse.

In order to illustrate the use of the memristive grid in describing a maze, the maze of **Figure 6a** is used. The entrance of the maze is marked by the green arrow and the output is marked by a red arrow, and the walls are shown in red. The maze is mapped onto the memristive grid as shown in **Figure 6b** by denoting the entrance of the maze as a voltage source, while the output of the maze is given by the ground node. For sake of clarity, both figures are merged into **Figure 6c**, where

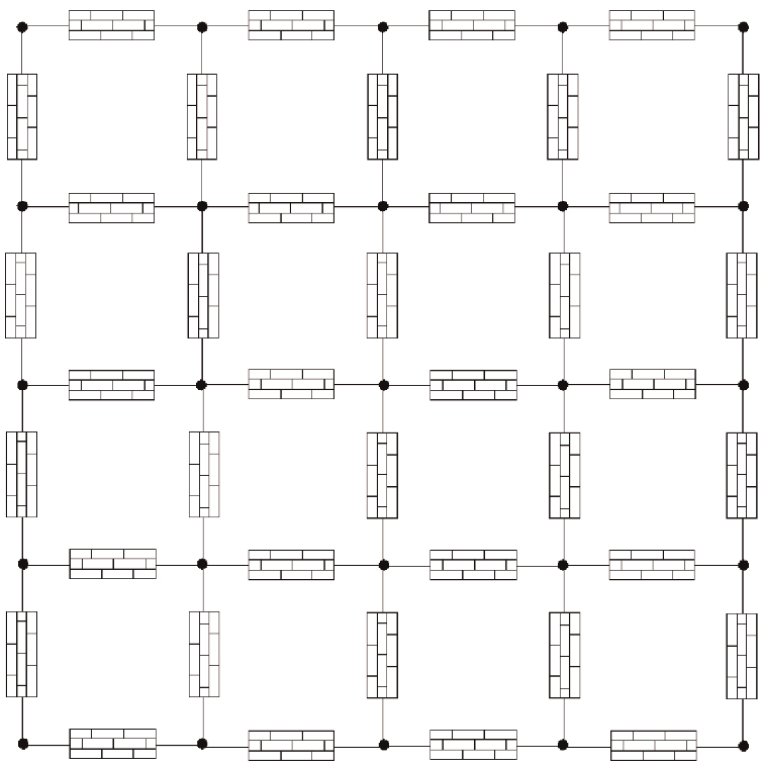

Figure 4.
Description of the memristive grid.

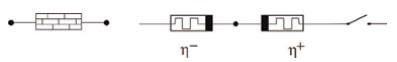

Figure 5.
Configuration of the memristive fuse for maze solving.

the blocked paths are represented by memristive fuses in red, on the contrary, the paths that can be followed are represented by memristive fuses in white. It clearly results that the walls should be given by memristive fuses with the switch in the OFF-state (high-resistance), while the open paths are constituted by memristive fuses with the switch in the ON-state (low-resistance).

On the top of this, the memristive grid can be straightforwardly adapted to other kinds of mazes. Mazes with multiple entrances are represented with multiple input voltages. Similarly, mazes with multiple outputs are given by setting multiple instances of the ground node.

3.1 An algorithmic view

A close look of the solution path in **Figure 6a** can lead us to a graph-theoretical explanation on how the memristive grid solves the maze, because the open ways in the maze can be regarded as an unweighted graph where the solution path is subgraph. The solution path can be found by using a *breath-first-search* (BFS) algorithm in order to traverse the graph which yields indeed the shortest-path because we deal with an unweighted graph [31].

The application of BFS is illustrated by determining the shortest path between nodes 3 and 6 of the graph from **Figure 7a**. Here, node 3 can be regarded as the input (i) and node 6 as the output (o). The algorithm starts by selecting the initial node (3). From this, a first level of coloring is achieved by selecting the neighboring nodes (2, 4, 5). This procedure is repeated until all nodes have been visited. For this graph, it suffices with 2 levels. The shortest path is defined by the sequence 3→5→6, which is shown in red in **Figure 7b**.

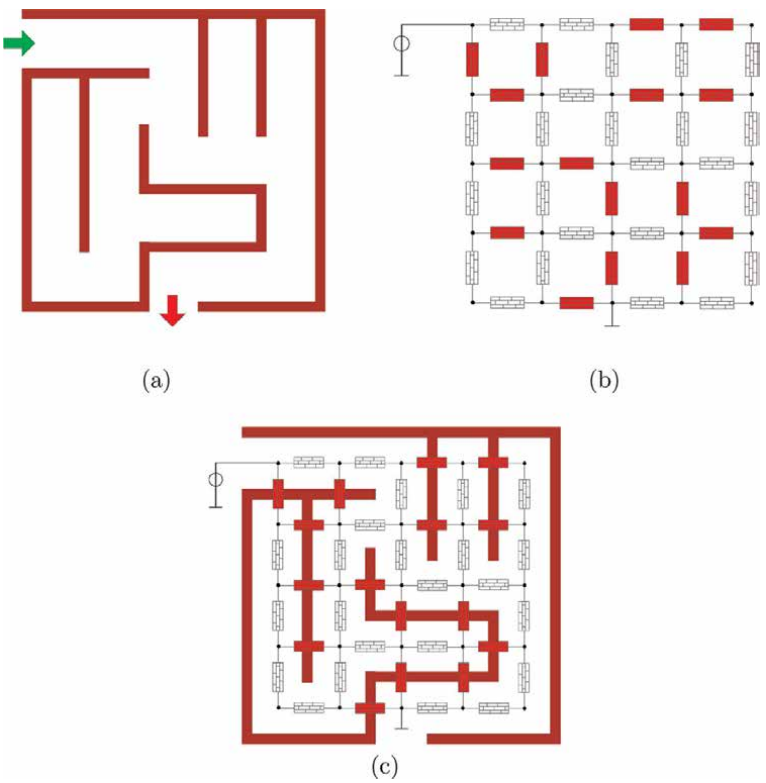

Figure 6.
Mapping the maze onto the memristive grid. (a) Maze, (b) Grid and (c) Merging the maze and the grid.

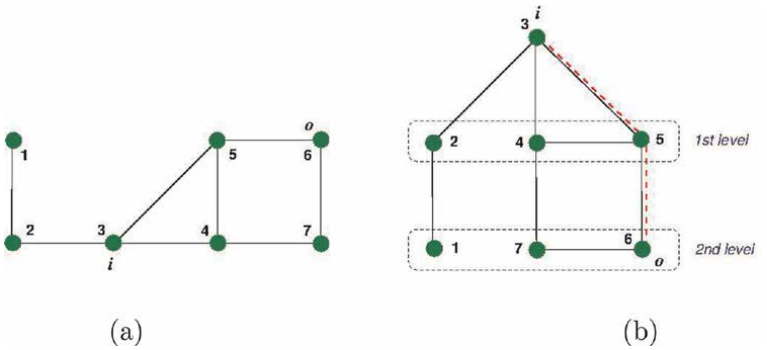

Figure 7.
BFS algorithm to obtain the shortest path. (a) A graph and (b) The BFS algorithm.

As a result, by representing the graph with the memristive grid, it allows us to define ways for the current to flow through the open paths by gradually changing the equivalent memristance of the fuse. Besides, what is more relevant, since the current is given as the time-derivative of the charge, then the solution of the maze is always given by the shortest path to ground which represents the path with the fastest changing memristance.

3.2 Technical specifications of the memristive fuse

The memristive fuse from **Figure 5** contains a pair of memristors in anti-series connection. Such a memristor connection produces an M-q characteristic that is composed of the overlapping of the M-q curves of the memristor expressions for η^- and η^+. **Figure 8a** shows the M-q characteristics for the model of order-1, $k = 5$ and **Figure 8b** shows the schematic curve with the values of R_{off} and R_{init}. Physical parameters of the memristor model are given by the nominal values of the HP memristor. A summary of the specs for the memristor model is given in **Table 2**.

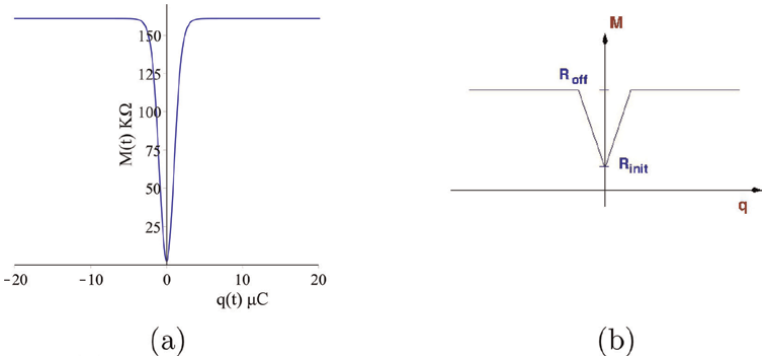

Figure 8.
Memristance-charge characteristic of the anti-series connection. (a) M_{O1K5} and (b) M-q.

$\mu_v \left[\frac{m^2}{Vs}\right]$	Δ $[nm]$	R_{on} $[\Omega]$	R_{off} $[\Omega]$	R_{init} $[\Omega]$	k	Order
1×10^{-14}	10	100	16×10^3	1×10^3	5	1

Table 2.
Memristor parameters of the anti-series connection.

It clearly results that the overall performance of the grid in solving mazes is based on the model of the memristors that form the fuses. Even though the models are recast in fully symbolic form—which represent a great advantage, numeric values should be assigned to the parameters of the model, as given in **Table 2**. Since variations of the model parameters may appear, it is important to notice that the anti-series connection alleviates the possible effects of those variations. Specific sensitivity analysis on the parameter variations of the charge-controlled models are given in [30].

3.2.1 Switch implementation

In the memristive fuse, an ideal switch can be used in the process of finding the solution, however, with the aim to have a more realistic switch, a transmission gate is used instead. The transmission gate is a switch in CMOS technology, it consists of an NMOS transistor and a PMOS transistor connected in parallel, as in **Figure 9a**. Both devices in combination can fully transmit any signal value between V_{dd} (the supply voltage of the transistors) and ground. In order to switch, each transistor requires a complementary control input. Therefore, it is necessary to add an inverter connected between the control input and the PMOS gate [30, 32].

If the control input is V_{dd} then the switch is closed, and as a result, the transmission gate can pass the input signal to output because it exhibits a low-resistance. On the contrary, if the control input is grounded, then the switch is opened and the transmission gate presents a high-resistance.

In order to simulate the transmission gate of the memristive fuse, a CMOS 180 nm technology is used. The parameters of the two complementary transistors are shown in **Table 3**. The equivalent resistance of the transmission gate both states as a function of the input voltage is shown in **Figure 10**.

The resistance values are extracted making a sweep of the input voltage and measure the equivalent average resistance of the transistors in the ON-state

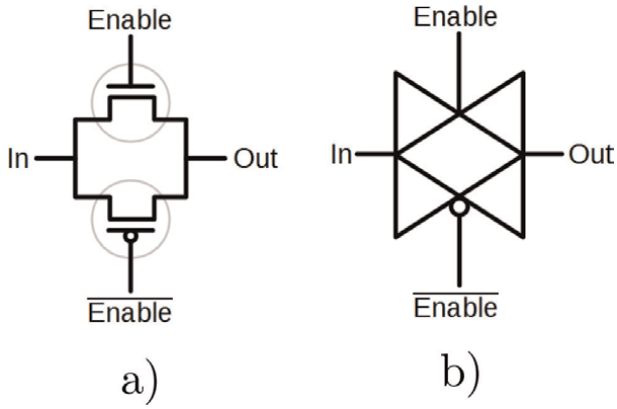

Figure 9.
Transmission gate. (a) Configuration and (b) symbol.

CMOS TG	W μm	L μm
PMOS	1.44	0.18
NMOS	0.48	0.18

Table 3.
Transmission gate: transistor parameters.

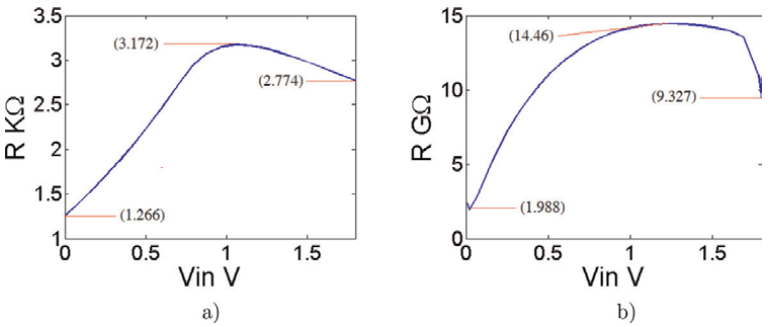

Figure 10.
Resistance characteristic of the transmission gate for both states. (a) ON-state and (b) OFF-state.

$R_{TG_{on}}$ Ω	$R_{TG_{off}}$ Ω
2.504×10^3	10.854×10^9

Table 4.
Selected values for $R_{TG_{on}}$ and $R_{TG_{off}}$.

(switch closed, **Figure 10a**) and OFF-state (switch opened, **Figure 10b**). **Table 4** shows the selected values for $R_{TG_{on}}$ and $R_{TG_{off}}$.

In addition, it can be noticed that the initial value of the ON-state resistance is given as:

$$R_{TG_{init}} = R_{TG_{on}}|_{Vin=0} = 1.266 \tag{13}$$

As a result of the specifications above, a couple of parameters are of special interest, namely, the initial resistance and the maximum resistance of the memristive fuses. At the start, the fuses present an initial resistance which is given as the sum of the initial resistance of the memristors in the anti-series connection plus initial resistance of the ON-state of the transmission gate:

$$R_{fuse_{init}} = 2R_{init} + R_{TG_{init}} \tag{14}$$

which is 3.266 kΩ.

Moreover, the maximum resistance of the fuse is given as:

$$R_{fuse_{max}} = R_{off_1} + R_{on_2} + R_{TG_{on}} \tag{15}$$

It is worthy to notice that the maximum fuse resistance does not contain R_{off} of both memristor, but R_{off} of one memristor and R_{on} of the other memristor due to the anti-series connection.

4. Simulation flow

Since the solution path for a given maze is obtained by determining the path where the fastest change in resistance occurs, the core of the solution process involves a transient analysis. We have chosen to achieve the electrical simulation of the memristive grid by using HSPICE. Both memristors of the fuse are defined as nonlinear resistors in the input netlist.

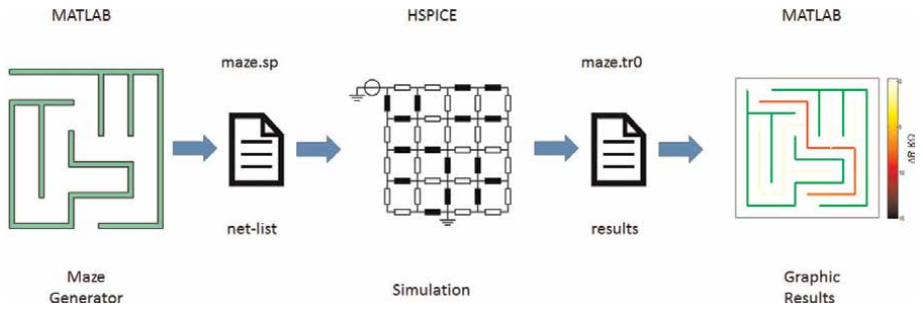

Figure 11.
Simulation flow.

The simulation flow is shown in **Figure 11** and is described as follows:

Maze generator: The first stage in the solution process is to generate the maze by using a script in MATLAB that generates the maze and it is shown as a plot. The walls of the maze are shown in green color in the resulting plot. From this graphical description, the maze can be automatically mapped onto the memristive grid and an input file for HSPICE is generated. The inputs in the maze are represented by input voltage sources of 1 V and the exits are connected to ground.

Electric simulation: The netlist obtained by the maze generator is simulated with HSPICE. Here, a transient analysis for 20 s is carried out, this time is enough to find the solutions of the mazes under-test, however, the exact time when the solutions are found depends on the maze dimensions (grid). The transient simulation results are saved in a .tr0 output file.

Graphic display of the results: In order to visualize the results, a script in MATLAB imports the output simulation signals obtained with HSPICE. The resistance dynamic change ($\Delta R(t)$) is calculated at each simulation time and then the paths of the maze are represented by a graph, where the color in each branch indicates the level of $\Delta R(t)$ at a given time. For sake of readiness, we have selected white for the minimum change and black for the maximum change.

During the transient simulation, the equivalent resistance of the fuses is obtained at every instant t. It clearly results that ΔR is obtained by calculating the difference between the measured resistance and the minimum resistance from Eq. (14):

$$\Delta R(t) = R(t) - R_{fuse_{init}} \tag{16}$$

Consequently, the fuses that first reach the highest ΔR define indeed the solution path of the maze. In mazes with multiple solutions, fuses that belong to the shortest path reach high values of ΔR more fastly. As time lapses, other solution paths are revealed reaching high values of ΔR. For a given time, all fuses within the solution paths reach the maximum ΔR, which is given by

$$\max(\Delta R(t)) = R(t) - R_{fuse_{max}} \tag{17}$$

5. Mazes under-test

In order to prove the behavior of the memristive grid in maze solving, this section presents several cases that have been ordered as follows:

- Mazes with a single solution
- Mazes with multiple solutions

- Maze with two inputs and two outputs
- An octogonal maze with three inputs and a single output
- A 3D maze

5.1 Single-solution mazes

The first set to be solved consists of three mazes with a single-entrance and single-output and the solution is given by a unique path.

5.1.1 The 5 × 5 maze

The first maze, from **Figure 12a**, is treated in full with the aim of highlighting the details of the solution procedure. The first stage of the procedure yields the memristive grid associated to the mapping of the maze, which is shown in **Figure 12b**. The resulting netlist of the memristive grid is then simulated in a transient analysis with HSPICE.

It can be noticed that there are 24 memristive fuses in the open paths of the maze. The electrical simulation is applied in order to measure the instantaneous resistance of the fuses. On the one hand, **Figure 13a** shows the transient behavior of the resistance of those fuses for the first $\frac{1}{5}$s. It can be noticed that all fuses start with the same resistance at $t = 0$, namely $R_{fuse_{init}}$. As a result, at $t = 0$, $\Delta R = 0$ for all fuses and the maze is not walked yet and the output display shows the open paths in white color, as shown in **Figure 13b**.

As time lapses, at $t = 0.197$s, only the fuses belonging to the solution path exhibit significant changes in their resistance. Here, the blue lines correspond to fuses outside the solution path, while the red lines correspond to fuses that belong to solution path. These changes are represented in the output display of **Figure 13c** for the same time in yellow. The solution path can already be distinguished.

On the other hand, **Figure 14a** shows $R(t)$ of the memristive fuses for $0 < t < 20$s. The red lines show that the fuses belonging to the solution path reached a maximum, while the blue lines remain in low levels of resistance, i.e., they belong to paths that finish in dead-ends.

Within this time-window, two snapshots of the output display have been taken at $t = 1.3929$s and $t = 3.7886$s—as depicted in the plots of **Figure 14b** and **c**, respectively. In the first display, the solution path is already highlighted in red with

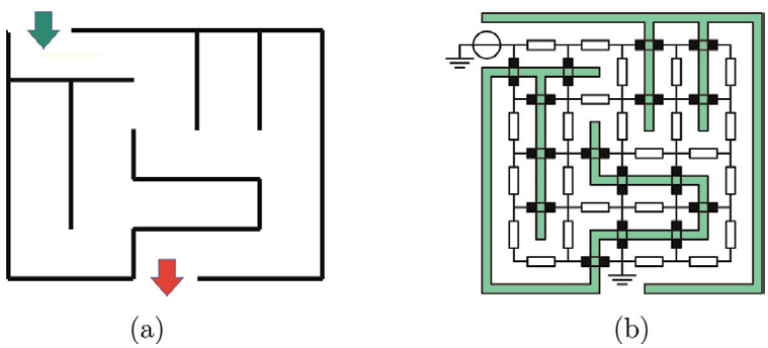

Figure 12.
Mapping the 5 × 5 single-solution maze onto the memristive grid. (a) A 5 × 5 maze and (b) associated memristive grid.

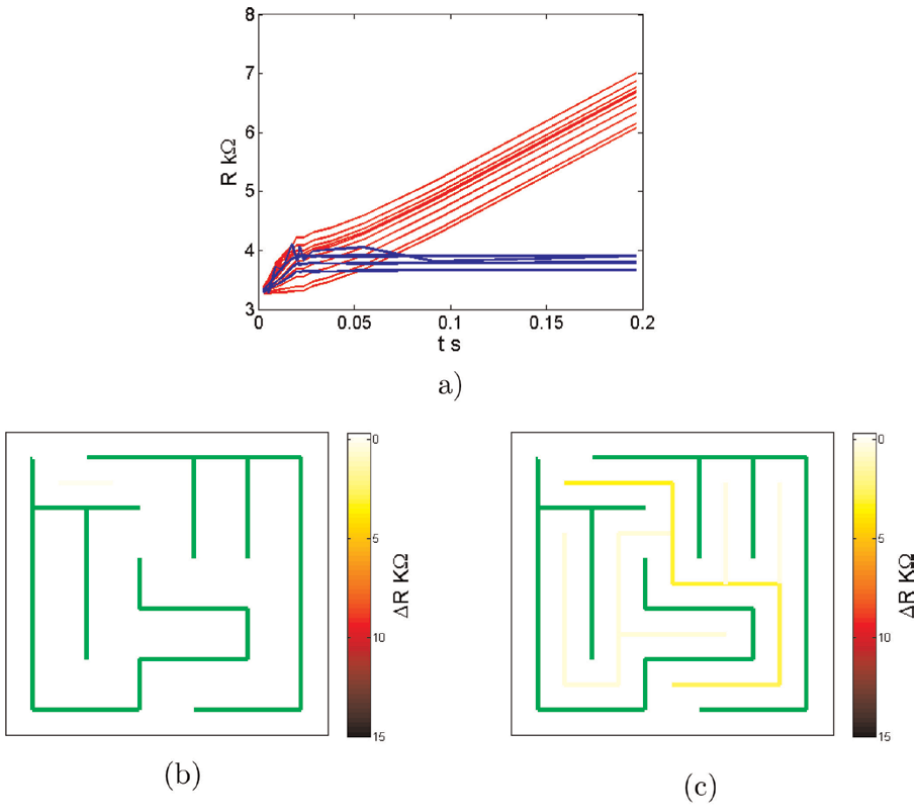

Figure 13.
Transient analysis of the maze in ***Figure 12*** *for small values of t. (a) R(t) of the fuses for* $0 < t < 0.197s$*, (b)* $t = 0$ *s, and (c)* $t = 0.197$ *s.*

fuses having a value of $\Delta R \approx 8.0k\Omega$. At $t = 3.7886$s, the fuses of the solution path show $\Delta R = 15.0k\Omega$.

In summary, it can be concluded that the memristive grid achieves the solution of the maze in a parallel processing by calculating the resistance of the fuses simultaneously. The progress of the solution procedure can be regarded as tracking the dynamic behavior of ΔR, which directly points out the solution path of the maze. On top of this, the output display allows us to visualize this procedure with the help of a color scale.

5.1.2 The 10×10 *and* 15×15 *mazes*

The memristive grid has also been applied to single-solution mazes that have larger sizes. The first maze is of 10×10 dimension and it is depicted in **Figure 15a** showing these mazes.

The second case is a 15×15 maze, which is shown altogether with its solution in **Figure 16**.

5.2 Multiple solutions mazes

The second set to be solved consists of three mazes that have solutions with multiple paths.

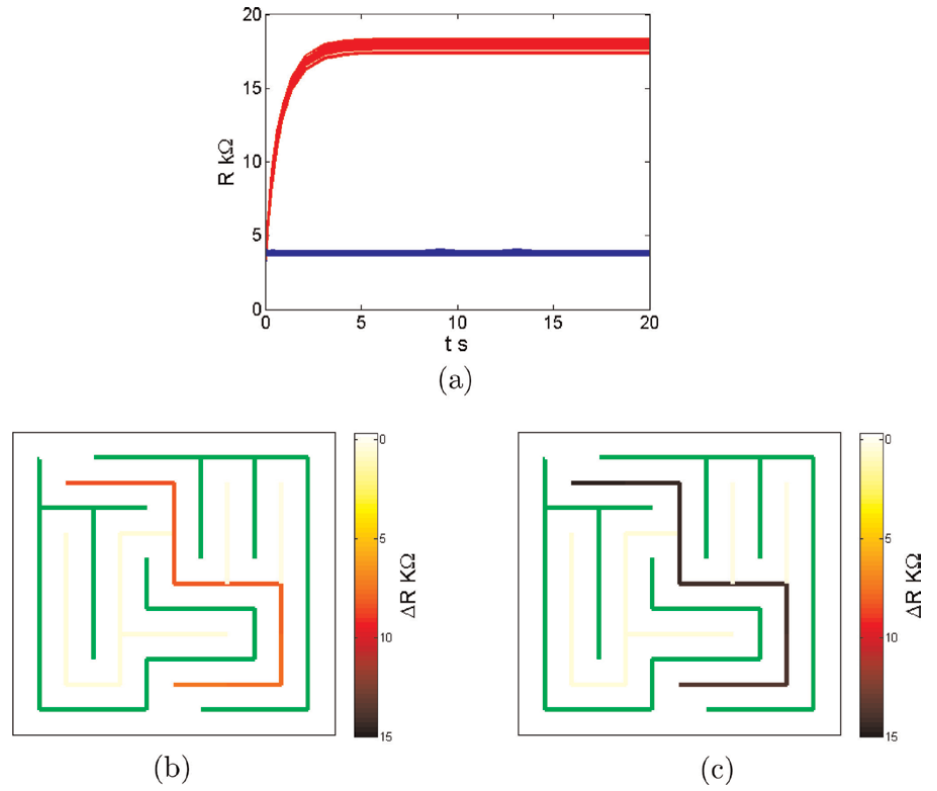

Figure 14.
Transient analysis of the maze in ***Figure 12*** *for larger values of t. (a) $R(t)$ of the fuses for $0 < t < 20$s, (b) $t = 1.3929$ s, and (c) $t = 3.7886$ s.*

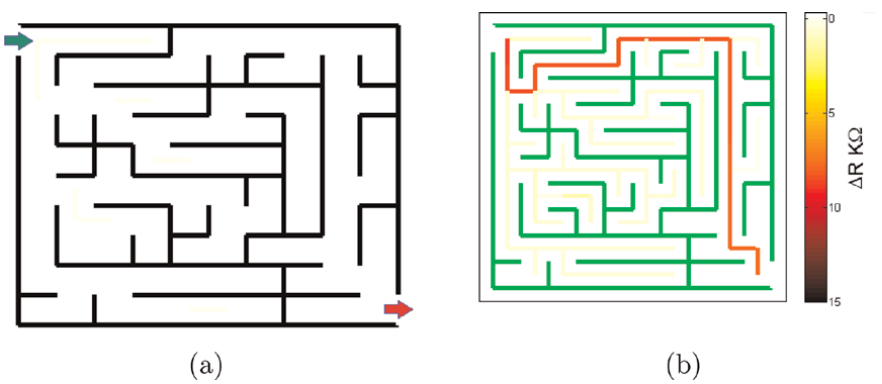

Figure 15.
10×10 *maze and solution at* $t = 1.3929$*s.*

5.2.1 The 5×5 maze with multiple solutions

This maze is shown in **Figure 17**. It is a very simple example that is explained to some extent in order to illustrate the procedure for finding the paths that constitute the solutions.

After carrying out the transient simulation, the resistance of the memristive fuses is obtained. **Figure 18a** shows $R(t)$ for $0 < t < 0.65$s. Herein, the attention is focused only on the resistance of the fuses belonging to the solution paths.

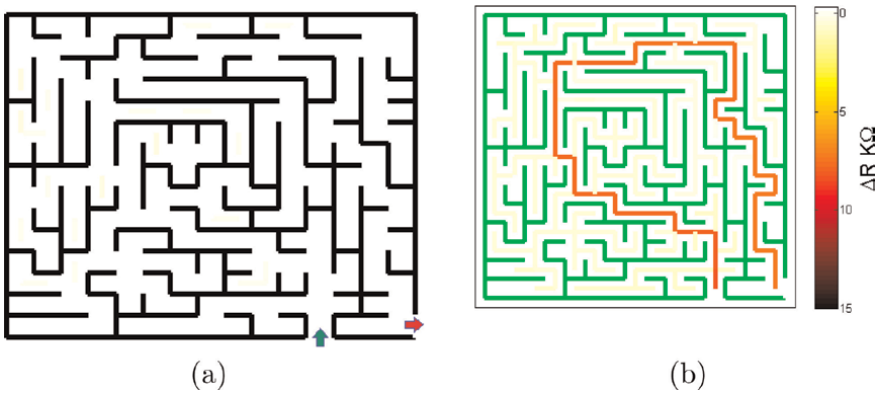

Figure 16.
15×15 *maze and solution at* $t = 3.7886s$.

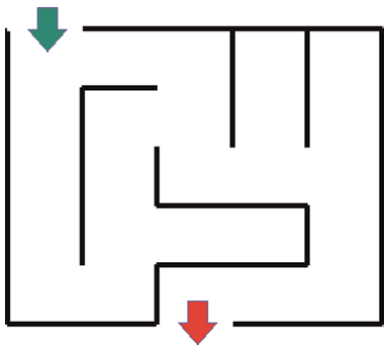

Figure 17.
A 5×5 *double-solution maze.*

Furthermore, the red lines show a steepest behavior which is a result that the red lines are associated to the fuses belonging to the solution with the shortest path. Besides, the blue lines are associated to fuses for the second solution path.

It can be observed that all paths start from $R_{fuse_{init}}$ when $t = 0$, i.e., the maze has not yet been walked—as given in the display of **Figure 18b**. After 0.2204 s, both solutions paths are already distinguishable, but the shortest path exhibits higher ΔR, which denoted by the darkest yellow tones in **Figure 18c**. After a while, at $t = 0.638$, the solution given by the shortest path is perfectly differentiable from the other solution, which can be compared by using the color bar.

After a larger sweep of time, the resistances of the fuses for both solutions have coalesced into an asymptotic level, which is the maximum value of the resistance at $t = 20$s—as shown in **Figure 19**.

5.2.2 Other mazes with multiple solutions

In this paragraph, two case studies are presented. The first one is the maze shown in **Figure 20a**, which is a 10×10 maze that has a single entrance and a single exit, but there are four possible solution paths.

A snapshot at 1.901 s has been taken—see **Figure 20b**. The four solution paths are visible in different colors. The shortest path is shown in red exhibiting the highest ΔR at the time of evaluation. On the opposite, the solution with the longest path is given in pale yellow. This example shows the usefulness of the color palette

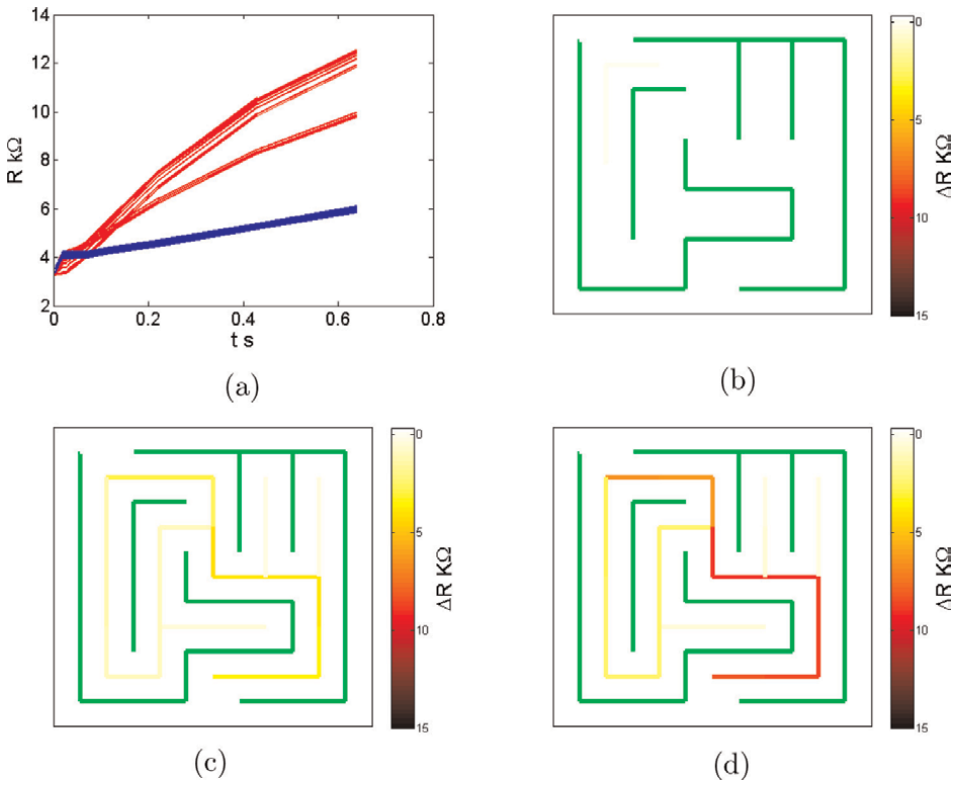

Figure 18.
Progress of the solution search for small t for the maze in ***Figure 17****. (a) $R(t)$ for $0 < t < 0.65s$, (b) $t = 0s$, (c) $t = 0.2204s$, and (d) $t = 0.638$ s.*

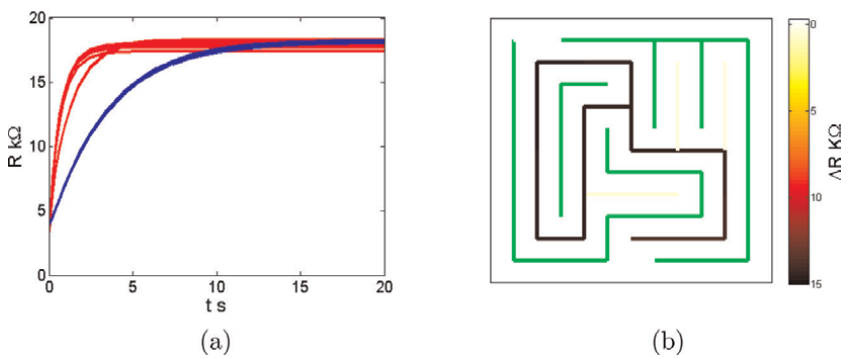

Figure 19.
Transient analysis for larger values of t. (a) $R(t)$ and (b) display at $t = 20s$.

of the output display on its full extent, because all possible solution paths are visible and it gives more insight on the progress of the solution procedure. After a long time, all the solutions reach the same resistance value as shown in **Figure 20c**.

The second example of this paragraph is a maze with two entrances and two exits that is shown in **Figure 21a**. We show in **Figure 21b** a snapshot taken at 1.0276 s. At this point, the memristive grid has been able to find both shortest paths for the solutions between the entrances and the outputs. After a while, at $t = 8.0716s$, the output display shows the connection between both paths—as given in **Figure 21c**.

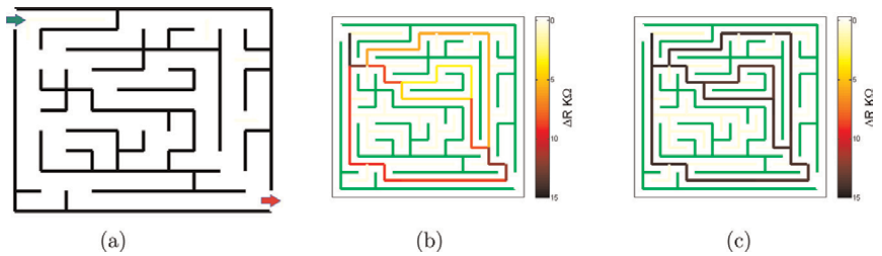

Figure 20.
Multiple-solution maze with one entrance and one exit. (a) Maze, (b) $t = 1.901s$, and (c) $t = 20s$.

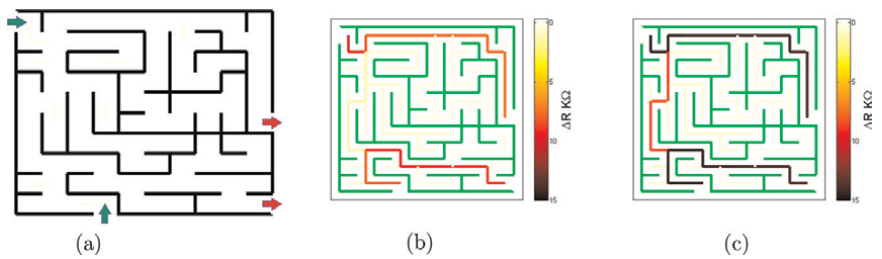

Figure 21.
Multiple-solution maze with two entrances and one exits. (a) Maze, (b) $t = 1.0276s$, and (c) $t = 8.0716s$.

5.3 Octogonal maze

A nonrectangular maze is given in **Figure 22a**, which is an octogonal concentric maze with three entrances and with the output goal in the center of the maze. The three entrances are denoted as **S**, **E**, and **NW**. Entrances **E** and **NW** cannot reach the solution, while entrance **S** does. Given the impossibility of the output display for dealing with nonrectangular mazes, the octogonal maze is converted into an isomorphic view that is given in **Figure 22b** that shows the solution path in red.

5.4 A 3D maze

In order to illustrate that the memristive grid is able to deal with a three-dimensional maze, a three-layer maze is solved. For sake of readiness, **Figure 23** shows the maze in separated levels in a puzzle-fashion. The ball on the top-layer

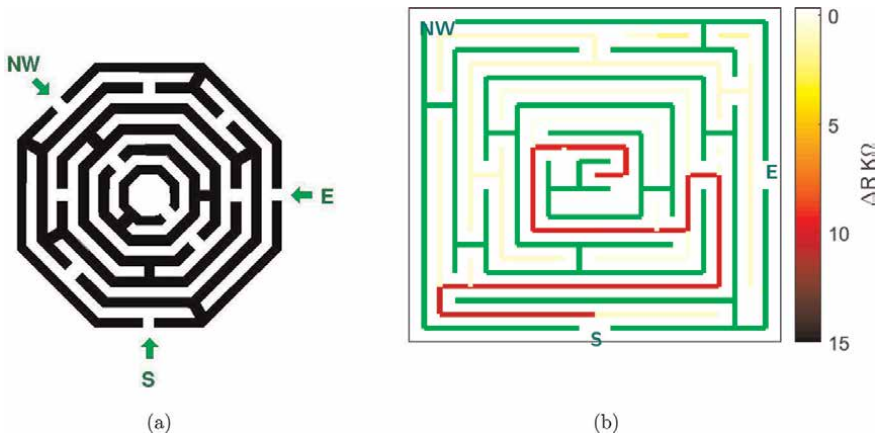

Figure 22.
Octogonal maze and solution.

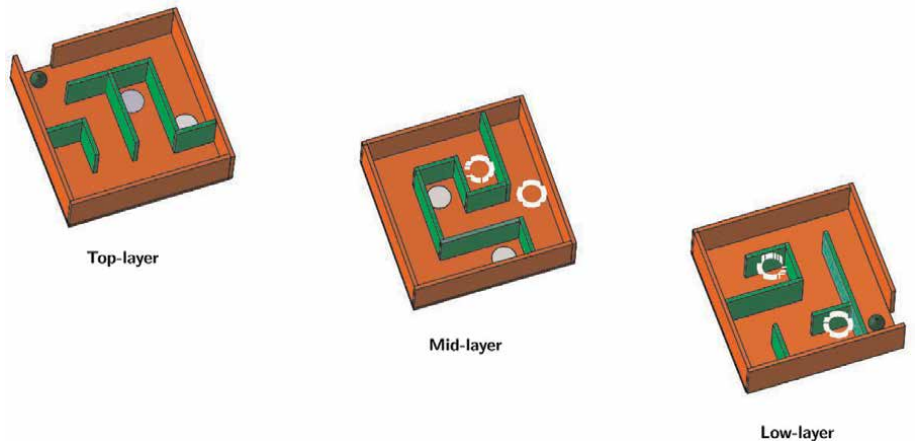

Figure 23.
A 3D-maze.

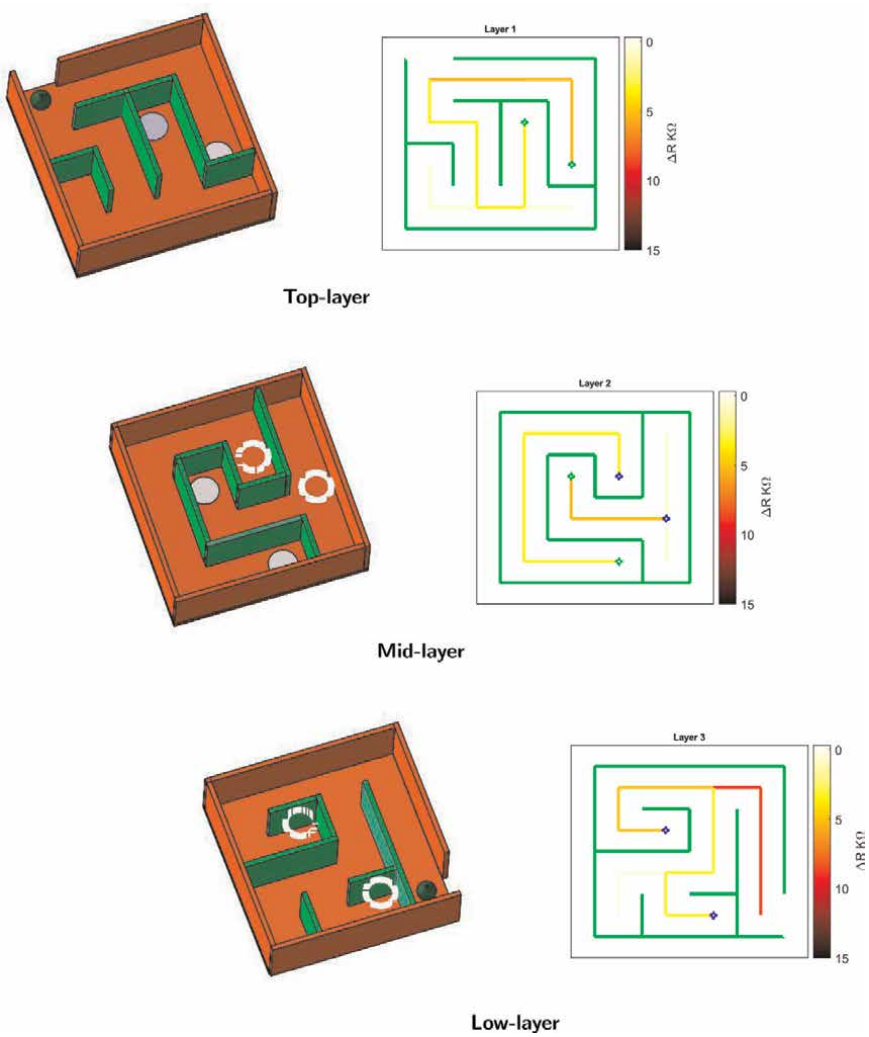

Figure 24.
Solutions of the 3D-maze.

indicates the starting point of the maze, while the ball in the low-layer points out to the output of the maze. The layers communicate each other with holes that are depicted as circles on the floor and disks on the roof of them.

The memristive grid that describes this maze counts 16 nodes per layer which yields a total of 48 nodes. Every layer possesses 24 branches (the external walls do not count) plus four inter-layer branches, i.e., 78 memristive fuses to describe the maze.

Finally, the output display given in **Figure 24** shows the progress of the solution procedure.

6. Code for the model

In the following, the code for the memristor model as used within HSPICE is given.

```
*Charge-controlled models
*INAOE, summer 2018
*Yojanes Rodríguez
.LIB MemModels
*-----------------------------------------------------
*HPMQ Joglekar k=5 01
.SUBCKT HPMQK501N N+ N-
.PARAM Xo=0.99
.PARAM mu=10f
.PARAM eta=-1
.PARAM Roff=16e3
.PARAM Ron=100
.PARAM Delta=10n
.PARAM kappa='Ron*mu/(POW(Delta,2))'
.PARAM Pol1='-(256/45)*POW(Xo,10)+32*POW(Xo,9)-(576/7)*POW(Xo,8)+128*POW
(Xo,7)-
+(672/5)*POW(Xo,6)+(504/5)*POW(Xo,5)-56*POW(Xo,4)+24*POW(Xo,3)-9*POW
(Xo,2)-Xo'
.PARAM Pol2='(256/45)*POW(Xo,10)-(224/9)*POW(Xo,9)+(352/7)*POW(Xo,8)-(1280/
21)*POW(Xo,7)+
+(736/15)*POW(Xo,6)-(136/5)*POW(Xo,5)+(32/3)*POW(Xo,4)-(8/3)*POW(Xo,3)+
+POW(Xo,2)-(1441/315)*Xo+1126/315'
.PARAM Pol3='-9*POW(Xo,2)+18*Xo-9'
.PARAM Pol4='-24*POW(Xo,3)+72*POW(Xo,2)-72*Xo+24'
.PARAM Pol5='-56*POW(Xo,4)+224*POW(Xo,3)-336*POW(Xo,2)+224*Xo-56'
.PARAM Pol6='-(504/5)*POW(Xo,5)+504*POW(Xo,4)-1008*POW(Xo,3)+1008*POW
(Xo,2)-504*Xo+504/5'
.PARAM Pol7='-(672/5)*POW(Xo,6)+(4032/5)*POW(Xo,5)-2016*POW(Xo,4)
+2688*POW(Xo,3)-
+2016*POW(Xo,2)+(4032/5)*Xo-(672/5)'
.PARAM Pol8='-128*POW(Xo,7)+896*POW(Xo,6)-2688*POW(Xo,5)+4480*POW(Xo,4)-
+4480*POW(Xo,3)+2688*POW(Xo,2)-896*Xo+128'
.PARAM Pol9='-(576/7)*POW(Xo,8)+(4608/7)*POW(Xo,7)-2304*POW(Xo,6)
+4608*POW(Xo,5)-
+5760*POW(Xo,4)+4608*POW(Xo,3)-2304*POW(Xo,2)+(4608/7)*Xo-576/7'
.PARAM Pol10='-32*POW(Xo,9)+288*POW(Xo,8)-1152*POW(Xo,7)+2688*POW(Xo,6)-
4032*POW(Xo,5)+
+4032*POW(Xo,4)-2688*POW(Xo,3)+1152*POW(Xo,2)-288*Xo+32'
.PARAM Pol11='-(256/45)*POW(Xo,10)+(512/9)*POW(Xo,9)-256*POW(Xo,8)+(2048/
```

```
3)*POW(Xo,7)-
+(3584/3)*POW(Xo,6)+(7168/5)*POW(Xo,5)-(3584/3)*POW(Xo,4)+
+(2048/3)*POW(Xo,3)-256*POW(Xo,2)+(512/9)*Xo-256/45'

*Integrator
Ecur Ni 0 VOL = 'I(Rmem)'
R Ni Na 1k
C Na No 1m
Eop No GND GND Na 1Meg

Echarge charge GND No GND -1


Rmem N+ N- R='(V(charge)>0)?(+(256/45)*POW(Xo,10)*exp(-200*kappa*V
(charge))-
+32*POW(Xo,9)*exp(-180*kappa*V(charge))+(576/7)*POW(Xo,8)*exp(-160*kappa*V
(charge))-
+128*POW(Xo,7)*exp(-140*kappa*V(charge))+(672/5)*POW(Xo,6)*exp(-
120*kappa*V(charge))-
+(504/5)*POW(Xo,5)*exp(-100*kappa*V(charge))+56*POW(Xo,4)*exp(-80*kappa*V
(charge))-
+24*POW(Xo,3)*exp(-60*kappa*V(charge))+9*POW(Xo,2)*exp(-40*kappa*V
(charge))+
+(Pol1)*exp(-20*kappa*V(charge)))*(Roff-Ron)+Roff:((Pol2)*exp(20*kappa*V
(charge))+
+(Pol3)*exp(40*kappa*V(charge))+(Pol4)*exp(60*kappa*V(charge))+
+(Pol5)*exp(80*kappa*V(charge))+(Pol6)*exp(100*kappa*V(charge))+
+(Pol7)*exp(120*kappa*V(charge))+(Pol8)*exp(140*kappa*V(charge))+
+(Pol9)*exp(160*kappa*V(charge))+(Pol10)*exp(180*kappa*V(charge))+
+(Pol11)*exp(200*kappa*V(charge)))*(Roff-Ron)+Ron'
.ENDS
*-------------------------------------------------------
.ENDL MemModels
```

7. Conclusions

A specially tailored memristive grid has been used as an analog processor for solving mazes. The memristives branches of the grid (fuses) are formed by an anti-series connection of two memristors and a switch. On one side, we have introduced a family of symbolic models for the memristor that are defined by charge-controlled functions. The fact that the models are charge-controlled allows us to monitor the velocity of the variation of the equivalent memristance of the fuses by carrying out a transient analysis with HSPICE. It is worth to mention that the model has been recast in VERILOG-A. On the other side, with the aim of producing a more realistic scenario, the switches are implemented by a transmission gate in CMOS technology. In this form, the resulting grid is in fact a hybrid CMOS-Memristor circuit.

The simulation flow-work is formed by an input stage developed in MATLAB, the electric simulation in HSPICE and the output stage again in MATLAB. The input stage is responsible for mapping the structure of the maze onto the memristive grid. The outcome of this stage is an input file with the netlist of the grid. The intermediate stage executes the transient simulation. The output stage is used to display the variation of the resistance of the fuses and it literally draws the solution path of the

maze. The solution is found by sensing the variations of the resistance of the fuses that belong to the path, which implies that the memristive grid achieves the shortest path algorithm.

Finally, the maze grid has proven its reliability in solving mazes with different levels of complexity. A series of examples has been analyzed: single-solution mazes, multiple-solution mazes, and a 3D maze.

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Chapter 5

Mathematical Analysis of Memristor CNN

Angela Slavova and Ronald Tetzlaff

Abstract

In this chapter we present mathematical study of memristor systems. More precisely, we apply local activity theory in order to determine the edge of chaos regime in reaction-diffusion memristor cellular nanoscale networks (RD-MCNN) and in memristor hysteresis CNN (M-HCNN). First we give an overview of mathematical models of memristors, CNN and complexity. Then we consider the above mentioned two models and we develop constructive algorithm for determination of edge of chaos in them. Based on these algorithms numerical simulations are provided. Two applications of M-HCNN model in image processing are presented.

Keywords: memristor, cellular nanoscale networks, reaction-diffusion systems, hysteresis, edge of chaos, image processing

1. Introduction

Memristors form an important emerging technology for memory and neuromorphic computing applications (**Figure 1**). Chua has developed the fundamentals of the memistor framework nearly 40 years ago [1]. Since then, the industry has been engaged in the search for novel materials and technologies of these nano-structures [2].

Mathematical models of the complex dynamics which can be exhibited by nano-devices is presented in [3]. General and simple models are very important in the investigations of nonlinear dynamics in memristors [4]. Such models of memristor-based circuits are presented in [5, 6]. In order to develop novel hybrid [7] hardware architectures combining memory storage and data processing in the same physical location and at the same time [8] to explain the behavior of biological systems [9] new accurate mathematical models need to be introduced (**Figure 2**). Although several physical models [10–13] have been derived in order to study phenomena characterizing these nano-devices, a circuit theoretic-based mathematical treatment allowing the development of memristor circuits is still restricted to few cases. Most of these mathematical models have been studied in [14]. The merit for the first model of a titanium dioxide-based nano-structure may be ascribed to Williams [15]. This model is simple not specifying boundary conditions in the state equation. Literature was later enriched with a number of more complex models taking into account nonlinear effects on ionic transport and defining behavior at boundaries. The model proposed by Joglekar and Wolf [16] may allow for single-valued state-flux characteristics only, under any sign-varying periodic input with zero mean. By contrast, only multi-valued state-flux characteristics may be reproduced by Biolek's

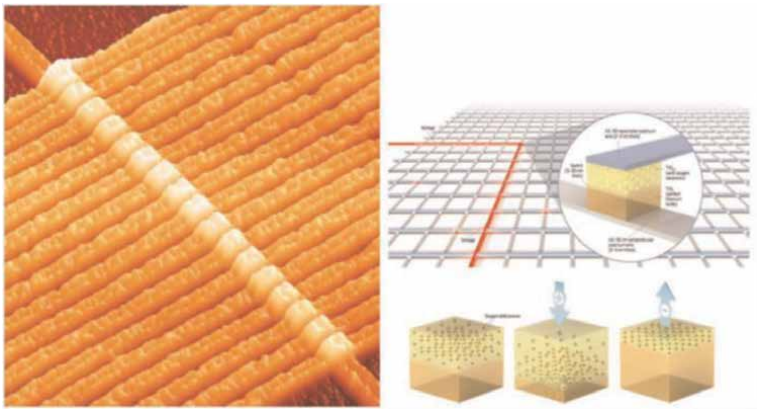

Figure 1.
Crossbar architecture and crossbar elements of a memristor.

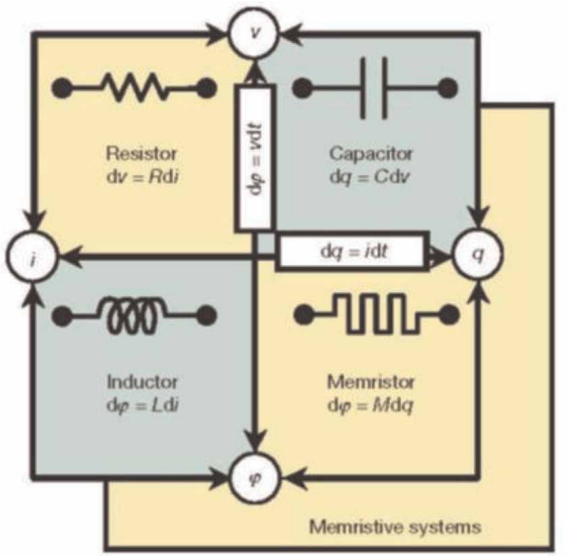

Figure 2.
Four basic circuit elements.

model [17] under the same type of excitation. A comparison of the dynamic behavior of titanium dioxide memristor circuits assuming different boundary models including the BCM model is given in [18]. The results underline the sensitivity of these nonlinear circuits to the modeling accuracy. In the following, models have been proposed also for memristors based on other materials, e.g., for a tantalum oxide element [13, 19] and for a niobium dioxide memristors [12]. Nevertheless, recent investigations [14] uncover numerical problems occurring in the numerical solution of the strongly nonlinear differential-algebraic equations or in a SPICE simulation [8] of these memristors.

Computing with memory is one of the main properties of neural networks, in which the performance is within localized memory storage. Therefore, they can provide high density analogue storage and can be integrated locally with computing elements which is the main advantage of the network learning algorithms. The memristive array works as a conventional memory, i.e., the weigh values can be calculated outside the array and can be programmed to the correct addresses. The

algorithms are flexible because they can be implemented with an appropriate design. Local and non-local learning algorithms can be implemented in a straightforward way. The disadvantage is that they cannot have high connectivity and internal dynamics.

Cellular Nonlinear/Nanoscale Networks (CNN) have been introduced in 1988 by Chua and Yang [20, 21] as a new class of information processing systems which show important potential applications (**Figure 3**). By endowing a single CNN cell with local analog and logic memory, some communication circuitry and further units, the CNN Universal Machine (CNN-UM) has been invented by Roska [22–24]. Analog CNN-UM chip hardware implementations have been developed some time ago. A CNN-UM chip represents a parallel computer with stored programmability allowing real-time processing of multivariate data. CNN have very promising applications in image processing and pattern recognition [22, 25–27]. Although, recently realized systems, e.g., the EyeRis 1.3 system, the MIPA4k, and SCAMP-5, are characterized as sensor-processor systems for high speed vision by reaching frames rates more than 20 kHz, their low resolution (e.g., 176×144 pixel in the EyeRis 1.3 system) limits the applicability to certain problems in practice only. Since the cell size cannot be decreased considerably in conventional CMOS technology, nano-elements will play an important role in future CNN-UM chip realizations. Especially, memristors [28] which are considered for synaptic connections in first realizations [29], will play an important role for the realization of future CNN-UM sensor-processor systems by taking their rich dynamical behavior into account. However, a deep mathematical treatment of CNN with memristors, briefly called memristor CNN in the following, has not been provided so far. Especially, the derivation of methods allowing the determination of the parameter space of a memristor CNN showing emergent complex behavior, is being essentially important in the development of CNN-based computational methods.

Many scientists have struggled to uncover the elusive origin of "complexity" and its many equivalent jargons, such as emergence, self-organization, synergetics, collective behaviors, non-equilibrium phenomena, etc. [22, 30–32]. In his works, Schrödinger [31] defines the exchange of energy as a necessary condition for complexity of open systems. Prigogine [32] states the instability of the homogeneous systems as a new principle of nature, whereas Turing finds the origin of morphogenesis in symmetry breaking. In [31] Smale considers a reaction-diffusion system

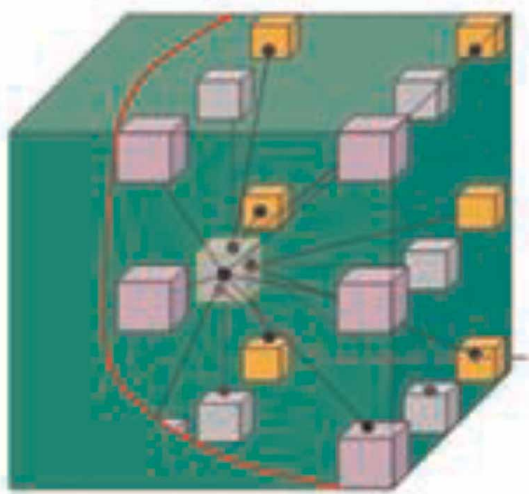

Figure 3.
CNN architecture.

which has properties such that it makes the Turing interacting system to oscillate. Recent laboratory observations suggesting that chaotic regimes may in fact represent the ground state of central nervous system point to the intriguing possibility of exploiting and controlling chaos for future scientific and engineering applications.

Among other things, a mathematical proof is given in [22, 30, 33, 34] showing that none of the complexity related jargons cited above can explain emergent complex behavior in reaction-diffusion system without introducing local activity. The theory of local activity offers a constructive method for determination of complexity. We shall propose algorithm for hysteresis CNN which defines the domain of the cell parameters in which the system is capable of exhibiting complexity. The main advantage of local activity theory is that the complex behavior of reaction-diffusion system can be explained in a rigorous way by explicit mathematical formulas determining a small subset of locally active parameters' region called edge of chaos. Cell kinetic equations which are locally active can exhibit limit cycles or chaos if the cells are uncoupled from each other by letting all diffusion coefficients to be zero. In this case complex spatiotemporal phenomena arise, such as spatiotemporal chaos or scroll waves.

In particular, constructive and explicit mathematical inequalities can be obtained for identifying that region in the CNN parameter space. By restricting the cell parameter space to the local activity domain, a major reduction in the computing time required by the parameter search algorithms is achieved [33, 34].

In the next sections we shall present two mathematical models of memristor CNN. First one is reaction-diffusion memristor CNN, and the second one is memristor hysteresis CNN. We shall derive algorithm for determination of edge of chaos regime in these models based on local activity theory [33].

2. Reaction-diffusion memristor CNN (RD-MCNN)

Nonlinear reaction-diffusion types of equations are widely used to describe phenomena in different fields. We shall determine for reaction-diffusion CNN the domain of the cell parameters in which the cells are locally active and therefore they can exhibit complex behavior. Edge of chaos (EC) is associated with a region of parameter space in which complex phenomena and thus information processing can appear.

In this section the principle of local activity will be applied in studying complex behavior of reaction-diffusion CNN with memristor synapses (RD-MCNN). Semiconductor reaction-diffusion (RD) large scale circuits (LSI) implementing RD dynamics, called reaction-diffusion chips, are mostly designed by digital, analog, or mixed-signal complementary-metal-oxide-semiconductor (CMOS) circuits of CNN and cellular automata (CA).

In our model each cell will be arranged on a two-dimensional square grid and will be connected to adjacent cells through coupling devices that mimic 2-D spatial diffusion and transmit the cell's state to its neighboring cells, as in conventional CNN.

We shall consider a discrete medium of identical cells which interact locally and therefore the homogeneous medium exhibits a non-homogeneous static or spatiotemporal patterns under homogeneous initial and boundary conditions. The theory of local activity will be formulated mathematically and implemented in circuit models. We shall start with reaction-diffusion CNN equations as a special class of spatially extended dynamical systems and we shall define the principle of local activity which will not be based on observations but on rigorous mathematical analysis.

2.1 Definition of local activity for reaction-diffusion equations

We call reaction-diffusion CNN equations locally active if and only if their cells are locally active at some cell equilibrium points [33].

In [34] principle of local activity is explained with the assumption of zero energy at the zero time. Therefore we can say that the cell is acting as a source of small signal energy and it is able to give rise to an initially very small input signal to a larger energy signal.

From mathematical point of view the signal should be very small in order to take the linear terms of Taylor series expansion of the cell model. In this way we can derive explicit analytical inequalities for the cell to be locally active at some equilibrium points in which the Taylor series expansion is computed. In other words, we can say that complex behavior of cells arises from infinitesimal small perturbations.

In this section we shall consider reaction-diffusion system [35, 36]:

$$\begin{aligned}\frac{\partial u(x)}{\partial t} &= g_u \nabla^2 u(x) + f_u(u(x), v(x)) \\ \frac{\partial v(x)}{\partial t} &= g_v \nabla^2 u(x) + f_v(u(x), v(x))\end{aligned} \tag{1}$$

where $g_{u,v}$ are the diffusion coefficients, $f_{u,v}(.)$ state for the reaction model. In (1) $u(x)$ and $v(x)$ are represented by voltages on the RD hardware, and the gradient is represented by linear resistors.

Let us discretize first equation of (1) in space:

$$\frac{d\, u_j(t)}{dt} = \frac{g_u\left(u_{j-1} - u_j\right) + g_u\left(u_{j+1} - u_j\right)}{\Delta x^2} + f_u(.), \tag{2}$$

where j is the spatial index, Δx is the discrete step in space, terms $g_u\left(u_{j-1} - u_j\right)$ and $g_u\left(u_{j+1} - u_j\right)$ represent respectively current flowing into the jth node from $(j-1)$th and $(j+1)$th nodes via two resistors whose conductance is represented by g_u.

We consider the memristor model [9], in which the resistors are replaced with memristors:

$$i = g_u(w)v,\ \frac{dw}{dt} = i, \tag{3}$$

where the voltage across the memristor is v, the current of the memristor is i, the nominal internal state of the memristor corresponding to the charge flow is w, and the monotonically non decreasing function is $g_u(w)$ when w is increasing.

We shall replace resistors for diffusion in analog RD LSIs with memristors (**Figure 4**).

Then we obtain the resulting point dynamics

$$\begin{aligned}\frac{du_j}{dt} &= \frac{g_u\left(w_j^l\right)\left(u_{j-1} - u_j\right) + g_u\left(w_j^r\right)\left(u_{j+1} - u_j\right)}{\Delta x^2} + f_u(.), \\ \frac{dv_j}{dt} &= f_v(.),\end{aligned} \tag{4}$$

where $g_u(.)$ is the monotonically increasing function defined by:

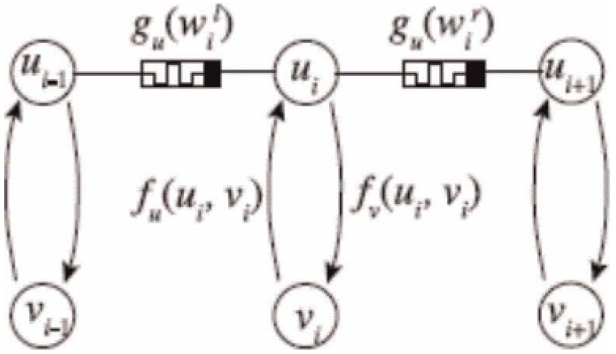

Figure 4.
Circuit realization.

$$g_u\left(w_j^{l,r}\right) = g_{min} + \left(g_{max} - g_{min}\right) \frac{1}{1 + e^{-\beta w_j^{l,r}}}, \tag{5}$$

where β is the gain, g_{min} and g_{max} are the minimum and maximum coupling strengths, respectively, and $w_j^{l,r}$ denotes the variables for determining the coupling strength (l—leftward, r—rightward).

We introduce the following memristive dynamics for $w_j^{l,r}$:

$$\tau \frac{dw_j^{l,r}}{dt} = g_u\left(w_j^{l,r}\right).\eta_1.\left(u_{j-1} - u_j\right), \tag{6}$$

where the right-hand side represents the current of the memristors in (2), η_1 denotes the polarity coefficient—$\eta_1 = +1$: w_j^l, $\eta_1 = -1$: w_j^r.

In the next we shall study RD-MCNN model of FitzHugh-Nagumo system.

Simplification of Hodgkin-Huxley model (**Figure 5**) can be given by FitzHugh-Nagumo system consisting of two coupled partial differential equations with two diffusion coefficients. In generally it describes the electrical potential across cell membrane when the flow of ionic channels is changed. It also can be presented as the model of electrical waves of the heart.

In this section we shall present the following FitzHugh-Nagumo system with two diffusion terms:

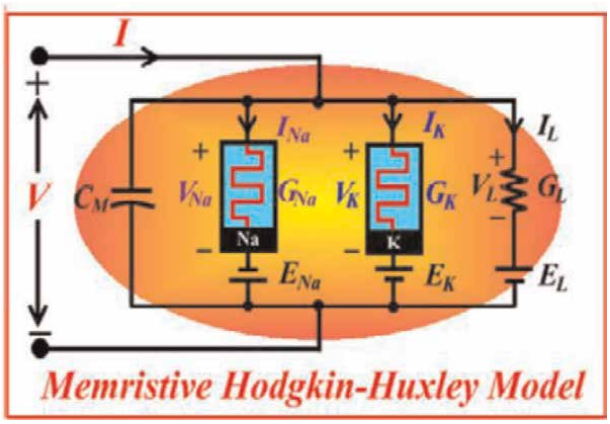

Figure 5.
Memristive model.

$$\begin{aligned}\frac{\partial u}{\partial t} &= f_1(u,v) + d_1\nabla^2 u,\\ \frac{\partial v}{\partial t} &= f_2(u,v) + d_2\nabla^2 v,\end{aligned} \tag{7}$$

where

$$\begin{aligned}f_1(u,v) &= -\frac{1}{\varepsilon}u(u-1)\left(u-\frac{b+v}{a}\right),\\ f_2(u,v) &= f(u) - v,\end{aligned} \tag{8}$$

$f(u)$ is monotonically non decreasing function

$$f(u) = \begin{cases} 0, & 0 \le u \le \frac{1}{3}\\ 1 - \frac{27u(u-1)^2}{4}, & \frac{1}{3} \le u \le 1\\ 1 & u > 1\end{cases}$$

The parameters ε, a, b are physical parameters, related to pressures of oxide, carbon oxide and to the temperature.

We discretize spatially system (7) and the resulting point dynamics are given as:

$$\begin{aligned}\frac{du_{ij}}{dt} &= f_1(u_{ij},v_{ij}) + d_1(w^{l,r})\left(u_{i-1j} + u_{i+1j} + u_{ij-1} + u_{ij+1} - 4u_{ij}\right)\\ \frac{dv_{ij}}{dt} &= f_2(u_{ij},v_{ij}) + d_2(w^{l,r})\left(v_{i-1j} + v_{i+1j} + v_{ij-1} + v_{ij+1} - 4v_{ij}\right),\end{aligned} \tag{9}$$

where $d_k(w^{l,r})$ denotes the monotonically increasing function defined as

$$d_k(w^{l,r}) = d_{min} + (d_{max} - d_{min}).\frac{1}{1 - e^{-\beta w_k^{l,r}}},\ \mathrm{k} = 1, 2 \tag{10}$$

Then the memristive dynamics is defined as in (6).

We shall apply the constructive algorithm for determining edge of chaos (EC) region for the memristive FitzHugh-Nagumo system (9) and (10).

- We map memristive FitzHugh-Nagumo system into the associated FitzHugh-Nagumo CNN model:

$$\begin{aligned}\frac{du_{ij}}{dt} &= f_1(u_{ij},v_{ij}) + d_1(w)\left(u_{i-1j} + u_{i+1j} + u_{ij-1} + u_{ij+1} - 4u_{ij}\right)\\ \frac{dv_{ij}}{dt} &= f_2(u_{ij},v_{ij}) + d_2(w)\left(v_{i-1j} + v_{i+1j} + v_{ij-1} + v_{ij+1} - 4v_{ij}\right),\end{aligned} \tag{11}$$

- We find the equilibrium points of (11). According to the theory of dynamical systems equilibrium points u^*, v^* are these for which:

$$\begin{aligned}f_1(u^*,v^*) &= 0\\ f_2(u^*,v^*) &= 0\end{aligned} \tag{12}$$

System (12) may have one, two or three real roots (u_1^*, v_1^*), (u_2^*, v_2^*), (u_3^*, v_3^*). In general, these roots are functions of the cell parameters a, b, ε.

- We calculate the four cell coefficients $a_{11}, a_{12}, a_{21}, a_{22}$ of the Jacobian matrix of (12) about each system equilibrium point E_k^*, $k = 1, 2, 3$.

- Then we calculate the trace $Tr(E_k^*)$ and the determinant $D(E_k^*)$ of the Jacobian matrix of (12) for each equilibrium point.

- We define locally active region for each equilibrium point E_k^*:

$$LAR(E_k^*) : a_{22} > 0, \text{ or } 4a_{11}a_{22} < (a_{12} + a_{21})^2$$

- Additional stability condition in this case is:

$$Tr(E_k^*) < 0 \text{ and } D(E_k^*) > 0$$

It can be shown that this is the only region which corresponds to locally asymptotically stable equilibrium points of our model.

- We define the stable and locally active region $SLAR(E_k^*)$.

- In our particular case, we have three equilibrium points $E_1 = (0, 0), E_2 = (1, 1), E_3 = \left(\frac{b+1}{a}, 1\right)$.

Then we check the conditions for the local activity and stability of the equilibrium points. The result is that only E_1, E_2 satisfy these conditions.

By the above presented algorithm we can prove the following theorem:

Theorem 1. *We say that MCNN model of FitzHugh-Nagumo system (7) and (8) operates in EC region if and only if the following conditions for the cell parameters are satisfied:*

$$\varepsilon \ll 1, \ \frac{a - b - 1}{a} < 1.$$

In other words there is at least one equilibrium point which is in $SLAR(E_k^*)$.

In the simulations of the above algorithm we can see the cell parameter projection on the (T, Δ, a_{22})-plane (**Figure 6**). We have red subregion in which we have three equilibrium points of our model and at least one is both stable and locally active; blue subregion in which we have either one or three equilibrium points and every equilibrium point is unstable; green subregion in which there is only one equilibrium point and it is both stable and locally active. By definition, red and green subregions in **Figure 6a** together constitute the edge of chaos. In **Figure 6b** we can see the plot of edge of chaos regime in the parameter (a, b, ε) plane.

Through extensive numerical simulations we obtain that non uniform spatial patterns are generated in our CNN model with memristor synapses depending on initial conditions—see **Figure 7**.

Through the above numerical simulations, the following things were demonstrated: (a) excitable waves propagating on the memristor can modulate the memristor conductance which depends on the memristor's polarity; (b) change of memristor conductance can modulate the velocity of the excitable wave propagation, and it is inversely proportional to the time constant of the model; (c) the model under consideration generates nonuniform spatial patterns which process depends on the initial condition of FitzHugh-Nagumo system (7) and (8), memristor polarity and stimulation.

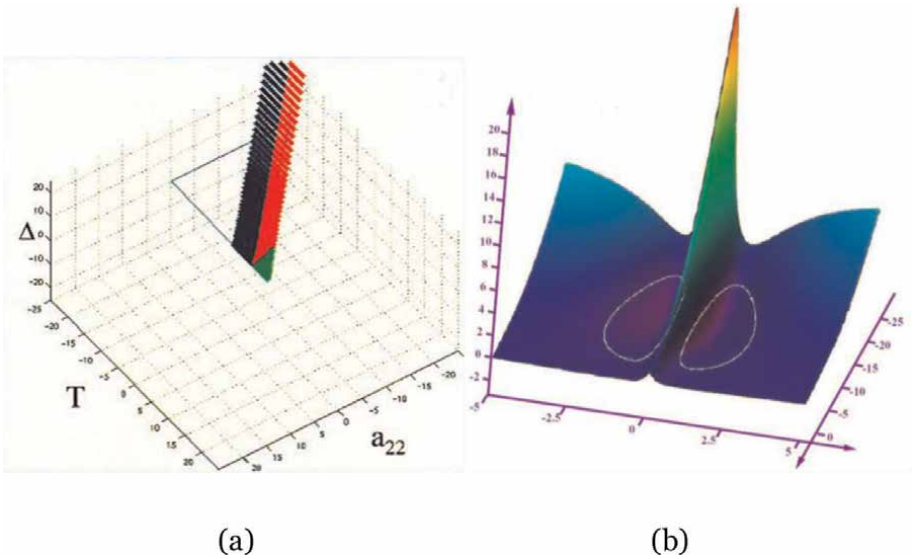

Figure 6.
Simulations.

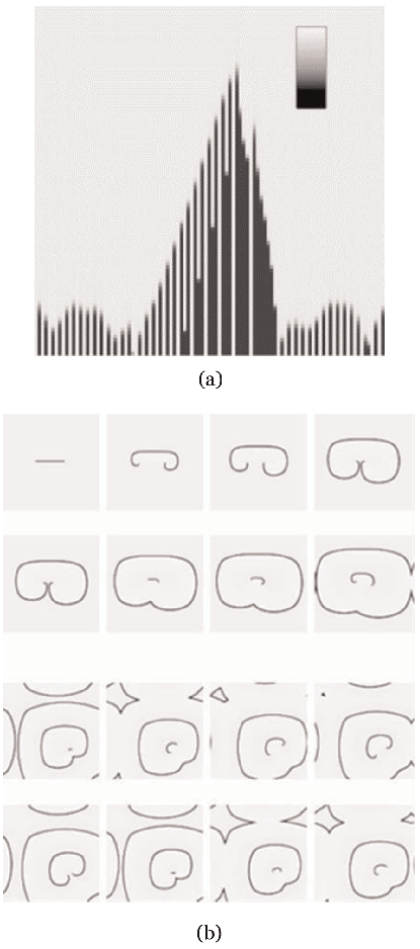

Figure 7.
Pattern formation: (a) spatial pattern formation and (b) clockwise spiral wave patterns.

3. Hysteresis CNN with memristor synapses

In this section we shall present mathematical study of hysteresis CNN (HCNN) with memristor synapses. In our model the cells are of first order and they have hysteresis switches. It is known from the literature [21–26, 35, 37–41] that such models have many applications because they operate in two modes—bi-stable multi-vibrator mode and relaxation oscillator mode. We shall consider HCNN working in second one. When CNN operates in the relaxation oscillator mode then various patterns and nonlinear waves can be generated. Associative (static) and dynamic memories functions can be derived from the hysteresis CNN [35, 37, 41].

Let us consider hysteresis CNN with memristor synapses, which we shall call memristor hysteresis CNN (M-HCNN):

$$\frac{du_{ij}}{dt} = -m(u_{ij}) + \sum_{k,\, l \in N_{ij}} \left(a_{k-i,\, l-j} f(u_{kl})\right) \qquad 1 \le i, j \le \mathrm{N}, \tag{13}$$

where u_{ij} denotes the state of the cell, the output $y_{ij} = f(u_{ij})$ is dynamic hysteresis function defined by:

$$f(u(t)) = \begin{cases} 1, \text{ for } u(t) > -1, f(u(t_-)) = 1 \\ -1, \text{ for } u(t) = -1 \\ -1, \text{ for } u(t) < 1, f(u(t_-)) = -1 \\ 1, \text{ for } u(t) = 1, \end{cases} \tag{14}$$

$t_- = \lim_{\varepsilon \to 0} (t - \varepsilon)$, $\varepsilon > 0$, $m(.)$ is defined as $m(u_{ij}) = \frac{u_{ij}}{M(t)}$ in which by $M(t)$ we denote the memristance. When we insert memristor [9] in HCNN model we expect to obtain better resolution in static and dynamic images [41]. We introduce a memristor in HCNN by replacing the original linear resistor. In this way it can exhibit nonlinear current-voltage characteristic with locally negative differential resistance. The main advantage of our memristor HCNN (M-HCNN) is the versatility and compactness due to the nonvolatile and programmable synapse circuits. In the circuit realization of M-HCNN the output function is not complex.

Let us consider M-HCNN model working in a relaxation oscillator mode described by

$$\frac{du_{ij}}{dt} = -m(u_{ij}) - 2h(u_{ij}) + bf(u_{ij}), 1 \le i, j \le N. \tag{15}$$

Below is the picture of relaxation oscillator under consideration (**Figure 8**).

M-HCNN model (15) generates patterns close to the bifurcation point $b = 3$. Computer simulations of (15) when we use the Laplace template $\begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$ show the generation of spiral waves for b = 3 (see **Figure 9**):

3.1 Determination of edge of chaos domain in M-HCNN model

We shall apply theory of local activity [33, 34] in order to study the dynamics of M-HCNN model (15). The theory which will be presented below offers both constructive analytical and numerical method for obtaining local activity of M-HCNN. It is known [35, 41] that the cells of HCNN can exhibit complexity in the domain of

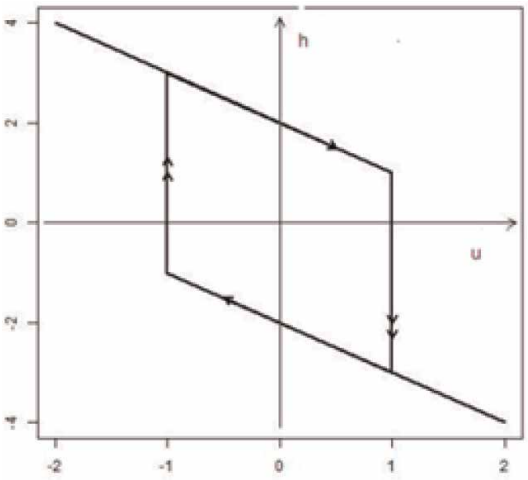

Figure 8.
Relaxation oscillator defined by (15).

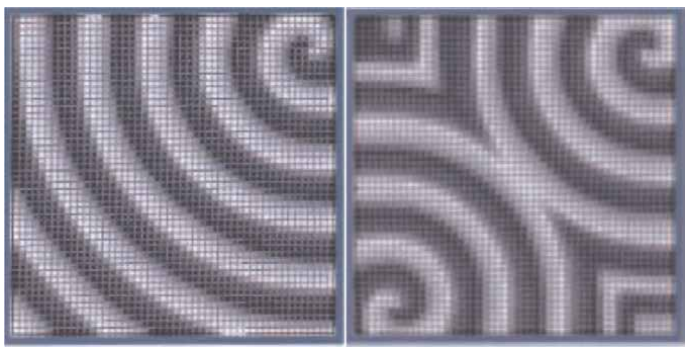

Figure 9.
Spiral waves in HCNN model (15).

cell parameters in which the cells are locally active. We shall develop constructive and explicit mathematical inequalities for identifying the region in the M-HCNN model (15) parameter space where complexity phenomena may emerge. By restricting the cell parameter space to the local activity domain we can achieve a major reduction in the computing time required by the parameter search algorithms. This will allow to determine and control chaos which will be useful for the future scientific and engineering applications [34, 41, 42].

We shall develop constructive algorithm for studying the dynamics of our M-HCNN model (15) based on [33]:

(1) We chose the Laplace template of the following type $\begin{pmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{pmatrix}$ in order to discretize the M-HCNN model (15). Then in relaxation mode the dynamics of an isolated cell when there are no control and threshold parameters can be written:

$$\frac{du_{ij}}{dt} = -m(u_{ij}) - 2h(u_{ij}) + bf(u_{ij}) = F(u_{ij}). \tag{16}$$

(2) We can find the equilibrium points E_k of (16), which satisfy the equation $F(u_{ij}) = 0$. In general, this system may have four real roots as functions of the cell parameters.

(3) We calculate the cell coefficients $a_{11}(E_k)$, $a_{12}(E_k)$, $a_{21}(E_k)$, $a_{22}(E_k)$, $k = 1, 2, 3, 4$.

(4) We denote the trace of the Jacobian matrix at equilibrium point by $Tr(E_k)$ and determinant by $\Delta(E_k)$.

Remark. In order to provide physical implementation it is important to have appropriate circuit model for which we can use the results from the classical circuit theory. In order to obtain locally active cells it is sufficient the cell to act as a source of small signal in at least one equilibrium point. In this way the cell injects a net small signal average power into the passive resistive grids.

Let us now define stable and locally active region for the M-HCNN model (16).

Definition 1. *We say that the cell is both stable and locally active region at the equilibrium point E_k for M-HCNN model (16) if*

$$a_{22} > 0 \text{ or } 4a_{11}a_{22} < (a_{12} + a_{21})^2 \text{ and}$$
$$Tr(E_k) < 0 \text{ and } \Delta(E_k) > 0.$$

This region in the parameter space is called $SLAR(E_k)$.

(5) We shall define the EC region our M-HCNN model (16). According to [33, 34] it is such region in the cell parameter space where we can expect emergence of complex phenomena and information processing.

Definition 2. *For M-HCNN model (16) edge of chaos region is such that there exists at least one equilibrium point both locally active and stable.*

Based on the above algorithm we can prove the following theorem:

Theorem 2. *We say that M-HCNN model (16) is working in edge of chaos regime if and only if the following conditions are satisfied: $-1 < b < 3$. In other words there is at least one equilibrium point which is locally active and stable.*

We obtain the following edge of chaos domain for our M-HCNN model (16) through computer simulation:

The location of 16 cell parameter points arbitrarily chosen within the locally active domain. We have locally active and stable (or edge of chaos) in red; locally active and unstable in green; locally passive in blue (**Figure 10**).

3.2 Simulation results and some applications

In this section we shall consider two applications of M-HCNN model (16) in image processing. First one is for edge extraction and the second one is for noise removal. In our simulations we use programing environment MATLAB and we use a forward Euler algorithm with a time step size Δt = 0.01. The dynamic hysteresis function $h(x)$ can be programmed applying this algorithm is:

$$h(u(t_n)) = \begin{cases} 1, & for\ u(t_n) > -1, \quad h(u(t_{n-1})) = 1 \\ -1, & for\ u(t_n) = -1, \\ -1, & for\ u(t_n) < 1, \quad h(u(t_{n-1})) = -1 \\ 1, & for\ u(t_n) = 1, \end{cases}$$

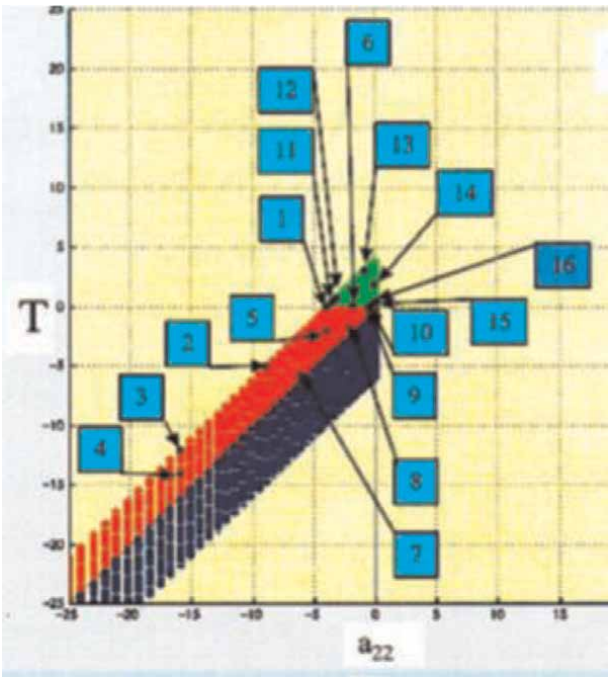

Figure 10.
Edge of chaos domain for M-HCNN model (16).

$$t_n = n\Delta t,\ n = 1, 2, \ldots$$

We shall start with the application of our M-HCNN model for edge extraction. The simulations are presented below (see **Figure 11**):

It is known that for feature extraction we firstly extract the edges of the image, which contain most of the information for the image shape. In the example provide on **Figure 11** we show the original image—(a), and then the results which we obtain simulating M-HCNN model—(b) and standard CNN model—(c). It can be seen that the results from M-HCNN (16) model and CNN model are very similar.

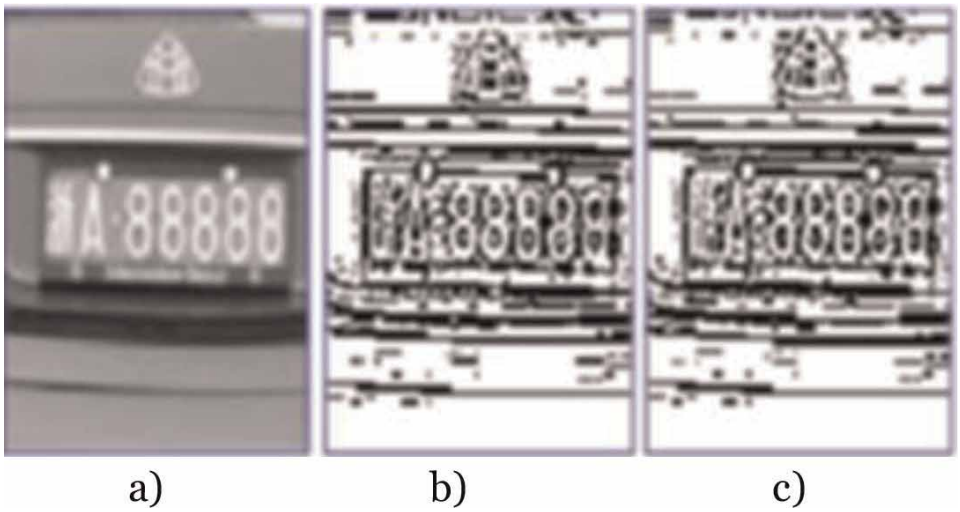

Figure 11.
Example of edge extraction: (a) original image, (b) M-HCNN, and (c) standard CNN.

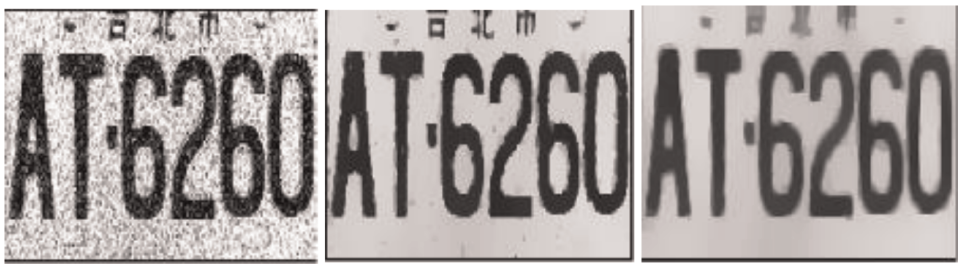

Figure 12.
Simulation of noise removal by M-HCNN model and by standard CNN model: (a) noise, (b) M-HCNN, and (c) CNN.

Another application which we shall present is for noise removal. The results of our simulations are given on the figure below (see **Figure 12**):

The applications of CNN show that the linear image processing can be compared to spatial convolution with infinite impulse response kernels [21, 41, 42]. When taking the image by a camera from the real world there is a possibility it to be polluted with some noise. That is why noise removal is very important for CNN applications such as AI devices, IoT. In our case, the simulations of M-HCNN model (16) shown in **Figure 12** present very good processing performance of noise removal similar to the simulations of standard CNN.

4. Conclusions and discussion

In this chapter, we stated the local activity theory for reaction-diffusion equations and hysteresis systems. However it can be generalized to other systems. In particular, the developed constructive procedure is applicable to any system whose cells and couplings are described by deterministic mathematical models. The crux of the problem is to derive testable necessary and sufficient conditions which guarantee that the system has a unique steady state solution at $t \to \infty$. A homogeneous non conservative medium cannot exhibit complexity unless the cells, or the coupling network is locally active.

In the second part of the chapter we focus our attention on HCNN model which has memristor synapses. The concept of CNN is based on some aspects of neurobiology and is adapted to integrated circuits. CNN are defined as spatial arrangements of locally coupled dynamical systems, cells. The CNN dynamics is determined by a dynamic law of an isolated cell, by the coupling laws between the cell and by boundary and initial conditions. The dynamic law and the coupling laws of a cell are often combined and described by a nonlinear ordinary differential- or difference equation (ODE), the state equation of a cell. Thus a CNN is given by a system of coupled ODEs with a very compact representation in the case of translation invariant state equations. Despite of having a compact representation CNN can show very complex dynamics like chaotic behavior, self-organization, pattern formation or nonlinear oscillation and wave propagation. Analog CNN chip hardware implementations have been developed [23]. The future of CNN implementation is in nano-structure computer architecture. CNN not only represent a new paradigm for complexity but also establish novel approaches to information processing by nonlinear complex systems. CNN have very impressive and promising applications in image processing and pattern recognition [22, 43]. After the introduction of the CNN paradigm, CNN Technology got a boost when the analogic cellular computer

architecture, the CNN Universal Machine has been invented [24, 30]. The unique combined property of memristors [44] to store the information for a very long time after the power is switched off may allow the development and circuit implementation of memcomputing paradigms.

We develop algorithm for determination of EC domain of the cell parameter space for M-HCNN model (16). Two applications are presented—for edge detection and noise removal. The conclusions of the simulation results are that the image does not change when we vary the memristor weights which is possible because of the binary quantization of the output. The speed of the numerical simulations of our M-HCNN model could be enlarged due to the need of more iterations of the algorithm in order to obtain stable solutions. But the quality of the image does not change.

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Chapter 6

Memristor Behavior under Dark and Violet Illumination in Thin Films of ZnO/ZnO-Al Multilayers

Adolfo Henrique Nunes Melo, Raiane Sodre de Araujo, Eduardo Valença and Marcelo Andrade Macêdo

Abstract

ZnO/ZnO-Al thin films were grown aiming the development of a memristor. Electrical voltage sweeps were imposed to induce dopant migration and to achieve several resistance states. A memristor behavior was observed, presenting adaptation to external electrical stimulus. Voltage sweeps occurred under the influence of violet light and in the dark, alternately, and the influence of the photon incidence on the current intensity was noticed. Throughout the alternating cycles between light and dark, less resistance was observed under illumination, but the migration of Al and O ions caused the formation of Al_2O_3 and ZnO oxides, resulting in a gradual increase in resistance. With constant voltage, the device presented continuous modification of resistance and sensitivity to the violet light with generation of free carriers. These results bring new opportunities for using memristors as violet light sensors as well as new insights for light-controlled memristor development.

Keywords: memristor, ZnO, ZnO-Al, thin films, violet sensor, dark, illumination, memristive behavior

1. Introduction

In 1971, Leon Chua predicted the existence of a fourth electronic passive element of two terminals, called a memristor (a union of the terms memory and resistance) [1]. A memristor is basically a resistor that has its resistance altered with external stimulation in a nonvolatile way. In other words, it maintains the state of resistance even if the stimulus is removed. In 1976, Chua and Kang determined that a wide class of devices and systems can be considered as memristives when they present time-dependent electrical resistance and also depend on application of electric voltage [2]. Memristor devices can be configured in nonvolatile memories, logic gates, and programmable connections having high-density integration or presenting complementary metal-oxide-semiconductor (CMOS) compatibility [3]. This CMOS compatibility makes memristors excellent candidates to go beyond Moore's law.

In 2008, in Hewlett-Packard (HP) laboratories, thin films of titanium dioxide prepared with two terminals presented memristor characteristics [4]. Their basic structure was based on epitaxial growth of metal-insulator-metal (MIM) thin

films [5–7]. With the experimental development of memristors in HP laboratories, there has been increasing research in this area, and several materials have been constructed in the MIM structure for analysis of memristive behavior. There is an appreciable number of materials that have been applied in the design of the MIM structure, such as semiconductor insulation (III-V), including MgO, TiO_x, ZrO_x, HfO_x, NbO_x, AlO_x, ZnO_x, or rare-earth oxides containing Y, Ce, Sm, Gd, Eu, Nd, and perovskites ($SrTiO_3$, $Ba_{0.7}Sr_{0.3}TiO_3$) [8, 9]. In addition to such applications as nonvolatile memory, devices based on transparent memristors can be applied even in near-eye display technology that requires the construction of transparent memories, transparent switches, and optical sensors [10]. These devices can also act as synapse elements, creating neural computing machines resembling the behavior of the biological brain [7, 11, 12].

However, transparent conductive oxides (TCOs) have been widely studied because they are essential components in flat-panel monitors, solar cells, touch screens, light-emitting diodes (LEDs), ultraviolet (UV) detectors, and other optoelectronic devices [10, 13, 14]. In addition, new transparent devices are being developed in applications of neuromorphic circuits [4, 7, 15] and adaptive systems [16, 17] in which they are based on resistive commutation depending on the history of the electric voltage application. Among the various materials that have memristor characteristics, ZnO stands out for its low toxicity, low cost, wide resistive switching ratio ($R_{off}/R_{on} \sim 10^{11}$), low power consumption, fast recording, and high-density storage [5, 10, 18, 19]. For the construction of a transparent MIM system, an indium tin oxide (ITO) substrate can be used because of its optical properties (transmittance ~90%) and electrical properties (sheet resistance ~20 Ω/sq) [20]. Transparent thin films of ZnO have been extensively studied which acquires excellent optical and electrical properties when doped with such metals as Al [21], Ti [22], and Nb [13], but a multilayer insulator/insulator+metal system may be a good candidate for memristor characteristics, where the diffusion of metallic ions may favor the mechanism of adaptation to the external electrical stimulus. Some researchers have reported thin films of ZnO/ZnO:Al presenting optical transmission of $> 80\%$ and bandgap $E_g = 3.32\,eV$ [23] or ranging from 3.65 to 3.72 eV when grown under heat treatment (300–500°C) [24].

Bandgap studies have an important role for light detection (near the ultraviolet UV zone in the case of ZnO), biological and environmental research, and detection sensors, being a protagonist in several chemical processes, which makes its determination extremely important. Bandgap determination can favor the development of wavelength-sensitive circuits enabling the generation of electrical signals that can be measured. However, memristive systems require electric charge flux through the device, which causes variation in the internal electrical resistance. This can be controlled using light incidence in addition to the usual electrical voltage. Inspired by the biological processes, Chen et al. demonstrated a visual memory unit in which it was based on In_2O_3 resistive switching, where logic states (0) and (1) associated with the high-resistance state and low-resistance state, respectively, were achieved under dark and UV illumination conditions, where the existence of UV stimulation provides the possibility of light information being memorized and erased under voltage sweep and then records light patterns, such as butterfly or heart shaped, in arrangements of 10 × 10 pixels [25].

In this work, ITO/ZnO/ZnO-Al memristor devices were grown using magnetron sputtering. They were subjected to electrical voltage sweep to study homogeneous resistive switching behavior under illumination and dark ambient conditions. The analysis of optical transmission and absorption properties and bandgap determination are also presented.

2. Experimental details

Thin films of ZnO/ZnO-Al were deposited on substrates of 100-nm Asahi Glass indium tin oxide (ITO) through physical deposition system RF/DC magnetron sputtering (AJA International). Three samples of ZnO thin films were grown on ITO using 100-W RF applied to a ceramic target of ZnO (99.9% purity, Macashew Technologies) as a function of the deposition time (40, 60, and 100 min). On these samples, a ZnO-Al film was grown by codeposition for 15 min, where an Al target (98.8%) was exposed to a 50 W DC source and simultaneously the ZnO target to 100 W RF. In all depositions, the base pressure was $\sim 10^{-6}$ Torr, and the working pressure with Ar gas was 20 mTorr with continuous flux of 20 sccm. There was no supply of oxygen flow, and all depositions were without heating source. The samples in this case had an epitaxial architecture. For simplicity, coding was performed, where ZA1 refers to the sample ITO/ZnO(100 min)/ZnO-Al(15 min), ZA2 refers to ITO/ZnO(60 min)/ZnO-Al(15 min), and ZA3 to ITO/ZnO(40 min)/ZnO-Al(15 min). The crystallinity of the samples was analyzed by X-ray diffraction (Bruker D8 Advance—CuK_α radiation with $\lambda = 0.154$ nm). A concentration profile of chemicals per depth was obtained through the Rutherford backscattering spectroscopy (RBS) technique carried out by bombardment of He^+ (2.2 MeV). The RBS data were obtained simultaneously at 120° and 170° scattering angles. This methodology was applied previously for the fabrication of these samples, and some results were previously published [26]. Transmission and optical absorption measurements were performed by UV-Vis spectrophotometry between 200 and 800 nm (Varian Cary 100 Scan UV-Vis spectrophotometer). All electrical measurements were performed using a voltage-current source (Keysight Agilent B2901) where, for the upper electrode, a Pt tip with ~200 μm in diameter was attached to a rod with micrometric displacement for a better approximation of the sample surface. The lower electrode (ITO) was grounded in all measurements. For realization of the measurements under illumination and dark conditions, a dark chamber was home built. A violet LED was coupled 1 cm away from the sample surface; this distance was suitably selected, aiming to provide a better homogeneity in the sample illumination where the Pt probe electrode would be acting. In addition, IR heating is minimized.

3. Structural and optical properties

Previously published [26] X-ray diffraction analyses showed hexagonal crystalline phase formation with a wurtzite ZnO structure where the films grew preferably along the axis *c* perpendicular to the substrate in direction (002). No phases corresponding to Al were identified, indicating possible incorporation of Al^{3+} ions in place of Zn^{2+} without altering the structure. This agreed with the results of RBS, confirming the structure ITO/ZnO/ZnO-Al [26, 27]. The nonidentification of crystalline phases of Al may be relevant for the construction of a device in which the insertion of the metal ion may favor the electric conduction without reducing the transparency and enabling the memristive behavior.

The transmittance and absorbance spectra are shown in **Figure 1a** and **b**. The transmittance of the glass is given for reference only. The glass/ITO substrate presents an average transmittance, in the visible region, of 90%, while the ZA1, ZA2, and ZA3 films show transmittance of ~88, 80, and 79.8%, respectively, and have absorption bands at wavelengths of 350–650 nm. This indicates that the investigated thin films exhibit excellent optical properties in the visible and near-infrared region and are semiconductors suitable for applications in electronic devices [28].

The values of the optical bandgap (E_g) were estimated using the Tauc relation in Eq. (1) [29]:

$$(\alpha h\nu)^2 = A\left(h\nu - E_g\right)^n \quad (1)$$

where A is a constant, α is the absorption coefficient, ν is the frequency of incident photons, h is the Planck constant, and E_g is the optical bandgap, which is associated with direct (n = 2) and direct (n = 1/2) transitions [28]. Adjustment was performed by linear extrapolation $(\alpha h\nu)^2 = 0$, and the graph was plotted with relation to $(\alpha h\nu)^2$ vs. E. The bandgap energy values of the samples are shown in **Figure 2** and **Table 1**. The bandgap energy obtained for the pure ITO was 3.75 eV, and the deposited films ZA1, ZA2, and ZA3 are in the range of 3.26, 3.23, and 3.19 eV, respectively. The bandgap reported in the literature for ZnO, Al-doped ZnO, and ITO is ~3.37, 3.28, and 4.2 eV, respectively [30–33]. It is important to note that in the ITO/ZnO/ZnO-Al thin films, an increase of the bandgap energy is observed with the increased thickness of the ZnO layer. This behavior depends on some process parameters such as crystallinity, grain size, and charge carrier density, which significantly affect bandgap energy [32, 34]. However, it is believed that for a greater thickness of the ZnO layer (Al poor region), the proportional number of defects that create traps between the valence band (VB) and the conduction band (CB) is smaller, resulting

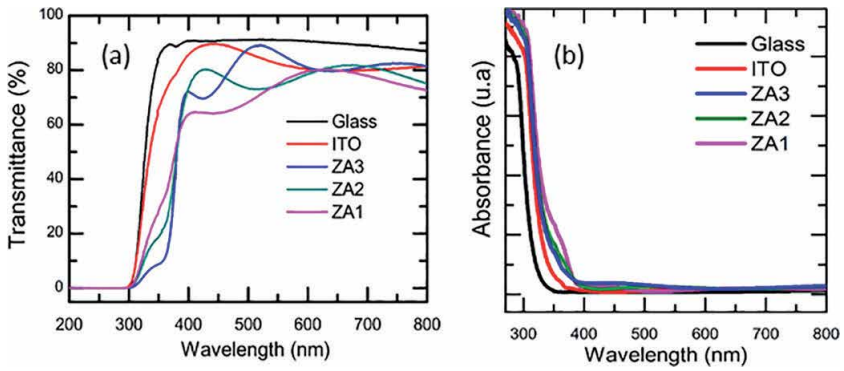

Figure 1.
(a) Transmittance and (b) absorbance spectra for ZA1, ZA2, ZA3 (ITO/glass substrate contributions were removed), ITO, and glass.

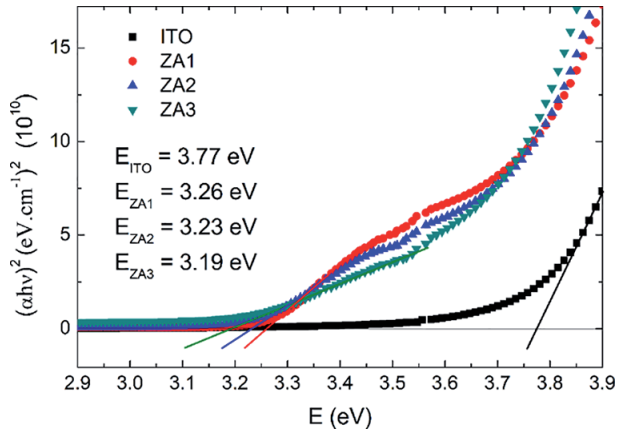

Figure 2.
Plots of $(\alpha h\nu)^2$ vs. energy of all ZnO/ZnO-Al and ITO substrates.

Thin film	Time deposition ZnO layer (min)	Thickness (nm)	Bandgap (eV)
ITO	—	100	3.77
ZA1	100	150	3.26
ZA2	60	110	3.23
ZA3	40	90	3.19

Table 1.
Optical properties of thin films of ITO/ZnO/AZO.

in a higher bandgap energy. However, for low ZnO thicknesses, the influence of the Al-rich region becomes relevant. Therefore, the number of energy levels between the VB and CB is higher, resulting in a lower average bandgap energy value. It is important to note that defects caused by the presence of Al metal forming an Al-rich ZnO (ZnO-Al) region, which may create energy levels within the bandgap, increase the availability of charge carriers over the sample when the photons impinge, thus reducing the electrical resistance.

4. Memristor behavior under dark and illumination

The memristor behavior as a function of the incidence violet light is presented in **Figure 3a**, where voltage sweeps between 0 and 2 V occurred five times and then five other sweeps between 0 and −5 V. The first five sweeps for the positive voltage polarity with the five negative polarity sweeps were performed under illumination of the violet LED (Illumination 1). Then, the same sweeping scheme was imposed on the sample; however, without ambient light (dark 1), the dark chamber was used to provide this situation. In total, the same sample was subjected to 10 alternating sweeps between illumination and dark. Observing specifically the first sweep under illumination, an adaptive-like response was found, in which the maximum value of the measured current intensity gradually increased, indicating that the electrical resistance of the sample decreases as the sweep occurs. This type of behavior is widely known in the scientific literature as the fingerprint of a memristor, where a

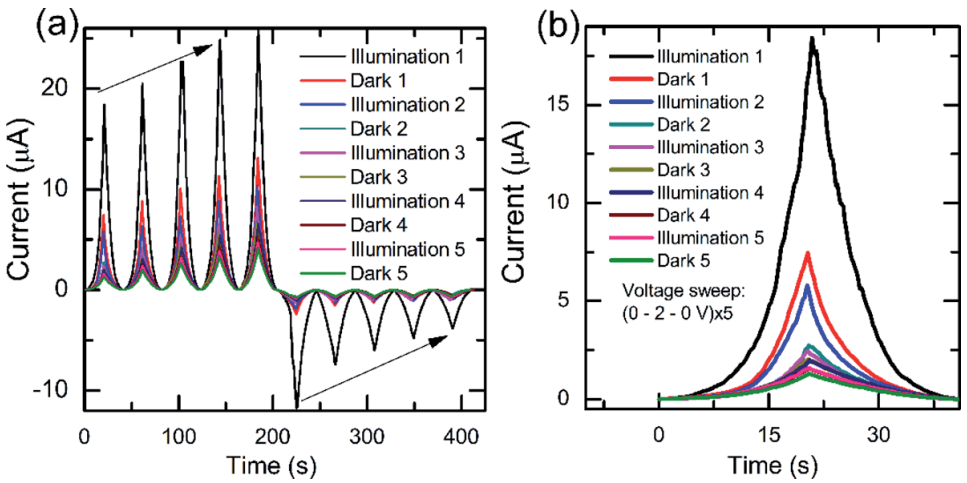

Figure 3.
(a) I–V characteristic curves of the ZA1 sample under continuous voltage scans (0 – 2 – 0 V) × 5 – (0 – (−2) – 0 V) × 5 under violet LED illumination and under darkness and (b) highlight of the first sweep cycles (0 – 2 – 0 V) × 5 under illumination and darkness.

device constructed in the form of metal-insulator (semiconductor)-metal presents electrical resistance dependent on the history of excitation by the application of an external electric field [1, 7, 26, 35].

The gradual conductivity increasing with the application of voltage is a desirable aspect related to memristors, as the memory effect associated to these devices is based on a change in the resistance state, usually a higher resistive state R_{OFF} and lower resistive states, reaching a minimum resistance level at R_{ON} [5, 8, 36]. Computational logic states are, therefore, associated with these two values of electrical resistance (bit 0—R_{OFF}; bit 1—R_{ON}). However, in this type of application, the memristors commonly present filamentary resistive switching mechanisms, where a conductive filament is formed by connecting one electrode to another [5, 6, 37]. The samples analyzed in this chapter are mechanisms based on a homogeneous resistive switching, in which electrical resistance states are gradually modified and controlled [26, 36, 38]. In this type of homogeneous resistive switching, it is possible to note an adaptive character to the applied electric voltage in which the state of resistance at a given instant depends on the entire history of the voltage sweep. Jo et al. presented a very interesting aspect of adaptation to the voltage in memristors of Si/Si + Ag thin films which behaved in a way similar to biological synaptic neurons, in other words, a neuromorphic behavior [7]. The samples worked in this chapter presented results of adaptation to voltage sweep very similar to Si/Si + Ag thin films; however, this work focused on the influence of violet LED light on memristive behaviors.

It is interesting to note that the sample showed a behavior of gradually increasing conductivity under illumination and darkness in all the sweeps. In addition, in the negative polarity, the reverse effect of decreasing conductivity was observed. These behaviors as memristors are explained in materials such as ZnO/ZnO-Ag, ZnO/ZnO-Al, or WO_3/Ag by ionic migrations through the insulating lattice [7, 26, 39]. As theoretically demonstrated by Strukov et al. [36], initially, a device with thickness D (distance between electrodes) presents maximum resistance R_{off}; however, the device may be constructed with a dopant-rich region that can continuously modulate the total resistance between R_{off} and R_{on} through ionic migrations. The control of the ionic migrations and, therefore, the resistance values reached by the device can be obtained with the application of electric voltage $V(t)$. The boundary separating the dopant-rich region from the poor region moves as a function of the applied voltage, which can cause diffusion of the ions, and the normalized position ($w(t)$) of this boundary can have values assigned between 0 and 1, where 0 refers to the case where the resistance is maximal (R_{off}) and 1 to the minimum resistance (R_{on}). Previous work has already shown that this typical behavior of the current in a memristor can be characterized as Eq. (2):

$$I(t) = \frac{1}{R_{on}w(t) + R_{off}(1 - w(t))}V(t) \tag{2}$$

where a pinched hysteresis loop can be obtained [1, 7, 26, 36, 40].

Characteristic I-V curves for different voltage frequencies were published previously in [26]; when voltage excitation frequency is diminished, the step between one conduction state and another is increased. This behavior is typical of memristor and was theoretically predicted by Chua [1] which showed that as the excitation frequency tends to infinity, the area under the I-V curve tends to zero: the effect of adaptation to the excitation is decreased dramatically. On the other hand, when the frequency is reduced, the mechanism of adaptation is evidenced. The work presented in this chapter used a fixed frequency of 5 Hz (or 200 ms excitation period) in all sweeps and samples; on this frequency, an adaptive behavior was very well observed.

The *I-V* characteristic curves under illumination present higher current values under the same voltage sweep than the dark response (see **Figure 3b**). This result indicates that the incidence of photons can significantly alter the number of free charge carriers in the CB, favoring the decrease of the electrical resistance. In this case, electrons trapped at energy levels between the VB and CB are excited due to the incidence of photons, increasing the electron population in the CB, which reduces the electrical resistance, a fact evidenced also in the bandgap values of these samples. However, as new voltage sweeps occur alternately between illumination and darkness (Illumination 1 → Dark 1 → Illumination 2 → Dark 2 → ...→Dark 5), a gradual increase in resistance is observed (decrease of the current intensity generated by the same voltage scanning interval). When the first sweep is initiated, the ion diffusion

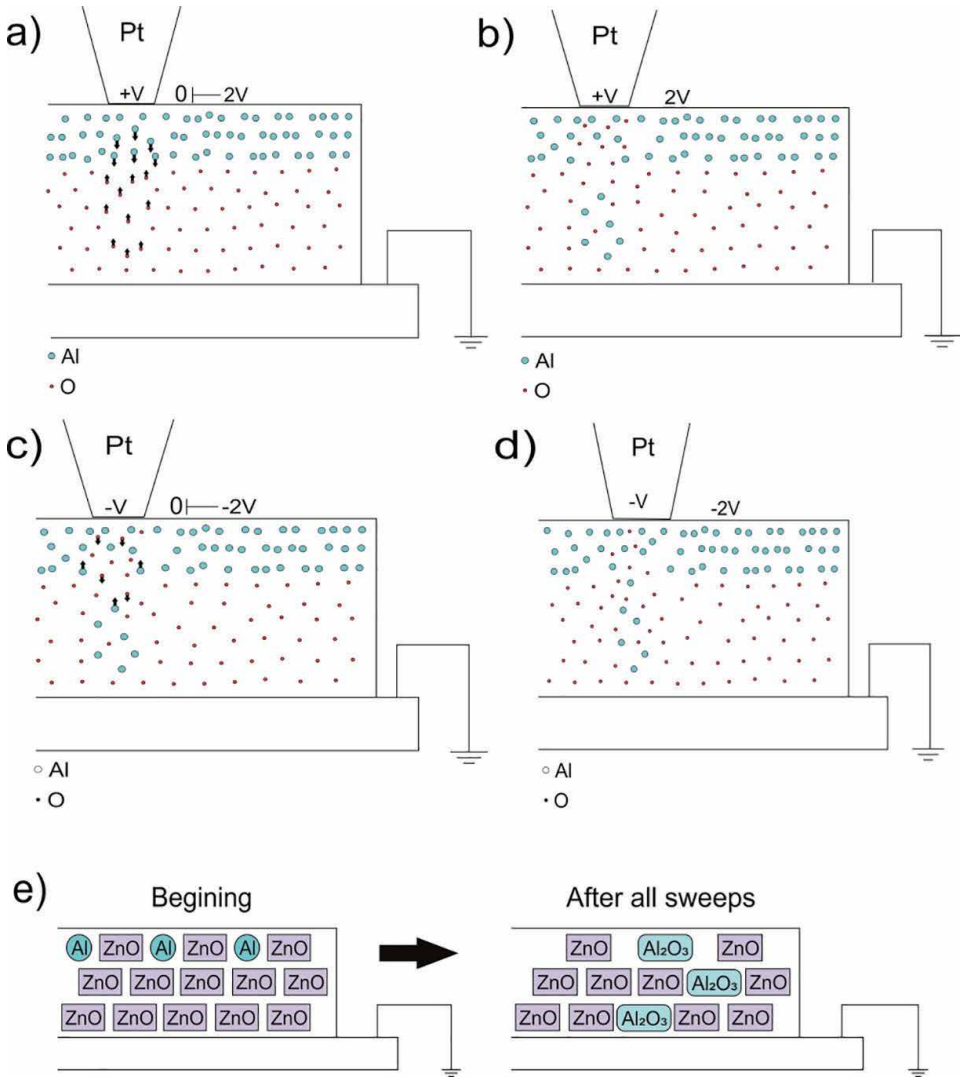

Figure 4.
Diffusion scheme of Al and oxygen dopant ions: (a) initially the Al ions are mostly in the Al-rich region, but, when the voltage sweep is initiated, Al and O ions migrate simultaneously in opposite directions; (b) after the first five sweep for positive polarity, a higher distribution of Al can be directed to the ZnO network, and oxygen ions can be allocated in the Al-rich region; (c) and (d) possible combinations of ions O with Al or Zn ions may prevent new migrations when the polarity is reversed, which indicates a formation of Al_2O_3 oxides in addition to the present ZnO; (e) ZnO and Al distribution scheme before voltage sweeps; and (f) scheme of ZnO and Al_2O_3 oxide distribution after all sweeps.

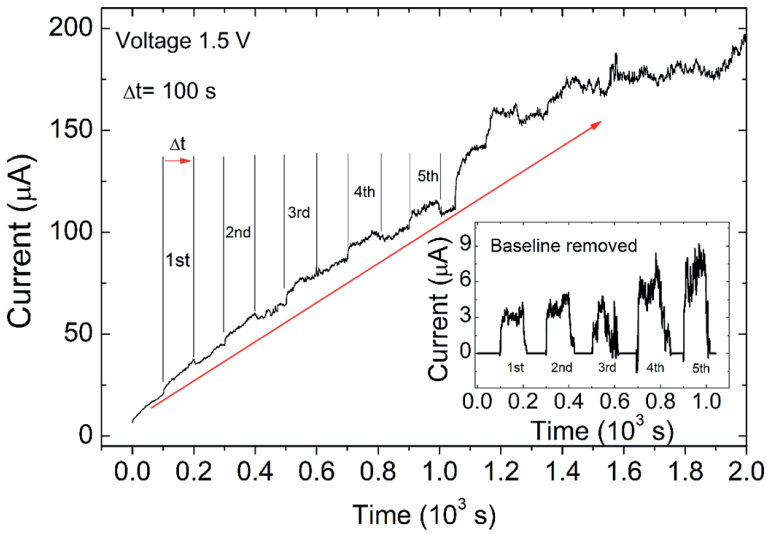

Figure 5.
Current as a function of time for a fixed voltage of 1.5 V: the red arrow indicates the direction of growth of the characteristic resistive switching current, and the violet LED light was set to oscillate between on and off at intervals Δt = 100 s; the first five light exposures are emphasized in the curve (inset: first five violet light exposures in which the baseline was removed).

process occurs, causing a distribution of Al^{3+} and O^{2-} along the entire crystalline network of the sample in a way where simultaneous migrations of Al and O ions (or oxygen vacancies) are realized. This distribution of ion dopants to the ZnO network facilitates electronic conduction, which results in the gradual decrease of the resistance, a fact known as homogeneous resistive switching [26, 38]. However, after several sweeps for positive and negative polarity, the distribution of Al and O ions enables the formation of Al_2O_3 oxide in addition to the existing ZnO network, where this fact may result in the gradual increase of the resistance after each set of voltage sweeps. **Figure 4** illustrates this ion diffusion scheme throughout the sample. Similar results were observed for samples ZA2 and ZA3 (not shown in this work).

Figure 5 shows a curve of the electric current intensity measured through the sample ZA1 as a function of the time for application of a constant voltage of 1.5 V. In each 100 s, the violet LED oscillated between on and off, where it was possible to perceive the sample response as a sensor of violet light by increasing the current intensity when illuminated for 100 s. This result is interesting because it demonstrates two simultaneous responses. The first is a homogeneous resistive switching response that indicates an adaptive process of the sample because there is no variation of the applied voltage modulus, and a gradual increase of current is observed. In addition, this memristor-like behavior is affected when the LED light is on. The first five illuminations in the sample are indicated in the inset of **Figure 5**, where the baseline has been removed. Considering that the incidence of photons in the sample can promote trapped charge carriers in the network to the CB, the amount of charge generated in the first five incidences of violet light was calculated knowing that $q = \int I dt$. The calculated electric charges were, respectively, 320.4, 420.0, 242.1, and 650.9 μC.

5. Conclusions

The ZnO/ZnO-Al thin films with memristor behavior showed a transparency of 88% in the visible region for a thickness of 150 nm, which makes it a relevant candidate in transparent electronics. The bandgap values were determined through the

optical absorption spectrum where the values are between 3.19 and 3.26 eV, similar to values in the literature for this type of material. The ZnO/ZnO-Al thin films' memristive behaviors were observed under the incidence of violet light and under darkness for cycles of voltage sweeps in which an adaptive character can be inferred. The incidence of light favored the increase of the number of carriers, but it did not impede the ion migration to form Al_2O_3 and ZnO oxides throughout the sample, a fact that gradually increased the resistance of the device. The memristor behavior was explained by the diffusion of Al ions that facilitated the electric conduction mechanism between illumination and dark conditions; however, for several voltage sweep cycles, the formation of oxides resulted in the reverse effect, increasing the resistance. Testing as a violet light sensor indicated the generation of electrical charges in the sample network while an adaptive behavior characteristic of the memristor occurred. In other words, two simultaneous phenomena were observed, in which the ZnO/ZnO-Al memristor was influenced by violet light, increasing the conductivity, at the time when it had homogeneous resistive switching due to the electric voltage. These results indicate a scientific advance in the area of resistive switching with the observation of ZnO/ZnO-Al memristive behavior dependent on the voltage application history and the ambient light conditions. In addition, new insight is provided for future research related to optical effects on memristor behaviors.

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Conflict of interest

There is no conflict of interest.

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Chapter 7

Application of Probe Nanotechnologies for Memristor Structures Formation and Characterization

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Abstract

This chapter presents the results of experimental studies of the formation and investigation of the memristors by probe nanotechnologies. This chapter also perspectives and possibilities of application of local anodic oxidation and scratching probe nanolithography for the manufacture of memristors based on titanium oxide structures, nanocrystalline ZnO thin film, and vertically aligned carbon nanotubes. Memristive properties of vertically aligned carbon nanotubes, titanium oxide, and ZnO nanostructures were investigated by scanning probe microscopy methods. It is shown that nanocrystalline ZnO films manifest a stable memristor effect slightly dependent on its morphology. Titanium oxide nanoscale structures of different thicknesses obtained by local anodic oxidation demonstrate a memristive effect without the need to perform any additional electroforming operations. This experimentally confirmed the memristive switching of a two-electrode structure based on a vertically aligned carbon nanotube. These results can be used in the development of designs and technological processes of resistive random access memory (ReRAM) units based on the memristor devices.

Keywords: nanotechnology, scanning probe microscopy, memristor, titanium oxide, nanocrystalline ZnO films, carbon nanotubes

1. Introduction

Reducing the elements of integrated circuits (ICs) leads to an increase in the speed of the processors and an increase in the amount of memory, but at the same time the bandwidth between them varies only slightly. This is referred as the von Neumann bottleneck and often limits the performance of the system [1]. One possible solution to this problem is the transition of computing systems to an architecture close to the structure of a biological brain, which is a set of elements of low power connected in parallel neurons interconnected via special channels synapses [1–4]. Processors built on this architecture have concurrent computing and will be able to surpass modern computers in tasks related to unstructured data classification, pattern recognition, as well as in applications with adaptable and self-learning

control systems. One of the possible ways of implementing such an architecture is to manufacture ICs based on neuromorphic structures, which are memory elements in the form of cells (neurons) interconnected by data buses (synapses) and are capable of changing their electrical resistance under the influence of an external electric field (the effect of resistive switch) [1–5]. Such structures can maintain cell resistance after the termination of the external electric field and are the basis of non-volatile resistive memory (ReRAM). The advantages of ReRAM include small size, high degree of integration, low power consumption, and high speed, which allows on its basis to realize the mass parallelism and low power calculations observed in the study of biological brain [6–8].

Currently, active theoretical and experimental studies of the effect of resistive switching in nanomaterials and nanostructures are underway to create elements of the ReRAM self-learning adaptive neuromorphic processor with high speed and low power consumption. An analysis of the publications showed that for the manufacture of ReRAM, films based on binary metal oxides (SiO_x, TiO_2, ZnO, HfO_x, etc.) are promising from which amorphous titanium oxide and nanocrystalline zinc oxide can be distinguished, allowing for high response speed of the resistive switching process [8–10].

The creation of ReRAM elements for a neuromorphic processor is associated with the development and research of the formation processes of structures with a nanometer resolution. Existing lithographic methods of semiconductor technologies are approaching the limit of their resolution, characterized by a high degree of complexity and cost of equipment. Therefore, there is a need for research and development of new methods, the use of which will allow the creation of nanostructures of ReRAM elements, including at the prototyping stage.

One possible way of ReRAM elements prototyping is probe nanotechnologies usage, which is a combination of methods for nanostructures forming using a probe tip with visualization and process control in situ. Promising methods of probe nanotechnologies for ReRAM elements prototyping include local anodic oxidation (LAO) and scanning probe nanolithography (SPN) of atomic force microscope.

The method of local anodic oxidation is promising for the manufacture of oxide nanostructures (ONS) of titanium, which have reproducible memristor effect and do not require forming [11–14]. The advantages of the LAO method also include precision, the possibility of conducting research on electrochemical processes in local areas up to the size of several nanometers in situ diagnostics of the results of the formation of ONS on the substrate surface, the absence of additional technological operations for applying, exposing, and removing photoresist, as well as the relatively low cost of process equipment [15–20]. A variety of nanoimprint lithography is scratching probe nanolithography, which allows using the tip of an atomic force microscope probe to form profiled nanostructures in polymer films [21]. The simplicity of the method implementation allows using it in the development and study of promising design and technological solutions for prototyping ReRAM elements [22].

At the present stage of nanotechnology development, one of the most promising methods for surface diagnostics is scanning probe microscopy (SPM). The use of SPM methods allows the study of the local geometric, electrical, and mechanical properties of the sample surface [23–26].

Of interest for creating ReRAM with high cell density are memristor structures based on vertically aligned carbon nanotubes (VA CNTs) [27, 28]. The vertical orientation of the nanotubes provides a significant reduction in the memory cell area and the technology of producing VA CNTs based on the method of plasma-enhanced chemical vapor deposition (PECVD) allows localized growth of nanotubes in a process compatible with silicon technology [29, 30]. In addition, the use of VA CNTs as a storage element is expected to reduce the switching time to picoseconds [28, 31].

A promising method of probe nanotechnologies for creation and characterization of memristor structures based on VA CNTs is the scanning tunneling microscopy (STM) [26]. This method allows you to create a controlled elastic deformation in VA CNT, the presence of which is a prerequisite for the occurrence of the memristor effect in VA CNT [32]. The mechanism of memristive switching of strained carbon nanotube is described in detail in [28].

This chapter describes application of scanning probe microscopy techniques for determination of resistive switching effects in vertically aligned carbon nanotubes, TiO_2 nanostructures, and ZnO thin nanocrystalline films. Described techniques can be used for formation and nanodiagnostics of parameters of memristor structures for creation of metal oxide and CNT-based neuromorphic system.

2. Formation and investigation of memristor structures based on titanium oxide by atomic force microscopy

2.1 Investigation of resistive switching of titanium oxide nanostructures formed by local anodic oxidation

The memristor effect study was carried out on titanium oxide nanostructures (ONS) using AFM spectroscopy using SPM Solver P47 Pro. For this purpose, local anodic oxidation (LAO) was carried out on the thin titanium film surface with a 20 nm thickness, and as a result, titanium ONS was formed with lateral dimensions 1 × 1 μm and 1.1 nm thick (**Figure 1**).

Then, using the AFM, the current-voltage (I-V) characteristics of the obtained structure were measured according to the scheme shown in **Figure 1c** with the application of a triangular-shaped voltage pulse (**Figure 2a** inset). It was shown that the titanium ONS obtained by the LAO exhibits a bipolar resistive switching effect (**Figure 2**) without additional doping and electroforming operations.

The analysis showed that the current-voltage characteristic type corresponds to the switching mechanism due to potential barrier width modulation at the

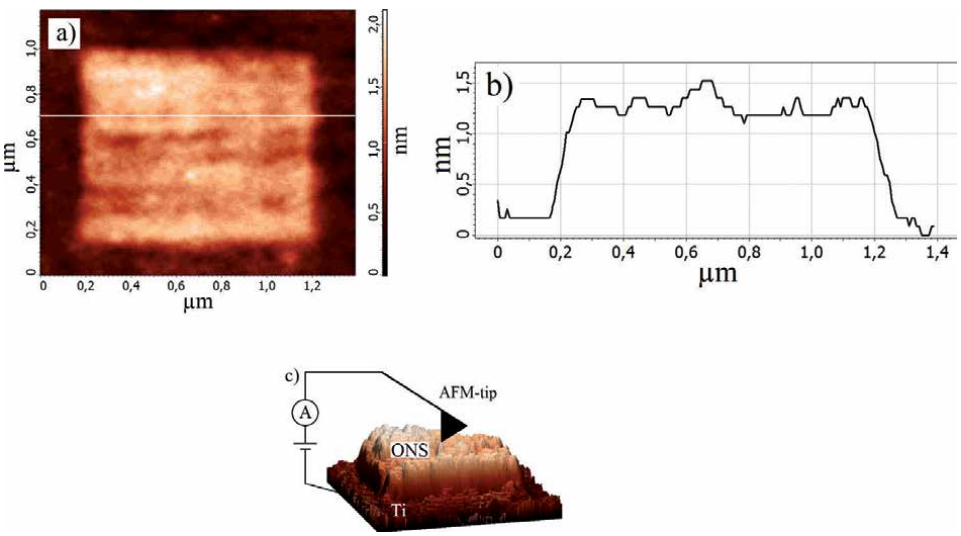

Figure 1.
Titanium oxide nanostructures, formed by LAO: (a) AFM image; (b) profilogram along the line; and (c) current-voltage characteristics measuring scheme.

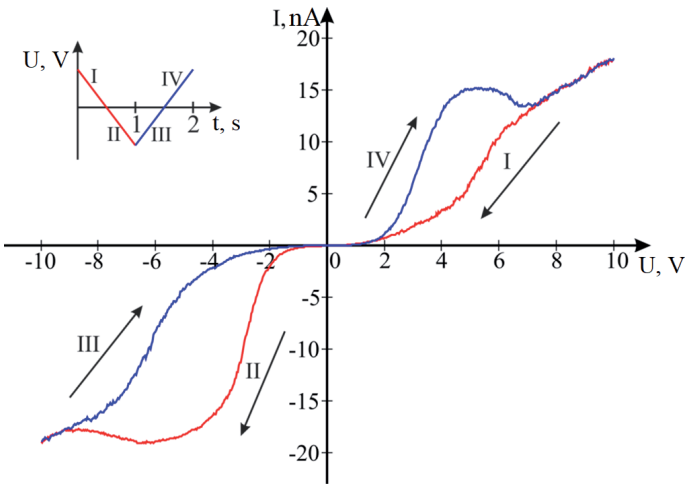

Figure 2.
Current-voltage characteristic of titanium ONS, formed by the LAO.

electrode/oxide interface described in [11, 12]. In this case, the potential barrier modulation occurs alternately at both the electrodes boundaries.

Initially, the structure is in high resistance state (HRS) (1.3 GΩ at 3.5 V) in the forward bias region (region I in **Figure 2**), while at a negative voltage applied to −5 V, the structure is in low resistance state (LRS) (0.27 GΩ at −3 V) (region II in **Figure 2**). Then, as the voltage rises in the reverse bias region from −6 to −10 V, the structure is switched, resulting in a HRS state (3.4 GΩ at −3 V) at the reverse bias (region III in **Figure 2**) and LRS (0.35 GΩ at 3.5 V) at up to 5 V direct bias (region IV in **Figure 2**). With an increase in the applied voltage from 6 to 10 V, the structure is switched to the initial state. In this case, the structure resistance ratio in the HRS state to the LRS state for positive voltages is 3.6, and for negative voltages is 12.6.

2.2 Investigation of influence of AFM probe pressing force on the resistive switching in titanium oxide nanostructures

For the experimental study, titanium ONS with 2 × 2 μm lateral dimensions and 6.8 nm thick was formed by LAO. Then, on its surface in the AFM contact mode was performed a spectroscopic measurement of dependence of the feedback circuit current on the cantilever beam bending. The spectrogram showed that with an increase in the feedback circuit current by 1.02 nA, the beam is bent by 20.8 nm. Since the cantilever beam stiffness is 2.5 N/m, it is possible to calculate the AFM probe pressing force to the ONS surface for a given feedback circuit current **Figure 3**.

Then, current-voltage characteristics were measured on the ONS surface in the ±10 V range with the AFM feedback circuit current values from 0.01 to 2 nA (**Figure 4**), after which the structure resistance values in the HRS and LRS states were measured at 3.5 V.

Obtained dependences analysis showed that an increase in the AFM probe clamping force to the surface from 0.51 to 102.8 nN leads to a decrease in the structure resistance in the HRS state from 1.12×10^{11} to 9.63×10^{9} Ω and in the LRS state from 2.28×10^{10} to 1.38×10^{9} Ω.

This dependence can be explained by the fact that with a clamping force increase, an increase in the contact area between the AFM probe and the oxide

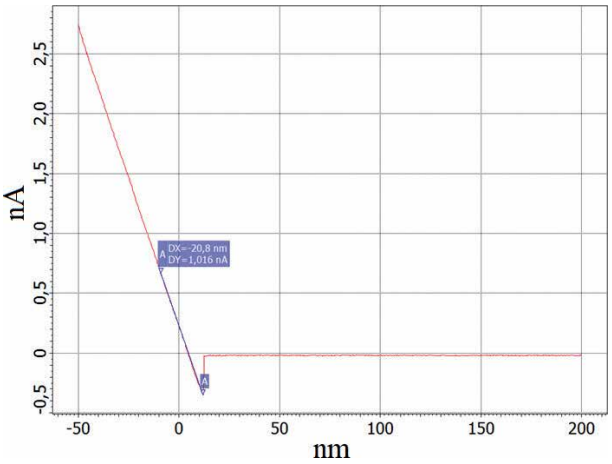

Figure 3.
Dependence of feedback circuit current from the cantilever beam bending.

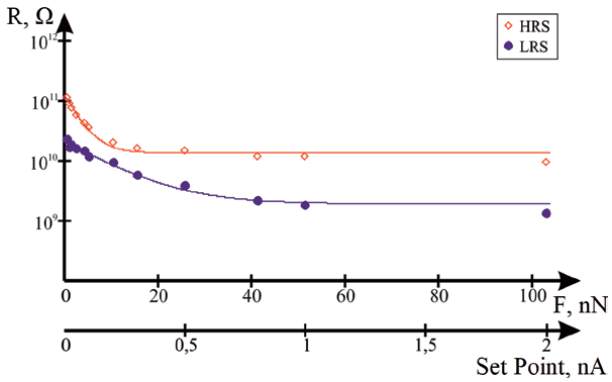

Figure 4.
Dependence of titanium ONS resistance in the HRS and LRS states on the pressing force.

surface occurs. In further studies, 60 nN clamping force was used, ensuring reliable contact of the probe with the structure.

2.3 Investigation of influence of top electrode materials on the resistive switching in titanium oxide nanostructures

Literature analysis showed that the top electrode material has a significant impact on the resistive switching of memristor structures. To study this effect, the current-voltage characteristics were measured in the mode of current AFM spectroscopy on the surface of oxide nanostructures formed by the LAO method; AFM probes with different conducting coating were used as the upper electrode. The resulting characteristics are presented on (**Figure 5**).

Obtained dependences analysis showed that the use of cantilevers with different coatings significantly affects the manifested memristor effect. So, when using a cantilever with a Pt coating, a symmetrical I-V characteristic was obtained (**Figure 5a**) with low current values, the structure resistance in the HRS state is 327×10^9 Ω, and in the LRS state is 22×10^9 Ω, while the resistance ratio in the high resistance to low resistance is 15.

When using a cantilever with a TiN coating, an asymmetric I-V characteristic was obtained (**Figure 5b**), while in the negative voltage region the memristor effect

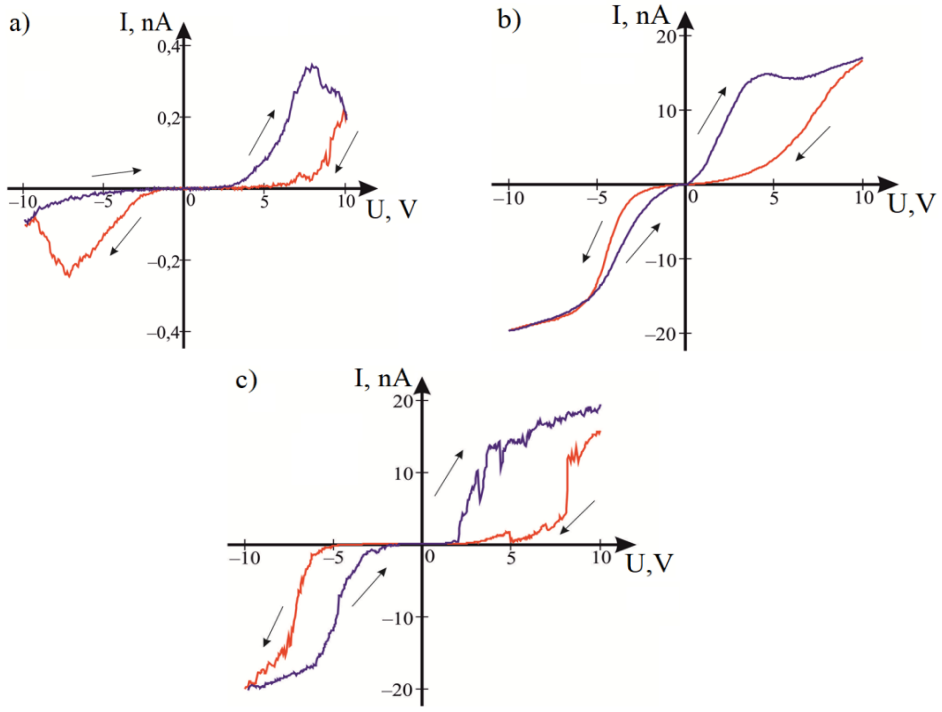

Figure 5.
Titanium ONS current-voltage characteristics, obtained using a cantilever coated by: (a) Pt; (b) TiN; and (c) carbon.

is insignificant, the structure's resistance in the HRS state is 4.65×10^9 Ω, and in the LRS state -0.39×10^9 Ω, at the same time, resistance ratio in the high resistance to low resistance is 12. In the case of using a carbon-coated cantilever, an asymmetric I-V characteristic is also observed (**Figure 5c**), and there is no current through the ONS when applying voltages less than ±5 V in the case of a structure being in HRS and applying a voltage less than ±2 V in case of a structure being in LRS. The structure's resistance in the HRS state is 1.74×10^9 Ω, and in the LRS state, it is 0.3×10^9 Ω, and the resistance ratio in the high resistance to low resistance is 6.

Study results showed that the platinum-coated cantilever use as the top electrode is characterized by a largest resistance ratio in the HRS and LRS states.

2.4 Investigation of influence of titanium oxide nanostructures geometric parameters on their resistive switching

Another goal is to study titanium ONS thickness effect and applied voltage pulses on the memristor effect. For this, four ONSs were formed with lateral 2 × 2 μm dimensions and 1.6–3.6 nm height, which, based on the expression describing the oxide height and depth ratio presented in [3], corresponds to 3.6–8.2 nm thickness. The current-voltage characteristics were measured on these structures surface by applying ±2.4 voltage pulse (**Figure 6**).

Obtained expression analysis showed that with an increase in the ONS thickness, a decrease in the current corresponding to the LRS state and an increase in the resistance in this state are observed, to the extent that the memristor effect does not manifest itself when the oxide thickness is 8.2 nm.

The results allowed us to obtain voltage of the switching structure in the HRS state (U_{res}) and in the LRS state (U_{set}) dependence, as well as the corresponding

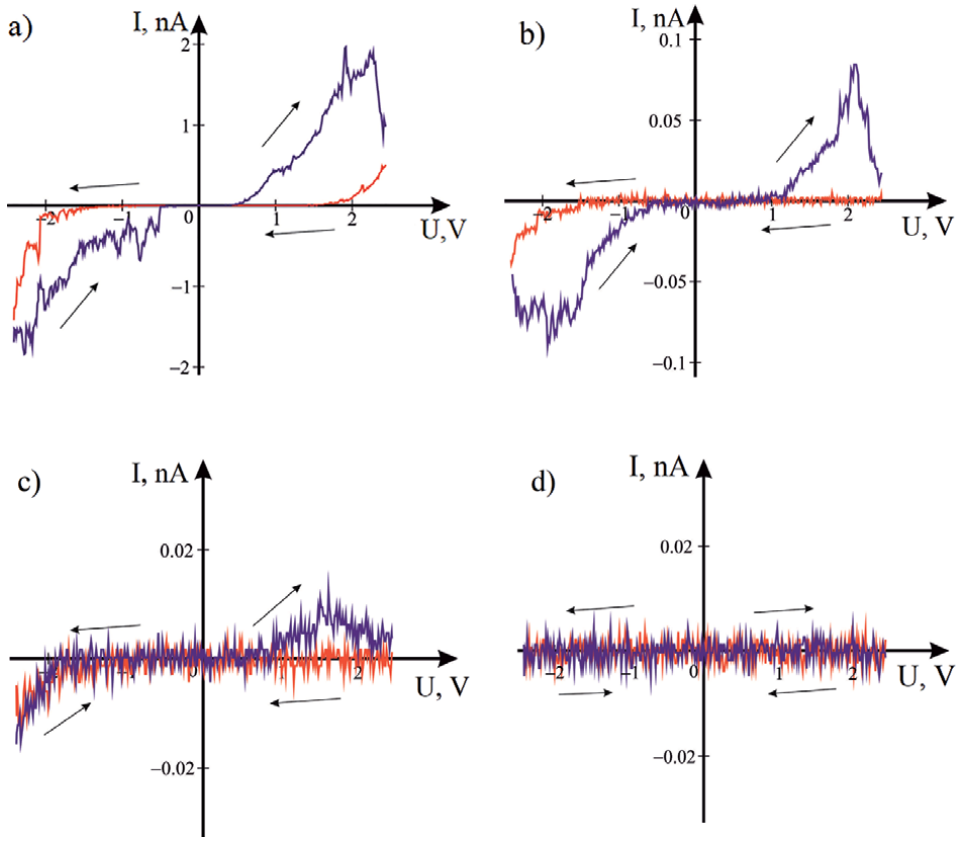

Figure 6.
Titanium ONS current-voltage characteristics with a thickness: (a) 3.6 nm; (b) 5.4 nm; (c) 7.2 nm; and (d) 8.2 nm.

currents (I_{res} and I_{set}) on the titanium ONS thickness (**Figure 7**). In addition, the dependence of the structure resistance measured in a HRS and LRS state on the ONS thickness measured at 1.5 V was obtained (**Figure 8**).

It is shown that increasing the thickness from 3.6 to 8.2 nm increases the resistance in the HRS state from 1.4×10^{11} to 8.8×10^{11} Ω, while the resistance in the LRS state increases from 1.765×10^{9} to 2.4×10^{11} Ω, while the structure resistance ratio in the high resistance to low resistance decreases from 79.4 to 3.6.

2.5 Investigation of influence of voltage pulses amplitude on the titanium oxide nanostructures resistive switching

To study the applied voltage pulses amplitude effect on the memristor effect, an titanium ONS with 2 × 2 μm lateral dimensions and 3.6 nm thickness was formed. Then, its current-voltage characteristic was measured in the voltage range from ±1 to ±4 V (**Figure 9**).

The analysis showed that when measuring the titanium ONS current-voltage characteristics with 3.6 nm thickness in the voltage range ± 1 V, the memristor effect is not observed, the structure shows the conductivity absence. When measuring the I-V characteristic in the ±2 V range, the structure also shows the conductivity absence, however, a small current surge in the I-V characteristic is already observed. When measuring the I-V characteristic in ±3 and ± 4 V range, this structure exhibits a memristor effect. It is shown that in the case of measuring the I-V characteristic in ±3 V range, the structure resistance in the HRS state is 39.2×10^{9} Ω, and in the LRS

state −1.4 × 10^9 Ω, the resistance ratio in the HRS and LRS states is 27.4. In the case of measuring the I-V characteristic in ±4 V range, the structure resistance the in the

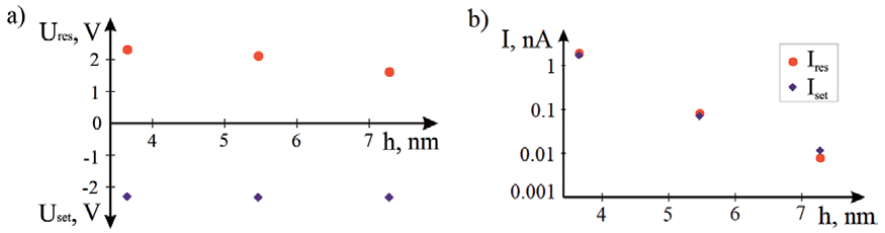

Figure 7.
Dependence of electrical parameters of titanium ONS on the oxide thickness: (a) voltage and (b) current.

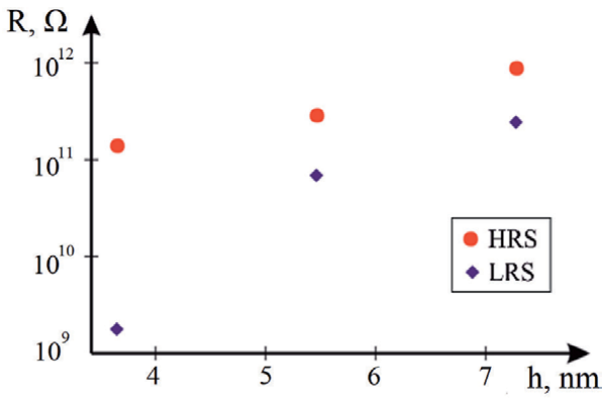

Figure 8.
Dependence of titanium ONS resistance on the thickness.

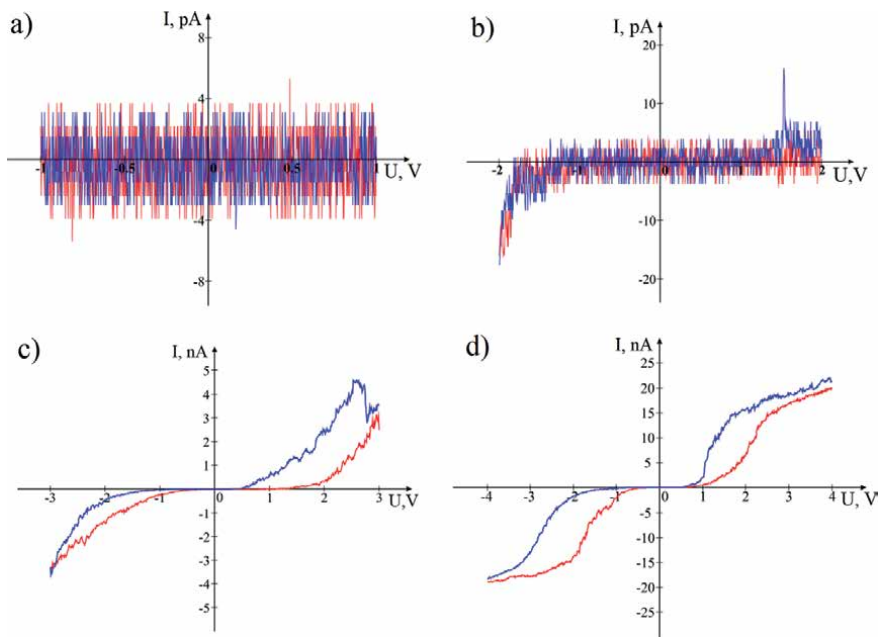

Figure 9.
Current-voltage characteristics of titanium ONS in the different voltage range: (a) ±1 V; (b) ±2 V; (c) ±3 V; and (d) ±4 V.

HRS state is 1.08 × 10^9 Ω, and in the LRS state it is 0.14 × 10^9 Ω, the resistance ratio in the HRS and LRS states is 7.5.

Such a memristor effect dependence on the titanium ONS thickness and the applied voltage pulses amplitude is explained by the electric field intensity influence in the oxide on the oxygen vacancies transfer in the oxide volume between the electrodes and the titanium ONS switching between high-resistance and low-resistance states.

3. Formation and investigation of memristor structures based on nanocrystalline ZnO thin films by atomic force microscopy

3.1 Investigation of resistive switching of nanocrystalline ZnO thin films

A resistive switching effect in thin oxide films is attractive for manufacturing of neuromorphic system, which offers significant advantages over classical computers, such as an effective processing of data recognition. ZnO is the one of the promising materials, which is widely used in electronic element developments, sensors, and microsystem technology. Also, ZnO demonstrates resistive switching, which has just one phase and is compatible with semiconductor technology. To fabricate ZnO-based neuromorphic system, it is necessary to study resistive switching in ZnO films and today there are insufficient experimental results about it.

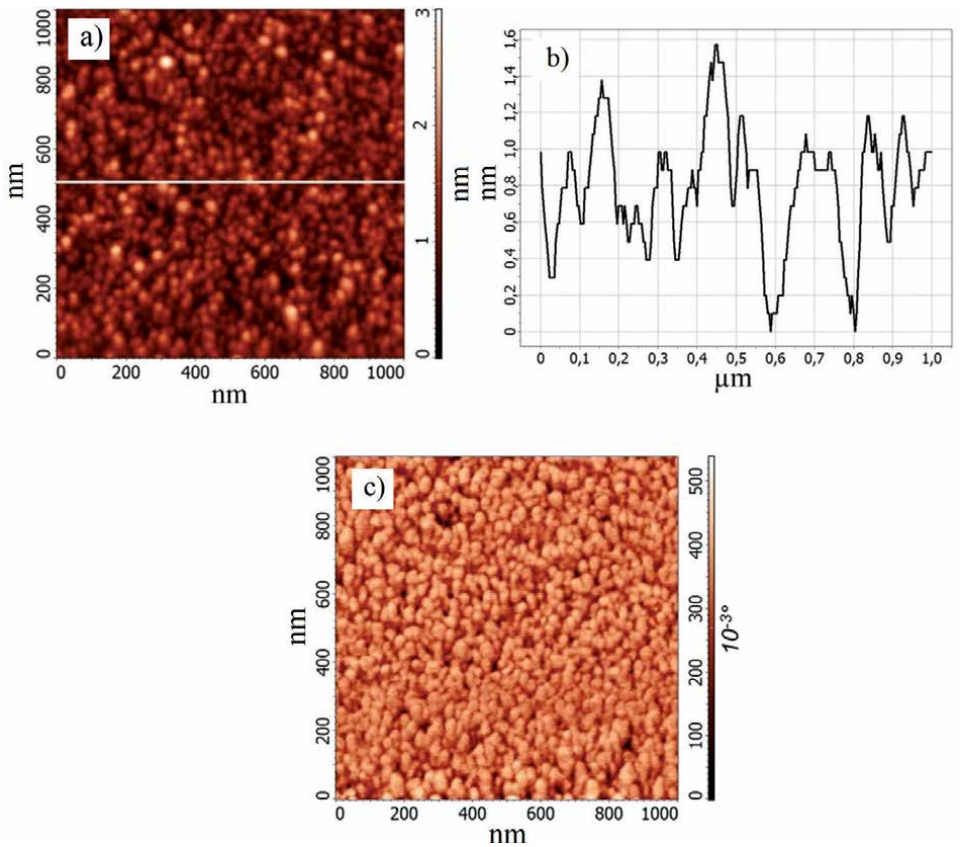

Figure 10.
ZnO film surface: (a) AFM-image; (b) AFM cross-sectional profile on (a); and (c) phase.

To investigate resistive switching Al_2O_3/ZnO:In (42.1 ± 5.6 nm) as a wafer was used. ZnO thin films were grown using pulsed laser deposition under the following conditions: wafer temperature: 400°C, target-wafer distance: 50 mm, O_2 pressure: 1 mTorr, pulse energy: 300 ml. To provide electrical contact to the bottom ZnO:In electrode, ZnO films were deposited through a mask.

Electrical properties of obtained ZnO films were measured by Ecopia HMS-3000 equipment (Ecopia Co., Republic of Korea). Obtained ZnO films had electron concentration 8.4×10^{19} cm^{-3}, electron mobility 12 $cm^2/V{\cdot}s$, and resistivity 5.2×10^{-3} Ω·cm.

AFM-images of the ZnO film surface were obtained in semi-contact mode using scanning probe microscope Solver 47 Pro (NT-MDT, Russia). The AFM-image processing was performed using Image Analysis software. **Figure 10** shows experimental investigations of ZnO film morphology. It is shown that ZnO film surface has a granular structure (**Figure 10a** and **c**) with 1.53 ± 0.27 nm roughness (**Figure 10b**). The ZnO film thickness was measured by ZnO/ZnO:In stair scanning, and was equaled 32.3 ± 7.2 nm.

Electrical measurements were taken using nanolaboratory Ntegra with W_2C probes. During the resistive switching investigation, ZnO:In film was grounded.

Current-voltage curves (CVC) were obtained from −3 to +3 V sweep for 15 cycles at the same point and for 15 cycles at different points on ZnO surface (**Figure 11a**). Based on the results obtained, resistance dependence on cycle number (uniformity test) and resistance dependence on number point were built (homogeneity test). It was shown R_{HRS} and R_{LRS} were equaled to 0.68 ± 0.07 GΩ and 0.11 ± 0.04 GΩ,

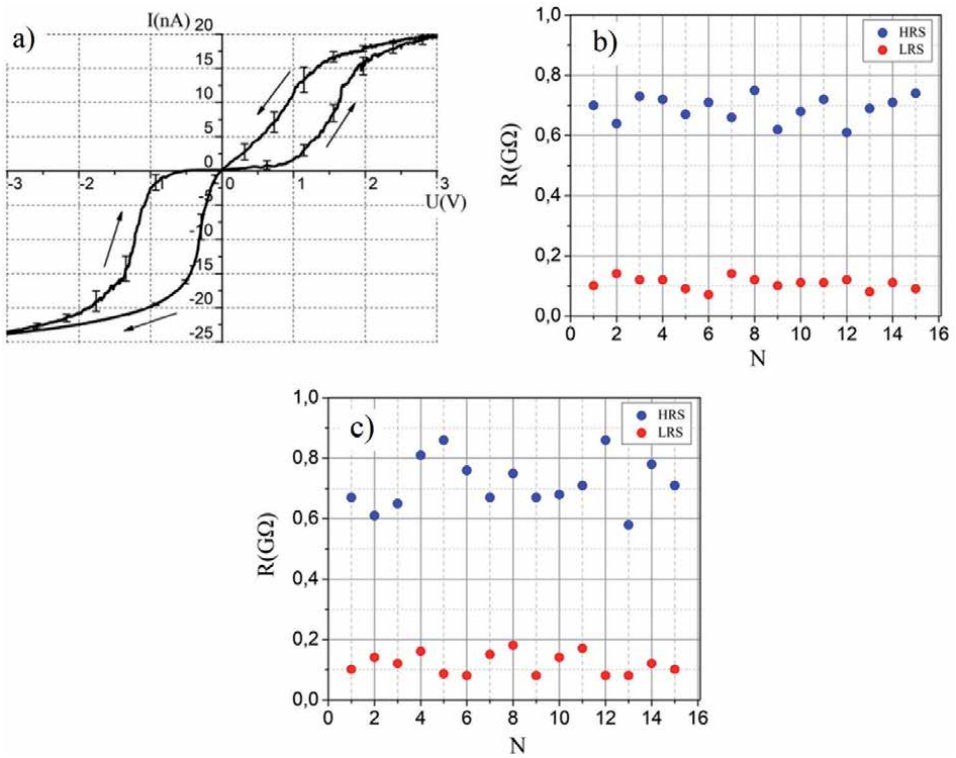

Figure 11.
Investigation of resistive switching in ZnO film: (a) current-voltage characteristic; (b) uniformity; and (c) variability.

respectively at the same point on ZnO surface. At different points, R_{HRS} and R_{LRS} were equaled to 0.75 ± 0.13 GΩ and 0.12 ± 0.06 GΩ. R_{HRS}/R_{LRS} was equaled to 9.05 ± 5.65 at 0.7 V. Resistance dispersion during uniformity test was more than resistance dispersion during homogeneity test that can be explained by a granular structure of ZnO film.

Time stability of resistive switching in ZnO was implemented using Ntegra in two stages. On the first stage, charge structure was formed on the ZnO surface at +5 V (**Figure 12a**). On the second stage, charged structure was scanned in Kelvin mode in the interval from 5 to 30 minutes with a step 5 minute (**Figure 12b** and **c**). It was shown that voltage decreased from 266 ± 17 to 68 ± 7 mV in 30 minutes (**Figure 12a**).

3.2 Investigation of scratching probe nanolithography regimes for memristor structure formation

Resistive switching element manufacturing is associated with the development and research of the formation processes of structures with a nanometer resolution. Existing lithographic methods of semiconductor technologies are approaching the limit of their resolution, characterized by a high degree of complexity and cost of equipment. Therefore, there is a need for research and development of new methods, the use of which will allow the creation of nanostructures of resistive switching elements, including at the prototyping stage. A promising method for the formation of nanoscale structures that can be used to create resistive switching elements is nanoimprint lithography based on the use of special dies and films of polymeric materials. A type of nanoimprint lithography is scratching probe nanolithography

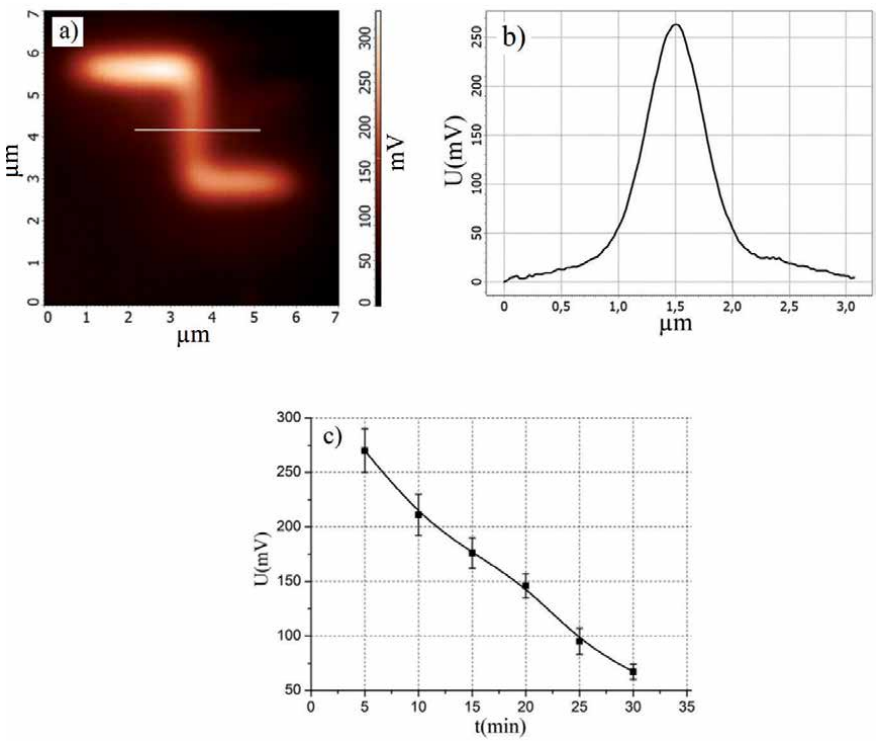

Figure 12.
Investigation of ZnO film surface charge: (a) Kelvin mode image of charged structure; (b) AFM cross-sectional profile on (a); and (c) time dependence of voltage.

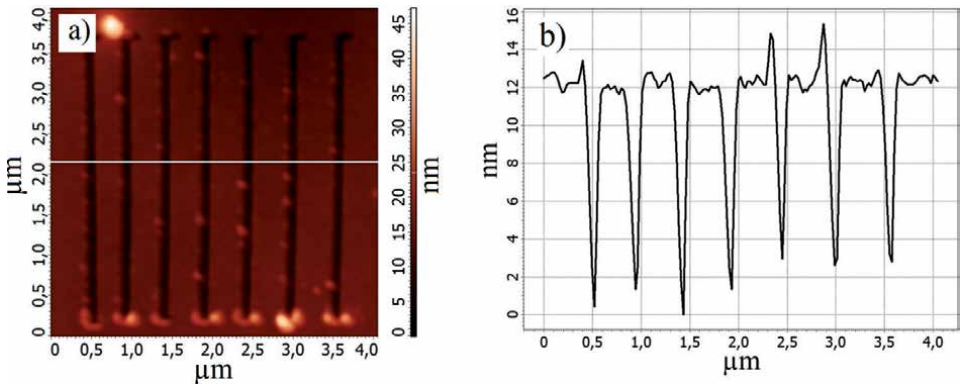

Figure 13.
Profiled nanostructures on photoresist surface: (a)AFM-image; and (b) AFM cross-sectional profile on (a).

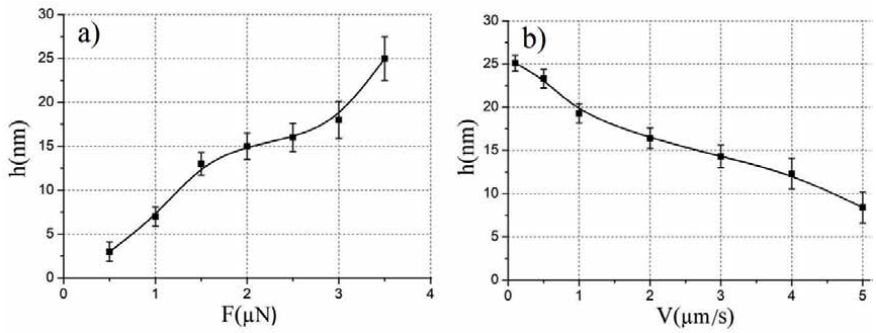

Figure 14.
Investigation of scratching probe nanolithography regimes: (a) force of depth dependence; (b) velocity of depth dependence.

(SPN), which allows using the tip of an atomic force microscope probe to form profiled nano-sized structures in polymer films. It was decided to use photoresist FP-383 as polymer film, because it is cheaper and has longer shelf life compared to other types of polymer films.

The solution of photoresist/thinner (FP-383/RPF383F) at volume ratio of 1:10 was transferred onto Si substrate using the centrifugal method at the rotation speed of a Laurell WS-400B-6NPP centrifuge at 5000 rpm. After the deposition of the film, the photoresist/thinner film was dried at a temperature of 90°C for 25 minutes. Thickness of the photoresist/thinner film was equaled to 32.1 ± 4.7 nm.

Scratching probe nanolithography on the photoresist/thinner film was performed using a Solver P47 Pro scanning probe microscope. Indentation was performed by applying an AFM probe to the surface of a FP-383 film with a fixed clamping force (the Set Point parameter in the AFM control program). Thus, arrays of the seven profiled lines-grooves were formed at different nanoindentation forces (**Figure 13**).

Analysis of the results obtained showed that nanoindentation force increase from 0.5 to 3.5 µN leads to nanostructure-groove depth increase from 2.7 ± 0.8 to 25.31 ± 2.11 nm (**Figure 14a**), tip velocity increase from 0.1 to 5 µm/s leads to nanostructure-groove depth decrease from 25.10 ± 1.2 to 8.87 ± 1.34 nm (**Figure 14b**).

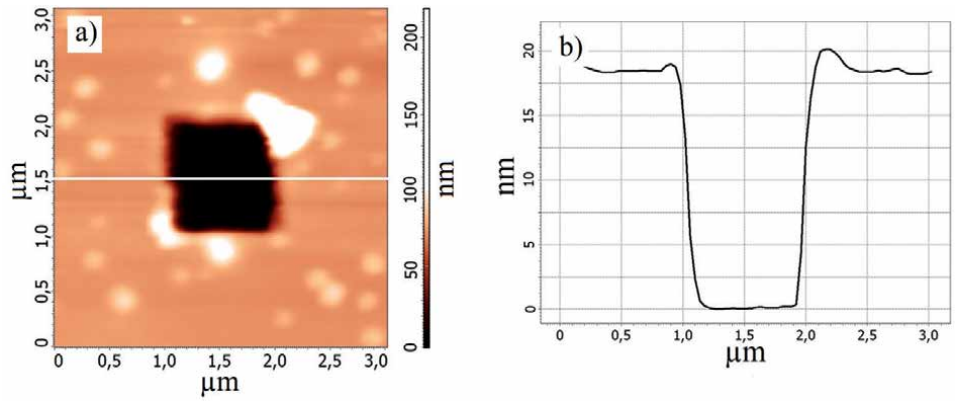

Figure 15.
Profiled nanostructure on FP-383 film surface: (a) AFM-image; and (b) AFM cross-sectional profile on (a).

The nonlinearity of the dependences obtained can be explained by the inhomogeneity of the viscoelastic properties of the FP-383 film. It should also be noted that the nature of the contact interaction between the probe and the film is complex and is largely determined by the elastic forces.

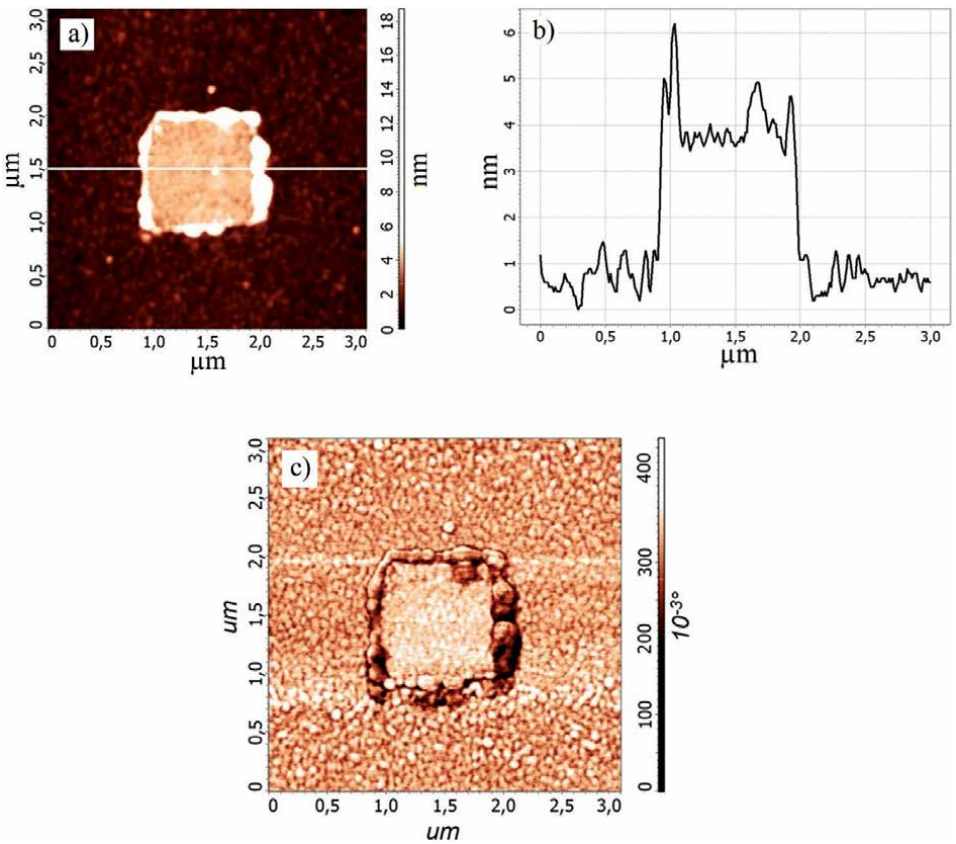

Figure 16.
Resistive switching Al_2O_3/ZnO:In/ZnO/Ti/W_2C memristor structure: (a) AFM-image; (b) AFM cross-sectional profile on (a); and (c) phase.

3.3 Fabrication and investigation of resistive switching of memristor structures based on nanocrystalline ZnO thin films

To fabricate memristor structure, photoresist FP-383 thin film with thickness 21.4 ± 3.1 nm was formed on Al_2O_3/ZnO:In/ZnO substrate. Then squared nanostructure-groove was formed on FP-383 film surface using scratching probe nanolithography at nanoindentation force 3.18 μN (**Figure 15**). Thin Ti film was deposited using BOC Edwards Auto 500 system. After that lift-off process was applied using dimethylformamide. AFM-image of the Al_2O_3/ZnO:In/ZnO/Ti resistive switching structure obtained is shown in **Figure 16**. Analysis of the result obtained showed that Ti film thickness was equaled to 4.1 ± 0.3 nm (**Figure 16b**). Ripped edges of Ti structures are result of lift-off process.

Figure 17 shows current-voltage characteristic of Al_2O_3/ZnO:In/ZnO/Ti/W_2C structure at −4 to +4 voltage sweep. It was shown that Al_2O_3/ZnO:In/ZnO/Ti/W_2C structure has nonlinear, bipolar behavior when the electric potential gradient is the dominant parameter of resistive switching.

Investigation of resistive switching of Al_2O_3/ZnO:In/ZnO/Ti/W_2C structure in the single point (uniformity test) shown that R_{HRS} was 8.23 ± 1.93 GΩ and R_{LRS} was 0.11 ± 0.06 GΩ (**Figure 17b**). At different points, R_{HRS} and R_{LRS} were equaled 7.65 ± 2.83 GΩ and 0.18 ± 0.11 GΩ, respectively (**Figure 17c**). It was shown, that R_{HRS}/R_{LRS} coefficient was equaled 135.31 ± 44.38 at 0.7 V.

In the end, it was shown that the use of Ti film allowed to increase R_{HRS}/R_{LRS} coefficient from 9.05 ± 5.65 to 135.31 ± 44.38 and to decrease the resistance dispersion of resistance switching (**Figures 11** and **17**). It can be explained by exception for the influence of air oxygen in Al_2O_3/ZnO:In/ZnO/Ti structure that significantly worsens the resistive switching.

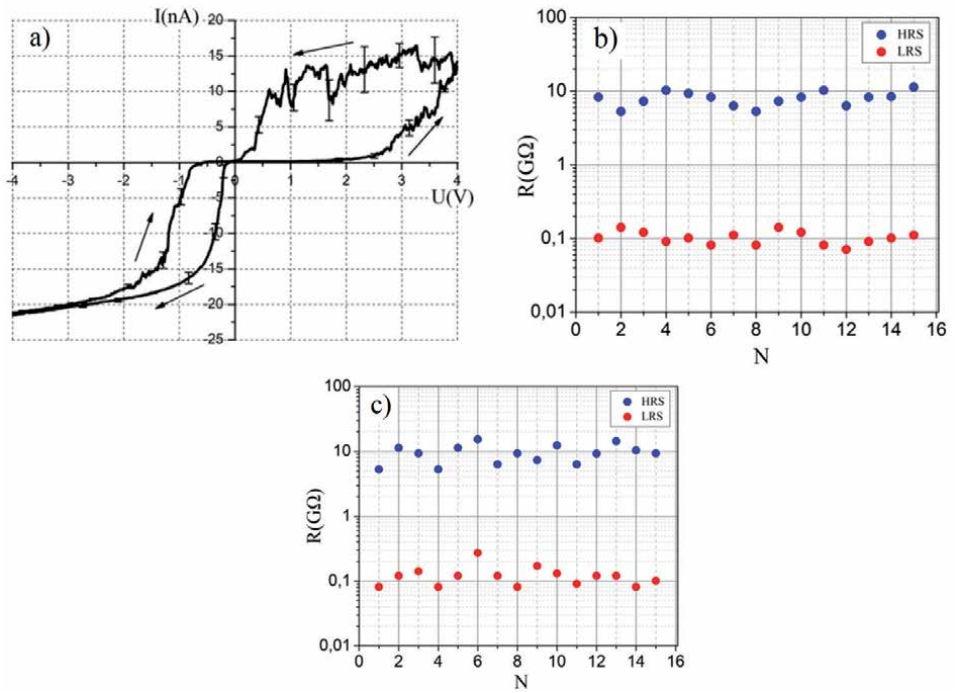

Figure 17.
Investigation of resistive switching in Al_2O_3/ZnO:In/ZnO/Ti/W_2C structure: (a) current-voltage characteristic; (b) uniformity; and (c) homogeneity.

4. Investigation of resistive switching in vertically aligned carbon nanotubes using scanning tunnel microscopy

4.1 Influence of voltage pulses amplitude on resistive switching of strained carbon nanotubes

The dependence of the resistive switching of a vertically aligned carbon nanotube on the voltage pulse amplitude was studied using the STM spectroscopy using the probe nanolaboratory Ntegra. **Figure 18** shows the current-voltage characteristics of a strained carbon nanotube, obtained by applying a series of voltage sawtooth pulses with amplitude of 1–8 V, duration of 1 second, and tunnel gap of 1 nm. The diameter of a VA CNT of the investigated array was 95 ± 5 nm, length 2.3 ± 0.2 μm, and density of nanotubes in the array was 18 μm^{-2}. It should be noted that the current-voltage characteristics are represented in the range from 0 to 50 nA, which relates to the peculiarities of the measuring system of the scanning tunneling microscope.

The measurement results showed that resistive switching of the VA CNT does not occur when the applied voltage amplitude is less than2 V (**Figure 18a**). This is due to the insufficient value of the external electric field for the formation of a low-resistance state in the nanotube [28]. The reproducible resistive switching was observed with a further increase in amplitude to 4 V and more (**Figure 18b–d**).

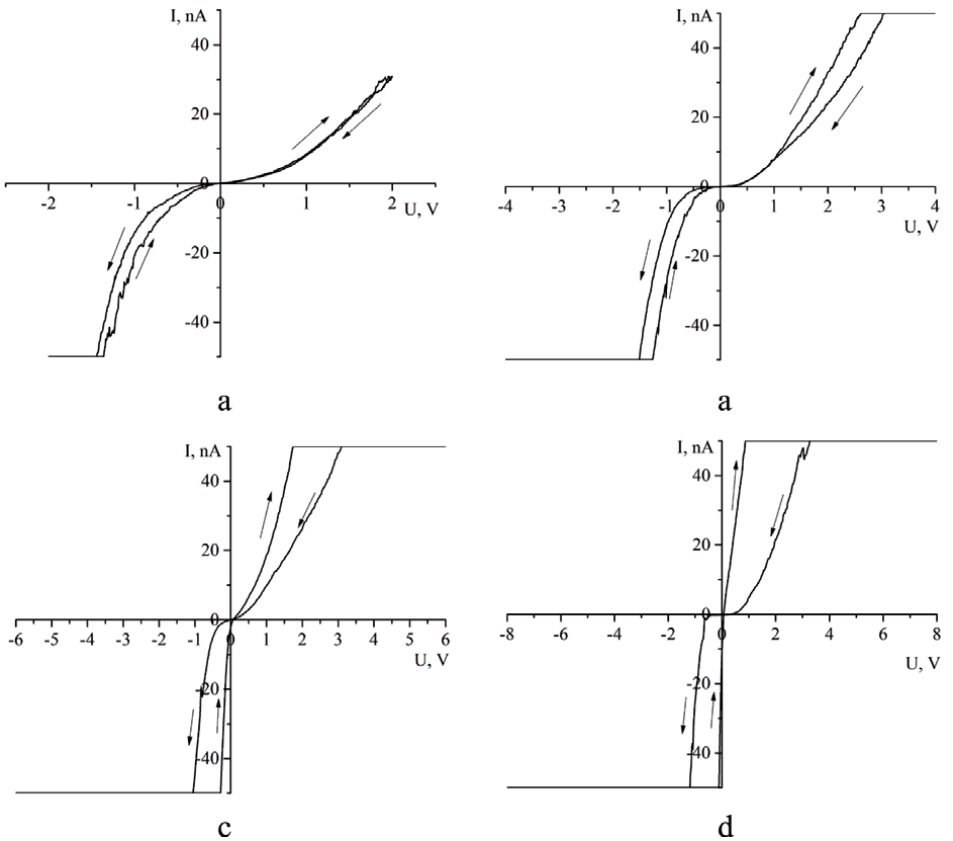

Figure 18.
CVCs of VA CNT upon application of a series of sawtooth voltage pulses with amplitude: (a) 2 V; (b) 4 V; (c) 6 V; and (d) 8 V.

The R_{HRS}/R_{LRS} ratio increased from 1 to 52 with an increase in the amplitude U from 1 to 8 V. This dependence is explained by the fact that the nanotube had the same resistance values of R_{HRS}, while the resistance of its low resistance state decreased inversely to the increase in the applied voltage amplitude due to the compensation of the internal electric field arising during deformation of the VA CNT with an external electric field [28].

It should be noted that the values of R_{HRS} and R_{LRS} of the VA CNT are 2–3 times lower at $U < 0$ than at $U > 0$. It is due to the fact that associated with the occurrence of a piezoelectric charge, internal field of the nanotube [33, 34] is co-directed with an external electric field, and accordingly, reduces the resistance of the VA CNT when a negative voltage is applied and is oppositely directed and increases the total resistance of the VA CNT when a positive voltage is applied.

4.2 Influence of deformation on resistive switching of strained carbon nanotubes

The studies of the influence of deformation on resistive switching of a VA CNT were performed by the STM spectroscopy with a tunneling gap d = 0.2, 0.5, 1, and 2 nm. Controlled elastic deformation of VA CNT was formed on the basis of the previously developed technique [32] and was equal to the tunnel gap. The value d was determined on the basis of current-height characteristics and was controlled using the STM feedback system. **Figure 19** shows the experimental current-voltage characteristics obtained by applying voltage sawtooth pulses with amplitudes of 4 and 8 V.

Analysis of the obtained CVCs showed that at U = 4 V, the R_{LRS} value initially decreased and increased again at $\Delta L = d = 2$ nm (**Figure 19a**). This is due to the fact that the magnitude of the external electric field was not enough to compensate the internal electric field of the nanotube at a deformation of 2 nm. This effect disappeared as the voltage amplitude increased to U = 8 V due to an increase in the external electric field (**Figure 19b**). The values of R_{HRS} and R_{LRS} of the VA CNT decreased with increasing deformation (**Figure 19b**). The decrease in the of R_{HRS} and R_{LRS} of the VA CNT is due to the increase in the initial deformation $\Delta L \approx d$ and the corresponding value of the piezoelectric charge, and is consistent with the mechanism of memristive switching of VA CNT [28].

It was also shown that the R_{HRS}/R_{LRS} ratio of the VA CNT does not depend on the deformation value and is determined by the value of the applied voltage: the R_{HRS}/R_{LRS} = 2–3 at U = 4 V (**Figure 19a**) and the $R_{HRS}/R_{LRS} > 50$ at U = 8 V (**Figure 19b**).

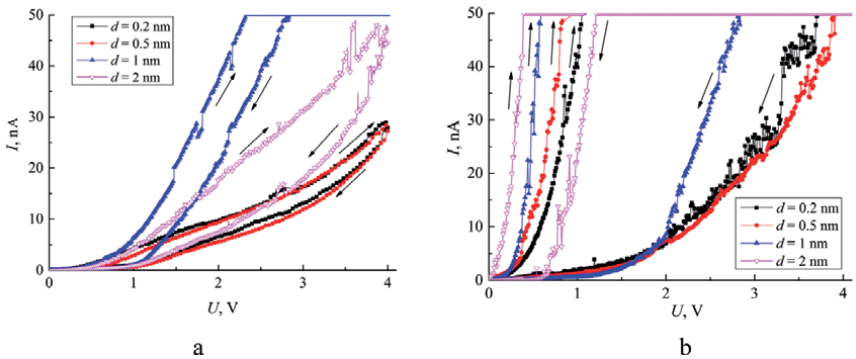

Figure 19.
CVCs of VA CNT at various values of deformation ΔL ≈ d and at voltage sawtooth pulses amplitude: (a) 4 V; and (b) 8 V.

5. Conclusion

Thus, application of scanning probe microscopy techniques for fabrication and determination of electrical parameters of memristor structures based on vertically aligned carbon nanotubes, titanium oxide nanostructures, and nanocrystalline ZnO thin films was presented. It is shown that titanium oxide nanostructures obtained by local anodic oxidation have a memristor effect without additional electroforming. The regularities of the manifestation of the memristor properties of oxide nanoscale structures of titanium are established, and the effect of the thickness of oxide nanoscale structures and the amplitude of applied voltage pulses on the displayed memristor effect in them is shown. It was found that the oxide nanoscale structures of titanium with a thickness of 1.6 nm have a resistance ratio in the high resistance to low resistance equal to 79.4. By using scratching probe nanolithography was made memristor structure based on nanocrystalline ZnO thin film obtained by pulsed laser deposition. The results can be used for micro- and nano-electronic elements manufacturing, as well as memristor structures, ReRAM elements using probe nanotechnologies, and for metal oxide and VA CNT-based neuromorphic system fabrication. The results of the study of resistive switching of vertical aligned carbon nanotubes using scanning tunneling microscopy are presented.

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Conflict of interest

The authors declare no conflict of interest.

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