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Advances in Memristor Neural Networks
Modeling and Applications

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ADVANCES IN MEMRISTOR NEURAL NETWORKS – MODELING AND APPLICATIONS

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http://dx.doi.org/10.5772/intechopen.75147
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First published in London, United Kingdom, 2018 by IntechOpen
eBook (PDF) Published by IntechOpen, 2019
IntechOpen is the global imprint of INTECHOPEN LIMITED, registered in England and Wales, registration number: 11086078, The Shard, 25th floor, 32 London Bridge Street
London, SE19SG – United Kingdom
Printed in Croatia

British Library Cataloguing-in-Publication Data
A catalogue record for this book is available from the British Library

Additional hard and PDF copies can be obtained from orders@intechopen.com

Advances in Memristor Neural Networks - Modeling and Applications
Edited by Calin Ciufudean

p. cm.

Print ISBN 978-1-78984-115-2

Online ISBN 978-1-78984-116-9

eBook (PDF) ISBN 978-1-83881-815-9

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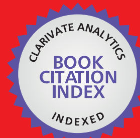

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Meet the editor

Dr. Calin Ciufudean is currently at the “Stefan cel Mare” University of Suceava, Faculty of Electrical Engineering and Computer Science, Department of Computers, Control Systems, and Electronics. He is the author of over 160 scientific papers published in scientific journals and conference proceedings abroad and in Romania, the author/coauthor of 17 books published in Romania and abroad, the author/coauthor of 32 inventions, and a technical expert for the Romanian Ministry of Justice. He is a member of the editorial boards of several international scientific journals and conferences of control systems and electric engineering science. He was designated chairman/keynote speaker for 34 international conferences.

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Preface

We are accused of going against the times. We are doing that deliberately and with all our strength.
—Lanza del Vasto

Neural networks significantly deal with a large area of applications such as image processing, speech recognition, natural language processing, and bioinformatics. Unfortunately, it is still difficult to fully analyze the inference provided by a layered neural network, as it contains complex parameters embedded in hierarchical layers.

Therefore, nowadays scientific research deals with alternative solutions for analyzing neural network architectures where the stochastic nature and live dynamics of memristive models play a key role. The features of memristors make it possible to direct processing and analysis of both biosystems and systems driven by artificial intelligence, as well as to develop plausible physical models of spiking neural networks with self-organization.

This book deals with advanced applications illustrating these new concepts, and delivers an important contribution for the achievement of the next generation of intelligent hybrid biostructures.

Different modeling and simulation tools can deliver an alternative to funding the theoretical approach as well as practical implementation of memristive systems.

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Section 1

Memristor Artificial Synapsis for Neural Networks

Chapter 1

Synaptic Behavior in Metal Oxide-Based Memristors

Ping Hu, Shuxiang Wu and Shuwei Li

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.78408

Abstract

With the end of Moore's law in sight, new computing paradigms are needed to fulfill the increasing demands on data and processing potentials. Inspired by the operation of the human brain, from the dimensionality, energy and underlying functionalities, neuromorphic computing systems that are building upon circuit elements to mimic the neurobiological activities are good concepts to meet the challenge. As an important factor in a neuromorphic computer, electronic synapse has been intensively studied. The utilization of transistors, atomic switches and memristors has been proposed to perform synaptic functions. Memristors, with several unique properties, are exceptional candidates for emulating artificial synapses and thus for building artificial neural networks. In this paper, metal oxide-based memristor synapses are reviewed, from materials, properties, mechanisms, to architecture. The synaptic plasticity and learning rules are described. The electrical switching characteristics of a variety of metal oxide-based memristors are discussed, with a focus on their application as biological synapses.

Keywords: memristor, metal oxide, synapse, neuromorphic computing, synaptic plasticity

1. Introduction

With the aid of modern technology, human society has entered into a new big data era. Meanwhile, it brings a new challenge to humans for data processing. Despite the great success in the past decades, the traditional computer based on Von Neumann architecture and complementary metal oxide semi-conductor (CMOS) technology is still suffering limitations of dealing with big data while it can only deal with well-defined data. These machines cannot compete with the biological system in solving the imprecisely specified problems of the real world which are very simple for biological beings [1, 2]. Even though the digital computers can emulate some functionality

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of certain animals with comparable speed and complexity, the energy consumptions increase exponentially as the animal hierarchy becomes higher with a very huge volume. Conversely, the biological brain is a compact dense system which can offer parallel processing, self-learning, and adaptivity with a combination of storage and computation in very low power consumption [3]. In these decades, the implementation of Von Neumann architecture computers to mimic biological systems has been in the form of software but such simulations are not comparable to biological systems in terms of efficiency and speed due to the physical limitation of those digital computers. Even the artificial neural networks based on CMOS-integrated circuits are far inadequate for constructing bionic systems. The truly reason for this drawback is the need to transfer data between a memory(storing data) and a processor(computing based on the data). This requirement of data transfer generates an intrinsic delay and inefficiency, which is a bottleneck for all CMOS-based neural networks [4]. In the past decades, the semi-conductive technology has led to great progress under the aid of the rapid development of the electronic industry, which has promoted the steps forward to develop artificial neural networks. In 2011, the supercomputer Watson, with 2880 computing cores [5], won the human-machine contest which proved that supercomputers have their advantages in some aspects [6]. But the important point that has been ignored in this comparison is the energy consumption and the physical volume of the computers. Watson has thousands of cores and requires about 80 kW of power and 20 tons of air-conditioned cooling capacity [7], while the human brain occupies space like a soda bottle and consumes power of 10 W.

Therefore, an alternative approach to building a brain-like or neuromorphic computational system with distributed computing and localized storage in networks becomes an attractive option [1, 8–11]. The brain-like computational system can outperform conventional computers with good performance in handing the real-time processing of unstructured sensory data, such as image, video or voice recognition, navigation, etc. [12–17]. Also, the brain-like computational system has the advantages of architecture and function compared to conventional computers, offering massive parallelism, small area, scalability, power efficiency, the combination of memory and computation, self-learning and adaptivity [3]. Many researches have helped us understand how neurons and synapses function and revealed how essential synapses are to biological computations, especially in memorizing and learning [18–21]. However, building compact neuromorphic computing systems remains as a challenge, especially for the lack of electronic elements which could mimic the biological synapses. In recent decades, the research of neuromorphic systems is renewed by the understanding of biological neural networks and the emergence of new nanodevices. Particularly, the emergence of the fourth electronic element, memristor [22–28], makes it feasible to construct bionic hardware which will lead to effective, high-performance neuromorphic computing hardware.

In this chapter, we will discuss synaptic devices and summarize the recent progress in neuromorphic hardware, which is based on memristors. In particular, we will focus on a few typical devices based on metal oxides and their key properties served as synapses. We will start with a brief description of memory and the learning of synapses in Section 2. In Section 3, we will elaborate more on these oxide-based memristors (TiO_x, WO_x, HfOx, TaOx, NiOx, etc.) with an emphasis on resistive switching (RS) characteristics, which is followed by neuromorphic computing applications and the underlying physical mechanism. We limit this review to metal oxide-based memristive devices for the emulation of synaptic functionalities and will not cover the literature on neuromorphic circuits.

2. Plasticity and learning of the synapse

In the nervous system, neurons and synapses are the basic units for transit information to the whole biological body. In the human brain, it consists of ~10^{11} neurons and an extremely large number of synapses, ~10^{15}, which act as a highly complex interconnection network among the neurons [29]. Neurons consist of three main parts: a soma, dendrites, and an axon. Neurons generate action potentials (spikes), with amplitudes of approximately 100 mV and durations in the range of 0.1–1 ms in their soma. The spikes propagate through the axon and are transmitted to the next neuron through the synapses. A synapse [30] is a 20–40 nm junction between the axon and the dendrites (shown in **Figure 1**) that permits a neuron (or nerve cell) to pass an electrical or chemical signal to another neuron or to the target efferent cell. Each neuron connects with other neurons through 10^3–10^4 synapses to form a complex network. The information transmission between neurons with the synapses is very complicated which

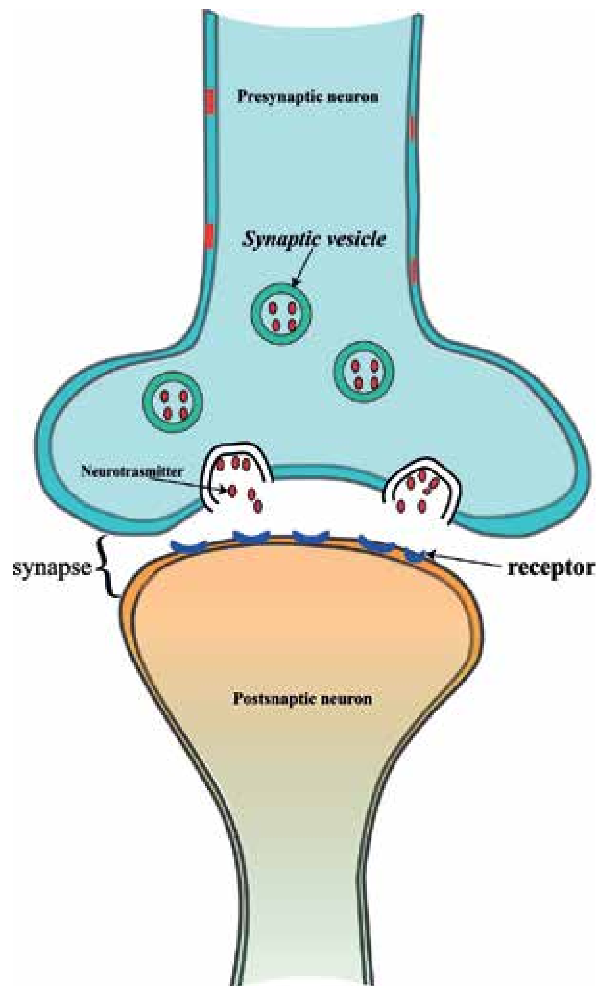

Figure 1. A schematic illustration of synapse.

is excited by the surroundings. At the synapse, the plasma membrane of the signal-passing neuron (the presynaptic neuron) comes into close apposition with the membrane of the target (postsynaptic) cell. Both the presynaptic and postsynaptic sites contain extensive arrays of molecular machinery that links the two membranes together and carries out the signaling process. The presynaptic neuron will open the voltage-gated calcium channels as the action potentials arrive, and then the diffusion of Ca^{2+} ions will make the synaptic vesicle release neurotransmitters to the synaptic junction. Released neurotransmitters bind with their receptor sites of the Na^{+} gated ion channels at postsynaptic neurons, which lead them to open and allow Na^{+} ions to diffuse inside the cell. When the aggregated membrane potential reaches a certain threshold, the neuron generates a spiking. The activation either potentiates or inhibits the postsynaptic neuron. The action potentials propagation, the neurotransmitters release and diffusion, and the neurons spiking activity constitute the ways whereby neurons communicate and transmit information to one another and to nonneuronal tissues [31].

In the biological brain, neurons and synapses are the two basic computational elements connected to each other. To perform different functions including visual, auditory, olfactory, gustatory and tactile means, as well as modulating and regulating a multitude of other physiological processes, the neuron system operates computation by integrating the inputs coming from other neurons and generating spikes across the synapses. In neuron computation, the synapses change their connection strength as a result of neuronal activity, which is known as synaptic plasticity. It is widely accepted that synaptic plasticity is the key mechanism of learning and memorizing for the biological brain [32]. In Hebbian's theory, both pre- and postsynaptic cells are activated coincidently, which results in modifications of synaptic strength between the two cells, thereby creating associative links between them [33]. In other words, the synapse plasticity is triggered by release of neurotransmitters of the presynaptic neurons and by diffusion of calcium ions into postsynaptic neurons, through excitatory amino-acid receptors and possibly voltage-gated calcium channels (VGCCs).

How the brain can achieve learning and memory is a critical question in neuroscience. In 1949 [34], Hebbian postulated a concept of spike-timing-dependent plasticity (STDP), firstly, as a synaptic learning rule which has been demonstrated in various neural circuits over a wide spectrum including insects, animals, and humans, even plants [35–37]. It has attracted considerable interest in neuroscience from experiment to computation [38–41]. According to the asymmetric window of STDP, the synaptic plasticity depends on the order of pre- and postsynaptic spiking within a window of tens of milliseconds. Over the past decades, much progress has been made in understanding the mechanism of STDP. In general, the synapse will be excited (increases in synaptic strength or weight) if repeated presynaptic spikes arrive a few milliseconds before postsynaptic spikes, whereas the synapse will be inhibited (decreases in synaptic strength or weight) if repeated spikes arrive after postsynaptic spikes. In [35], Bi and Poo have plotted a figure of the synaptic weight change as a function of relative timing of pre- and postsynaptic spikes which is called the STDP function or learning window and varies in synapse types. The change of synaptic weight Δw_i depends on the relative timing between presynaptic spike and postsynaptic spikes. A smaller spike timing difference results in a larger increase in synaptic weight. The total weight change Δw_i induced by an impulse with pairs of pre- and postsynaptic spikes is considered as a function [42, 43]:

$$\Delta w_i = \sum_{f=1}^{N}\sum_{n=1}^{N} W\left(t_j^n - t_i^f\right) \tag{1}$$

where *W(x)* denotes the STDP function, *i,j* are the notes of the pre- and postsynapses, and t_i^f (t_j^n) labels the firing times of the pre(post)synaptic neuron. An acceptable form of STDP function *W(x)* is given as

$$W(x) = \begin{cases} A_+ \exp(-x/\tau_+), & x > 0 \\ -A_- \exp(x/\tau_-), & x < 0 \end{cases} \tag{2}$$

The parameters A_+ and A_- depend on the current value of the synaptic weight w_i where τ_+ and τ_- are the time constants in the order of 10 *ms for* biological synapses [36]. Several recent reports have shown the STDP dependencies on rate, higher-order spiking motifs, and dendritic location [39]. This timing-centric view of plasticity is not meant to imply that spike rate is irrelevant. However, this timing-centric view of plasticity is not the only form responsible for synaptic learning in the biological brain. The learning rules may vary with different factors, such as the type, location of a synapse, firing rate, and spiking orders. Several other fundamental learning rules including rate-dependent synaptic plasticity, frequency-dependent synaptic plasticity, and cooperativity have also been studied extensively and believed to be very critical for biological neuron computation.

3. Synaptic devices based on metal oxide memristors

To imitate the learning and memorization of the biological system, new materials as well as architectures exhibiting memristive behavior fit the need well. Memristor, an abbreviation of memory and resistor, is the fourth fundamental passive circuit elements, the others being the resistor, the capacitor, and the inductor, which were proposed theoretically by Professor Leon Chua [22]. It is a kind of a nonlinear, two-terminal element that cannot be replicated with any combination of other fundamental electrical elements. Memristors behaves like a resistor with resistance depending on the history of the current passing through. In fact, it maintains a relationship between the time integrals of current and voltage across a two-terminal element, and the resistance remains in the value as it had earlier when the current stopped. In other words, the memristor has a memory of the current that was last turned on. In 2008, HP Labs realized memristors physically in nanoscale titanium dioxide cross-point resistive switches [24]. In this operation, the device exhibits pinched current-voltage(I-V) hysteresis indicating a resistive memory effect, and the conductive area is adjusted by the concentration of oxygen vacancies, which determine the whole conductive states (resistive switching state), that is, high resistance state (HRS) and low resistance state (LRS). This work invoked a renewable research of new materials and devices that have memristive effects, such as NiO, WO_3 ZrO_2, ZnO, HfO_2, TaO_2, and TiO_2 [44–50] binary oxides, $BiFeO_3$, $SrTiO_3$, $ZnSO_3$, and $LiNbO_3$ [51–54] ternary oxides, and CuO/ZnO, HfO_2/TiO_2, and TaO_x/NiO_x [55–57] heterostructures. **Table 1** gives a summary of the recent work of oxide-based memristors including memristive properties.

Material (architecture)	Endurance (cycles)	Retention	On/off ratio	Reference
$Pt/TiO_2/Pt$	83	10^4s	2	[69]
$Pt/TiO_x/Pt$	8000	—	1.2	[50]
$Pt/Ta_2O_5/Pt$	1000	10 years	10^6	[49]
$Ti/TaO_x/Pt$	120	10^4s	65	[50]
$ITO/WO_3/ITO$	320	2×10^4 s	10	[45]
$Al/WO_3/Pt$	200	3×10^4 s	~50	[79]
$Cu/WO_3/Pt$	150	3×10^4 s	~10	[79]
$Pt/WO_3/Pt$	50	3×10^4 s	~100	[79]
$Cu/WO_{3-x}/ITO$	1000	5×10^4 s	10^5	[80]
Al/ZnO/Al	5	—	54.8	[47]
$Al/ZnO_{1-x}/Al$	5	—	4.8	[47]
Ag/ZnO/Pt	100	10^7s	10^7	[106]
Ti/ZnO/Pt	1000	—	100	[107]
Al/ZnO/Pt	300	10^5s	10^4	[108]
$Pt/ZrO_2/Pt$	200	10^4s	162	[44]
$Cu/ZrO_2/Pt$	50	10^4s	30	[44]
$Ti/ZrO_2/Pt$	100	—	10^4	[109]
$ITO/ZrO_2/ITO$	150	10^3s	~7	[110]
$TiN/ZrO_2/ZrO_{2-x}/TiN$	50	10^4s	40	[110]
$Ta/HfO_2/Pt$	10^{11}	10 years	~100	[111]
$TiN/HfO_2/Pt$	1000	10^4s	~15	[112]
$Ti/HfO_2/Pt$	50	3×10^3 s	100	[100]
$Pt/HfO_2/HfO_{2-x}/TiN$	100	—	1000	[103]
$Pt/BiFeO_3/Pt$	50	2×10^3 s	~100	[51]
$Pt/Ti/Nb:SrTiO_3/Pt$	100	10^5s	$\sim10^3$	[105]
$Cu/HfO_2/TiO_2/Pt$	1000	10^3s	10	[56]
$Pt/NiO_x/TiO_2/FTO$	100	10^4s	100	[104]
$Pt/Ti/Ta_2O_5/HfO_2/Pt$	50	2×10^3 s	650	[102]

Table 1. Recent work on metal oxide-based memristors.

Nowadays, the memory is usually referred to as resistive random-access memory (RRAM) devices which can be traced as early as the 1960s [58]. In general, these devices are nanoscale in dimensions and offer excellent performance for data storage in terms of operation speed, nonvolatility, and read/write cycling [59]. Amounts of work have been performed to elucidate types of switching mechanisms that underlie resistive switching phenomena in a

broad spectrum of material systems [25–28, 60–62]. According to the switching mechanism, the memristors can be categorized into phase change, valence change, conductive bridge, electrochemical metallization, and ferroelectric devices. Due to the simple structure, biological plausibility, and excellent properties for memory, the scientific researchers explored the application of memristors from data storage to analogy neuromorphic computing for spatial-temporal pattern recognition, sequence learning, navigation, and direction selectivity. As for the human brain-like characteristics, memristor technology could one day lead computer systems to a new state that can remember and associate patterns in a way similar to how people do. Next, we will focus on several kinds metal oxide-based memristors with analog synaptic behavior which are intensively studied for neuromorphic computing.

3.1. TiO_2- and WO_3-based memristors

The first physical instantiation of the memristor was generally acknowledged that was made from TiO_2 by Strukov et al. [24], but as early as in 1968, it was found that the TiO_2 thin-film device shows memristive properties [63]. In literature [63], the work demonstrated that thin films exhibited resistive switching (RS) effects with pinched hysteretic current-voltage (I–V) curves during repeated tests. And also, there are several experimental researches on the RS effect of TiO_2-based devices before 2008, such as Pt/TiO_2/Ru [64] and sputter-deposited Pt/TiO_2/Pt [65] devices. For memristors, the distinctive property is the pinched hysteretic loop indicating no energy dissipation. In [62], the prototype of memristor showed bipolar RS I–V curves with pinched points, which are a result of local stoichiometric change caused by the migration of oxygen vacancies. As oxygen vacancies act as donors in the TiO_2 layer in the depletion zone, the conductance of the device could be modulated by the depletion or accumulation of Vos. Specifically, when the device undergoes a set process from a high resistance state to a low resistance state by the external electric field, the Vos will accumulate resulting in an increase of the conductive layer width. When applying electric pulse with reverse polarity, the Vos will be driven back thereby the conductive layer will become thin. Later it was demonstrated in some studies that the accumulation of Vos in TiO_2 may cause the formation of a new Magneli phase (Ti_4O_7) that is metallic and directly studied by TEM [66, 67]. In 2009 [68], a flexible Al/TiO_2/Al memristor fabricated by solution processing was reported. In this work, it showed that oxygen vacancies were introduced by the aluminum electrodes, and if a noble metal (Au) electrode was used, the form and reversibility of switching will change. The mechanism of the memristive effect strongly depends on the synthesis method, the choice of metal electrodes, and their interfacial properties. Many suggested that an understanding has been put forward through a series of experimental analyses from the view of film composition, microcrystalline structure, and switching zones. It also should be noted that the RS effect of the devices will be affected by device architecture, electrode materials, and layer stacks.

As a prototype of the memristor, TiO_{2}-based devices show their potential in neuromorphic computing. Seo et al. [69] used titanium oxide as the active material to perform synaptic behavior in the context of analog memory, synaptic plasticity and STDP function. A bilayer of TiO_x and TiO_y structure was fabricated by atomic layer deposition and the sol-gel method, respectively. In the device, the titanium oxide bilayer works as a progressive resistance-changing medium with Al and W as the top and bottom electrodes. The multilevel conductance states were achieved by

the movement of oxygen between the TiO_y and the TiO_x layer. In the report, the thickness of the less conductive layer TiO_y was controlled by the applied bias which finally resulted in multi-level conductance and analog memory characteristics. As a positive bias was applied to the top electrode, the oxygen ions were driven from TiO_y to TiO_x and the effective thickness of the TiO_y layer is reduced, which resulted in an increased conductance. Conversely, by applying negative bias to the device, the oxygen ions are moved from TiO_x to TiO_y, which caused a reduction of conductance. Due to the easy controlling of conductance, the analog characteristics of this device have been intensively studied. By applying sets of identical positive (negative) pulses, conductance can be progressively increased (decreased) as well as the potentiation (depression) in biological synapse. **Figure 2** illustrated the continuous potentiating and depressing characteristics of the device which were extremely useful for precisely modulating the device's synaptic weight. Also, the prior conductance state dependence of the subsequent conductance change is shown in **Figure 2b**. The results confirmed that the device showed the behavior as in the biological synaptic STDP model [70]: prior synaptic weight states affect the subsequent weight change. Furthermore, the time dependence of the device conductance change was studied which resembled that of the biological synapse. This indicated the titanium oxide bilayer's resistive switching device had great potential for mimicking biological synapses.

In 2012 [71], Yu fabricated $TiO_x/HfO_x/TiO_x/HfO_x$ multi-layer RRAM stacks and showed that the resistance states of the stacks could be gradually modulated by using identical pulses. The gradual resistance modulation behavior is useful for learning with high fault tolerance. Berdan in 2016 [72] demonstrated that TiO_2 memristors can exhibit non-associative plasticity. The transition between long-term plasticity (LTP) and short-term plasticity (STP) of this device was presented. The rate-limiting volatility in TiO_2 RRAM devices was very essential to capture short-term synaptic dynamics. In addition to Seo's works on the bilayer TiO_x/TiO_y device [69], Bousoulas studied the role of interfaces in TiO_x/TiO_y RRAM structures for high multilevel switching and synaptic properties [73]. A CMOS-memristor architecture composed of the 8*8 array of the neuron was demonstrated by Mostafa [74]. The proposed system comprises CMOS neurons interconnected through TiO_{2-x} memristors and spike-based learning circuits which modulate the conductance of

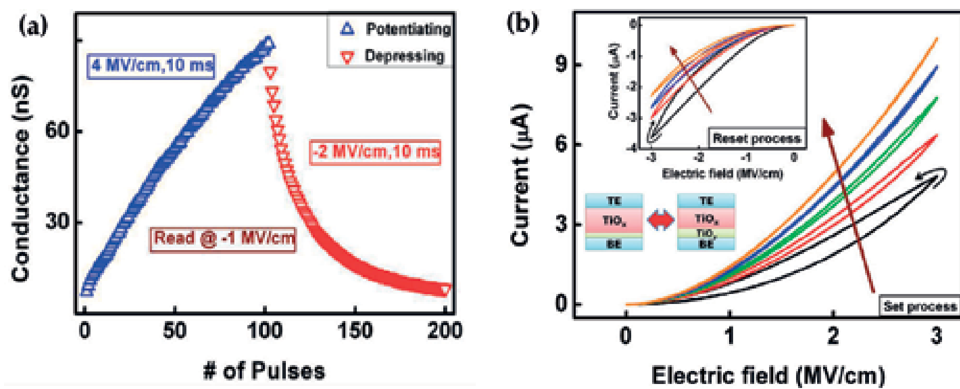

Figure 2. (a) The potentiation and depression for the device and (b) conductance dependence on history. Reprinted with permission from [69].

the memristive synapse elements according to a spike-based perceptron plasticity rule. In 2016, Park developed a Mo-/TiOx-based interface RRAM with 64-level conductance states and proposed a hybrid pulse mode for the synaptic application [75]. Under the stimuli of the hybrid pulse mode, the TiO_{2-x}-based devices show good performance and enhanced pattern recognition accuracy, which was confirmed through synaptic simulation.

Although many investigations have been carried out on the resistive switching mechanism of the TiO_2-based memristor, the demonstration of TiO_2-based memristor for the artificial synapse is still limited when compared to PCMO, HfO_x, and TaO_x materials. In most situations, TiO_x is used in bilayer or multi-layer stacks' synaptic device to optimize the performance. Another great candidate for memristors as artificial synapses is tungsten oxides (WO_x) because of their high endurance, CMOS compatibility, and memorization and learning functions.

Similar to TiO_2, WO_3 is also extensively studied as a memristor due to its CMOS compatibility into standard manufacturing processes [76]. Additionally, WO_3 is a kind of transition metal oxide and can be served as n-type semiconductors depending on its stoichiometry and morphology. Due to its attractive properties, it has been studied for both digital and analog memory. Liu et al. [77] have fabricated Cu/WO_3/Pt structure devices and demonstrated multilevel storage properties by the application of suitable compliance current values. In that study, the device exhibited pronounced RS effects with an endurance of over 100 cycles and a retention of over 10^4 s. During the set process, the conductive filament is modulated by the compliance current between the Cu and WO_3 interface. In addition to the work of Celano [78], the applied positive bias will aid the creation of oxygen vacancies resulting in conductive filaments. The applied negative bias will drive back the oxygen ions to recombine with the vacancies, making the device turn OFF. Meanwhile, the role of electrodes on RS effect has also been studied, such as Ag/WO_3/ITO, W/WO_3/Pd, and Pt/WO_3/ITO [79, 80]. In these studies, no matter the material of the electrodes, the RS effects originate from the formation or annihilation of oxygen vacancies. Under positive bias, the non-inert electrode is oxidized and the ions diffuse toward another electrode to expand a conductive filament and *vice versa*. That is to say, a continuous concentration gradient of oxygen vacancies will be introduced during the oxidation process for the inert electrodes, which can result in low or high resistance states of the devices. In addition, the temperature and humidity impact on the performance of WO_x memristors were studied [81, 82]. The conductance will decrease as the temperature increases due to higher oxygen vacancies' diffusion. In addition to the temperature, the memristive effects of tungsten oxide are also highly humidity dependent. The adsorbed moisture on the surface of WO_3 has resulted in decreasing conductances as the H cation induces an increase in barrier heights.

Synaptic behaviors and modeling of WO_x memristors were reported by Chang [83]. The Pd/WO_x/W memristor shows reliable synaptic operations with robust endurance behavior. The devices can endure at least 10^5 potentiation/depression pulses without degradation which is a necessary characteristic for practical applications in neuromorphic systems. Furthermore, the conductance change is governed by the history of the applied voltage signals, leading to synaptic behaviors including long-term potentiation and depression. The memristor behavior was explained by a novel model that takes both drift and diffusion effects into consideration. **Figure 3** presents the retention loss curve and memory loss in a human memory curve of the Pd/WO_x/W memristor [84]. It was found that the memristor device retention can be

improved with the application of repeated stimulations and bears remarkable similarities to the STM-to-LTM transition in biological systems. Among other transition metal oxides, WO_x is a great candidate material for synaptic device application. For further exploring its applications in neuromorphic computing, the enhancement of synaptic operation time (endurance) is of importance.

3.2. Other metal oxide memristor-based synaptic devices

Besides titanium oxide- and tungsten oxide-based memristors discussed above, a variety of other materials has been studied to implement the neural network as a synaptic device. Similar to TiO_x, NiO_x is one of the earliest materials found to exhibit restive switching behavior. Although NiO_x-based RRAM devices have been reported with high endurance (10^6) and retention, its application for neuromorphic computing is restricted due to poor uniformity. Akoh fabricated synaptic devices with bipolar NiO_x memristors [85]. This device also has the ability to update the synaptic conductance according to the difference of pre- and post-neuron spike timing. Hu *et al.* studied the paired-pulse-induced response of an NiOx-based memristor, which is similar to the paired-pulse facilitation(PPF) of biological synapse [86]. In addition to PPF, the synaptic LTP of NiOx-based memristors was also studied by Hu et al. [87]. The LTP effect of the memristor has a dependence on pulse height, width, interval, and number of pulses. An artificial neural network is constructed to realize the associative learning and LTP behavior in the extinction of association in Pavlov's dog experiment.

AlO_x is of interest in memristor materials due to its large band gap (~9 eV) and low RESET current (~ μA). For neuromorphic application, AlO_x can also be used alone or stacked with other RRAM materials to improve the uniformity of the synaptic device characteristics. A GdO_x and Cu-doped MoO_x stack with platinum top and bottom electrodes was reported by Choi [88]. The weighted sum operation was carried out on an electrically modifiable synapse array circuit based on the proposed stacks [89]. The biological synaptic behavior was demonstrated by Chang through integrating SiO_x-based RRAM with Si diodes. The proposed one-diode-one-resistor (1D-1R) architecture not only avoids sneak-path issues and lowers standby power consumption but also helps to realize STDP behaviors [90]. VO_x is a well-known Mott material,

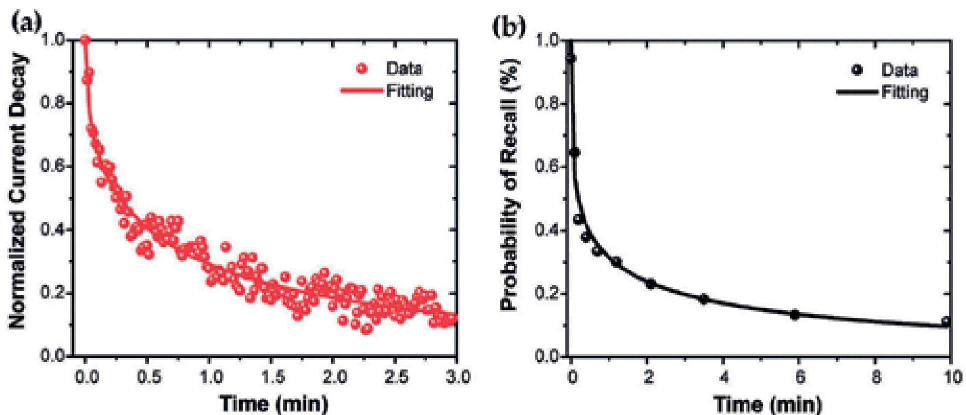

Figure 3. (a) Retention loss curve of Pd/WOx/W-based memristor and (b) forgetting memory of the human memory curve. Reprinted with permission from [44].

which experiences sharp and first-order metal-to-insulator transition (MIT) at the around 68°C [91]. The application of VO_x as RRAM materials had been explored by Drisoll et al. [92] through the sol-gel technique. Nevertheless, most researches on VO_x so far focus on its use for select devices, which can be integrated with the RRAM device to mitigate sneak-path current. The Pt/VO_2/Pt selector has been integrated with NiO unipolar RRAM by Lee et al. [93] in 2007 and ZrO_x/HfO_x bipolar RRAM by Son et al. [94] in 2011. In 2016, 1S-1R configuration of W/VO_2/Pt selection device and Ti/HfO_2/Pt RRAM was demonstrated by zhang et al. [95]. However, thermal instability is a major challenge with VO_2 for practical applications [13].

3.3. Mechanisms

The modulation of the device resistance with memory effects is essential to mimic biological synapse. And the understanding of switching mechanism is also important to incorporate memristors as a bionic synapse into the neuromorphic computing system. Many suggestions have been put forward to elucidate the causes of resistive memory effects of those oxide-based memristors. The most popular views on RS mechanism are taken as ionic diffusion and thermal effect.

For the mechanism of ionic drift and diffusion, under the stimulation of applied bias, the ions will migrate, and the conductance of memristors will be enhanced or depressed [96–98]. Actually, there are two types of ionic drift: cation and or anion drift, which depends on the materials used for active layers and electrodes. For example, for Strukov's [24] TiO_2 memristor, both electrodes have inert Pt; the movement of oxygen vacancies causes the whole active TiO_2 layer to separate into two parts, with one part rich in oxygen vacancies and being more conductive. Hence, the difference in the concentration of oxygen vacancies leads to oxygen ion (anions) diffusion. Oxygen ions move to the anode and more oxygen vacancies are created. The increase of oxygen vacancies then makes the device more conductive to a low resistance state. Meanwhile, there is some evidence that the noninert electrode can hinder the combination of oxygen ions and serve as an oxygen vacancy reservoir. In the set process, the metal is oxidized and the metal ions diffuse into the insulating layer to develop a conducting filament. Under negative bias, the filaments are ruptured by the increase of the electric field.

The second mechanism is about the heating effect [99, 100]. In the set or reset process, the active layer material is changed by the application of an electric field and flowing current heat. As the current is applied, the heat is released and the ions drift, forming an electron path to develop the conductive filament. At the same time, due to the collision of electrons, a new boundary may be created that inhibits the formation of the filament with excess heat [100]. Joule heating effects have been credited both in unipolar and in bipolar switching memories. In unipolar switching, under the high current passing through the memory devices, the heating fuses the conductive filaments in the reset process which is similar to that in bipolar switching. In bipolar switching, Joule heating dissolves the filament when sufficiently high current flows through the device. If this rupture happens in the SET process, it becomes a valid operation since the resistance did not stay in LRS and result in threshold switching [101]. However, large current should be avoided in the device which will introduce bad effects to performance or lead to a permanent failure because large current flowing through the filament will generate severe Joule heating, and a steep increase of the temperature in the filament will finally melt the filament.

Generally, the physical origin of the switching effect in memristors depends on architectures, materials, and interfaces. The comprehensive study of the mechanism is very helpful to the manipulation of memory and to extend the application of memristors. In terms of conductance modulation in memristors, many metal oxide-based memristors can perform not only on digital memory but also on analog memory which is similar to biological functions.

4. Conclusion

In this review, we have outlined an overview of memristor-based synaptic devices, especially for the metal oxide memristors. The neuromorphic approach with oxide-based RRAM devices is promising. Focusing on TiO_x, WO_x-based memristor, the electrical switching characteristics are reviewed. Exploiting the physical mechanisms, the synaptic behaviors of those devices are also discussed. Owing to the magnificent increased computational efficiency, and also increasing compatibility in computer technology and CMOS technology, metal oxide-based synaptic devices are gaining prominent interest. The progress of neuromorphic engineering on devices confirms that the memristive synapses can meet the demand of low energy consumption, high connectivity, and density in neuromorphic devices for efficiently encoding, storing, and processing information. However, challenges still remain for overall oxide-based RRAM materials. Although the inherent fault tolerance of neural network models is able to mitigate the impact of device variation to some extent, the improvement of spatial variation and temporal variation turns out to be one of the greatest challenges on a long-term basis. In addition, the improvement of reliability characteristics of the memristor synaptic devices is another key challenge which is not well studied.

Acknowledgements

This work was supported by National Natural Science Foundation of China (Grant Nos. 61,273,310 and 11,304,399), Natural Science Foundation of Guangdong Province (Grant Nos. 2015A030313121 and 2016A030310234), Scientific Research Fund of Hunan Provincial Education Department (Grant No. 15B203), and the Fundamental Research Funds of Central Universities (Grant No. 17lgpy02).

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Section 2

Memristor Neuromorphic Technologies for Computing Architecture

Chapter 2

The Roadmap to Realize Memristive Three-Dimensional Neuromorphic Computing System

Hongyu An, Kangjun Bai and Yang Yi

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.78986

Abstract

Neuromorphic computing, an emerging non-von Neumann computing mimicking the physical structure and signal processing technique of mammalian brains, potentially achieves the same level of computing and power efficiencies of mammalian brains. This chapter will discuss the state-of-the-art research trend on neuromorphic computing with memristors as electronic synapses. Furthermore, a novel three-dimensional (3D) neuromorphic computing architecture combining memristor and monolithic 3D integration technology would be introduced; such computing architecture has capabilities to reduce the system power consumption, provide high connectivity, resolve the routing congestion issues, and offer the massively parallel data processing. Moreover, the design methodology of applying the capacitance formed by the through-silicon vias (TSVs) to generate a membrane potential in 3D neuromorphic computing system would be discussed in this chapter.

Keywords: memristor, synapse, three-dimensional integrated circuit, neuromorphic computing, analog/mixed-signal circuit design, monolithic 3D integration

1. Introduction

The continued success of the development in the modern von Neumann computing system was firstly enabled by the increment of the transistor integration density, followed by the multicore computing architecture. However, hindered by the fabrication process and size incompatibility between technologies of the complementary metal-oxide-semiconductor (CMOS) and the memory, central computing units (CPUs) and memory are located separately in resulting that the communication bus is inevitable. This communication bus becomes an energetic and speed bottleneck in this architecture. Furthermore, the transistor size shrinking

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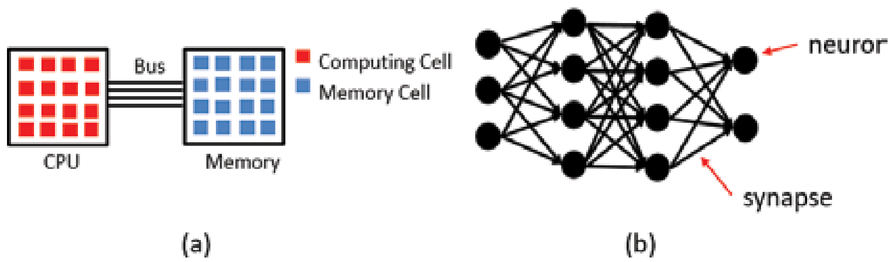

Figure 1. Architectures of (a) von Neumann computing system and (b) neuromorphic computing system.

trend is even harder to catch Moore's prediction due to the physical limitations [1]. As the density of data continuously escalates, extracting valuable information becomes computationally expensive, even for supercomputers. Meanwhile, the amount of energy required for supercomputers poses doubt on whether the increased performance is affordable.

On the other hand, as human beings, our brains have capabilities of learning and analyzing surrounding information with merely 20 W of power consumption [2]. Inspired by the working mechanism of the nervous system, the performance development of the computing system has led to a novel nontraditional computing architecture, namely, the neuromorphic computing system. The neuromorphic computing system was proposed by Carver Mead in the 1980s to mimic the mammalian neurology using the very-large-scaled-integrated (VLSI) circuit [3]. **Figure 1** illustrates the difference between the von Neumann architecture and the neuromorphic computing system. As powerful as the brain, the neuromorphic computing system potentially solves computing-intensive tasks that are only handled by the human brains before. These multifaceted tasks include speech recognition [4–6], character recognition [7, 8], grammar modeling [9], noise modeling [10], as well as the generation and prediction of chaotic time series [11, 12], etc. However, state-of-the-art neuromorphic chips with the traditional CMOS technology and the two-dimensional (2D) design methodology cannot meet the energetic and speed requirements at large-scale neuron and synapse realization [13–17]. In order to address this issue, recently, a three-dimensional (3D) neuromorphic computing architecture combining the memristors as electronic synapses is proposed and investigated [18–20].

This chapter is organized as follows, Section 2 introduces the background information of the neuromorphic computing, Section 3 discusses various neural models and their corresponding hardware implementations, Section 4 describes the biological reasons for employing memristive devices as electronic synapses, Section 5 illustrates the proposed 3D neuromorphic computing architecture, and at last, Section 6 draws some conclusions.

2. Neuromorphic computing

The digital computer based on the von Neumann architecture has powered our society for more than 40 years with its constant increment on computing capability. **Figure 2** shows the diagram of the typical von Neumann architecture. In this architecture, central computing

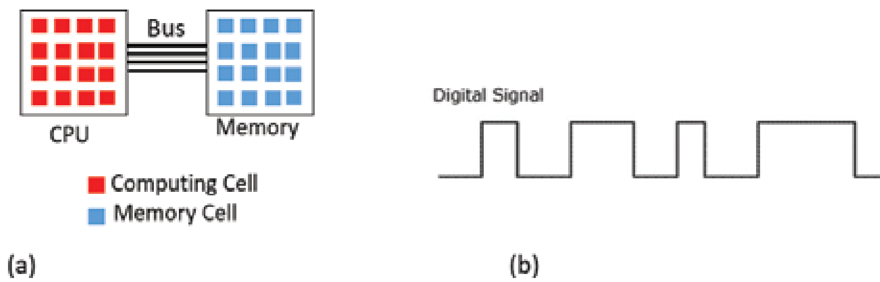

Figure 2. (a) The von Neumann architecture, (b) digital signal in computer.

units (CPUs) and memory units are physically separated at different locations due to their incompatibilities of fabrication process and size. A communication bus is used for the data transferring between them. In order to perform the Boolean algebra and arithmetic, the data stored in the memory need to be retrieved from the memory to CPU and be transferred back to memory after computing. These processes would be repeated a million times for accomplishing a data-intensive computing task; consequently, the communication bus connecting CPUs and memory inevitably becomes the energetic and speed bottleneck. Moreover, for achieving more powerful computing capability with low-power consumption, the transistor scaling and operating frequency increment is becoming the direction of technological development.

To achieve high computing capability, an extremely large number of transistors have been compressed in a single CPU. Furthermore, the power consumption is almost linear dependent proportionally with operation frequency [21]. This means that the power consumption and computing capability need to be balanced and cannot be achieved simultaneously with recent CMOS technology under the von Neumann architecture. On the contrary, scientists have noticed that the human brain has an excessive computing and energy efficiency [22]. With the idea and hypotheses to build a brain-like computing machine, the concept of neuromorphic computing was proposed by Dr. Mead [3]. The significance of the neuromorphic computing is not only for building a more-powerful computer, but also can potentially reveal the fundamental operating mechanism of the human brain. Another similar well-known concept is the artificial neural networks (ANNs), which is an attempt of simulating the neural network configuration of the brain, thereby to study the function of the brain [23, 24]. The main differences between neuromorphic computing and conventional ANNs are the former focuses more on the physical realization on the brain structure, while the latter studies the mathematical models of human brain structure. Neuromorphic computing is expected to offer an intelligent machine beyond the modern digital computer with capabilities of adaptive, distributive, cognitive computing, and perceptive computing. These capabilities fundamentally come from the unique architecture, computing/memory units, signal encoding scheme, and operating algorithms of the neuromorphic computing system.

To successfully implement a neuromorphic computing system, a comprehensive understanding of the differences between the human brain and von Neumann-based computer would be conducive to reverse engineering the brain, thus implementing the neuromorphic computing system. **Figure 3** illustrates the main difference between the human brain and the von Neumann

architecture from the device to the algorithm levels. In a brain-like neuromorphic computing system, blocking devices (computing units and memory units) need to be replaced from traditional CPUs and SRAMs to artificial electronic neurons and synapses. This is the first step for mimicking the brain at a device level. Unlike computing units in the CPUs that perform the binary code–based computing, the data in electronic neurons and synapses need to be represented in a spike sequence format for generating the brain-like signals [22]. Then, these electronic neurons and synapse are interconnected with each other in a brain-like neural network configuration at the architecture level, which is demonstrated in **Figure 3**. Spiking signals would be used for communication in this architecture. This neural network-based architecture eliminates the long signal transferring distance between CPUs and the memory in von Neumann architecture since the computing can be performed by neurons with the data extracted from adjacent memories (synapses). Due to the unique non-von Neumann architecture and spiking encoding scheme of the neuromorphic computing system, the binary algebra is not suitable for this system anymore. In the field, neural network-based machine learning algorithms are widely considered as the ideal candidate for running neuromorphic computing system.

Although fundamental functions of the brain are still under investigation, two main elements: neuron and synapse are well studied at the cellular level. The structure of a neuron is shown in **Figure 4**. There are four main parts of each neuron, whose functionalities are summarized as:

- Dendrite: the organ that receives spiking signals from other neurons,
- Soma (neuron body): generates/sends spiking signals to the axon under the condition of the integration of received spiking signal levels, which exceed a specific threshold voltage;
- Axon: propagates spiking signals to other neurons,
- Synapse: a space between the axon of the presynapse neuron and dendrite of the postsynapse neuron. It is widely considered as a memory organ in the brain by storing the memory information in its connectivity strength.

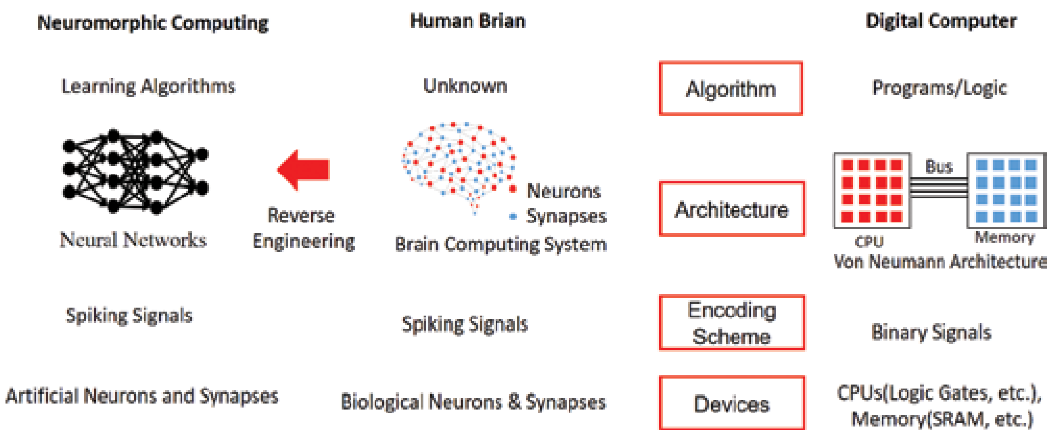

Figure 3. Comparison between brain computing architecture, von Neumann computing architecture, and neuromorphic computing architecture.

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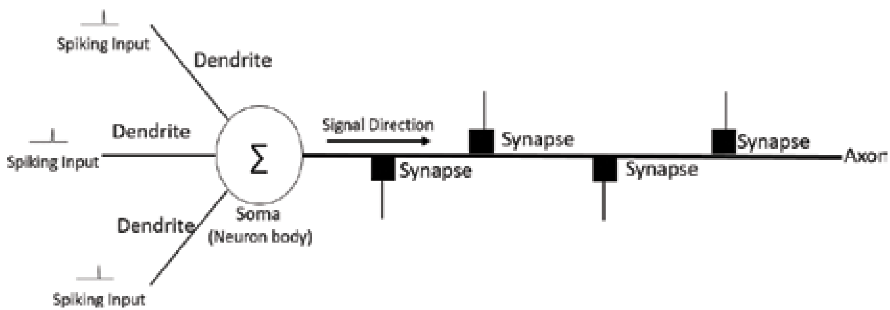

Figure 4. Neuron structure.

Unlike the rigid connection configuration of computing units and memory in the von Neumann architecture (**Figure 2**), neurons and synapses can be connected to each other in different topologies. **Figure 5** depicts three mainstream neuromorphic computing architectures named as the distributed neuromorphic computing architecture, cluster neuromorphic computing architecture, and associative neuromorphic computing architecture [13].

Firstly, the distributed neuromorphic computing architecture (DNCA) decomposes centralized computing units and memory units in a distributed brain-like network structure. In this architecture, neurons and synapses are located close to each other to minimize the signal propagation distance through communicating only with the adjacent electronic synapse (memory data).

Secondly, in the human brain, different types of sensory signals (for example somatic, tactile, auditory, visionary, olfactory, and gustatory signals) are routed and processed in different regions of the brain [22]. The cluster neuromorphic computing architecture (CNCA) is proposed to realize this signal processing methodology of the human brain. In this architecture, the proposed DNCA is divided into multiple regions, which are intrinsically responsible for processing signals captured by different types of sensory devices independently. This signal processing technique enables the CNCA to process multiple massive signals parallel in various regions with distributedly located neurons and synapses, thereby, realizing a parallel computing capability inherent similar to the human brain.

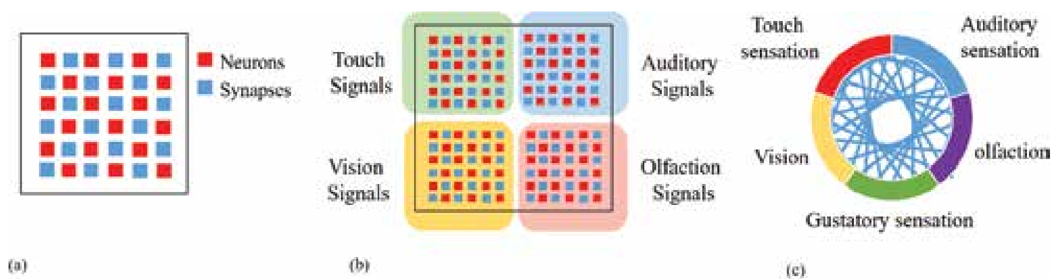

Figure 5. The neuromorphic computing architectures: (a) distributive neuromorphic computing architecture, (b) cluster neuromorphic computing architecture, and (c) associative neuromorphic computing architecture [13].

Thirdly, the human brain has a powerful unsupervised learning ability, which enables us to learn from our experiences. A well-known learning mechanism named associate memory is to associate different types of signals captured by various sensing organs together [22] so that it correlates these signals. Based on the CNCA, a novel architecture, we defined it with the name of associative neuromorphic computing architecture (ANCA), is proposed. **Figure 5(c)** illustrates this architecture. In this architecture, original signals captured from surrounding environments are processed in different regions. After that, the abstracted information would couple to each other to construct an associative natural network. The simplified ANCA with two neurons and one synapse has been investigated [25].

3. Neuron design

3.1. Neuron models

In the field of neuroscience, the research on the investigation of biological neurons has been continued in the past decade [26–31]. As discussed in Section 2, a neuron consists of four major elements, namely, dendrites, soma, axon, and synapse. Within the nervous system, signals are collected and transmitted to the soma by dendrites. The soma serves as the central processing unit where the nonlinear transformation carries out. When the input signal exceeds the threshold level, an output signal is generated, or so-called the firing process. The output signal is then transmitted along the axon, and to other neurons through the synapse. In a biological neuron, signals are in form of a nerve impulse, namely, action potential or spike [32].

When the signal, also known as the stimulus, from dendrites does not reach the critical threshold level, the membrane potential will leak out; otherwise, an action potential is generated. After the firing process takes place, the neuron will go through a refractory period, where the neuron is less likely to fire, and eventually reset to its initial state. This process is known as the firing and resting of a biological neuron, as illustrated in **Figure 6** [31]. Several well-known and representative neuron models are investigated, which include the integrate-and-fire (IF) model [26], Fitzhugh-Nagumo (FF) model [28], Hodgkin-Huxley (HH) model [33], and leaky integrate-and-fire (LIF) model [29]. The simplified electronic circuit representation of these neuron models is demonstrated in **Figure 7**.

3.2. Hodgkin-Huxley (HH) and Fitzhugh-Nagumo (FN) neuron model

Compared to the data that are extracted from the IF neuron, the HH neuron is found to be biologically meaningful and realistic [34]. The primary goal of the HH neuron is to mimic the electrochemical information transmission of a biological neuron [27]. **Figure 7(c)** demonstrates the simplified electronic circuit model of the HH neuron. The dynamic of the firing potential is described by a fourth-order nonlinear differential equation, which could be simplified as

$$C_m \cdot \frac{dV_m}{dt} = I_{ex} - g_i(h, m^3, n^4) \cdot \sum I_i(E_i, V_m), \tag{1}$$

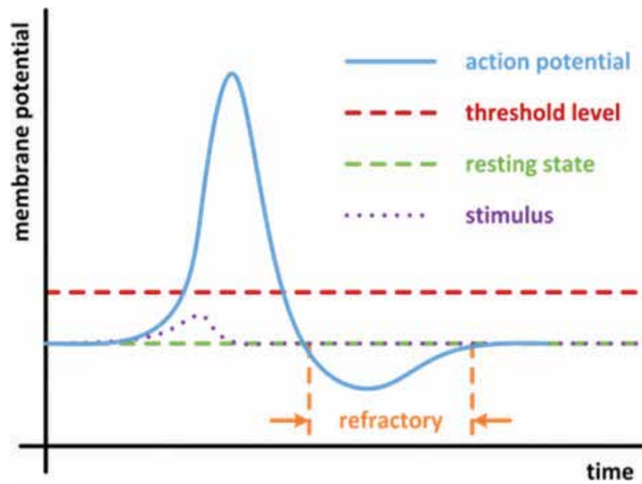

Figure 6. Action potential of a biological neuron.

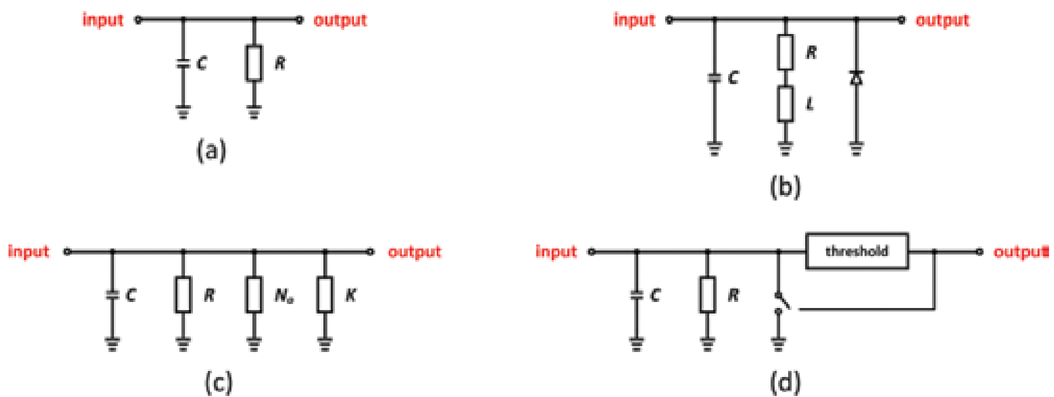

Figure 7. Simplified neuron models of (a) integrate-and-fire, (b) Fitzhugh-Nagumo, (c) Hodgkin-Huxley, and (d) leaky integrate-and-fire.

where g_i is the conductance parameter for different ion channels (sodium Na, potassium K, etc.), and $I_i(E_i, V_m)$ is the ion current with controlling variable as a function of time [33]. Although the HH neuron closely mimics the biological behavior of neurons, due to its design complexity, its electronic circuit model is not widely used in the hardware implementation, whereas the FN neuron is considered as the simplification of the HH neuron, as shown in **Figure 7(b)**. Its mathematical expression could be written as

$$\frac{dV_m}{dt} = V_m - \frac{V_m^3}{3} - w + I_{ex}, \tag{2}$$

where w is the linear recovery variable. Although the FN neuron reduces the four-dimensional set of the equations down to a two-dimensional one, the hardware implementation of the FN

neuron is still excessive challenging due to its high circuit design complexity inherent from its highly nonlinear behavior.

3.3. Leaky integrate-and-fire (LIF) neuron model

The LIF neuron model, as illustrated in **Figure 7(d)**, is constructed based on the traditional IF neuron. Its leakage property mimics the diffusion of ions that occur through the membrane when the equilibrium is not reached in the cell. The dynamic of the firing potential could be expressed as:

$$C_m \cdot \frac{dV_m}{dt} + I_{leak} = I_{ex}, \tag{3}$$

where I_{leak} is the leakage current. Similar to the traditional IF neuron, the membrane potential is initially charged up by the excitation current. An action potential is generated once the membrane potential exceeds the threshold level; otherwise, all charges will be leaked out. After the firing process takes place, the membrane capacitor in the LIF neuron will be fully discharged to the resetting state. Hence, the LIF neuron processes both firing and resting properties, which has an adequate resemblance to the biological neuron and relatively easier to implement using analog electronic circuits.

Compared to other neuron models, the LIF neuron plays a major role in the neuron design due to its compact structure, robust performance, and adequate resemblance to the biological behavior of neurons. The simplified analog electronic circuit model of the LIF neuron is demonstrated in **Figure 8**.

In the analog electronic circuit model of the LIF neuron, there are several key parameters that need to be carefully designed; for instance, the excitation current I_{ex}, the membrane capacitor C_m, the threshold level V_{th}, and the leakage current I_{leak}. In Eq. (4), the membrane potential is controlled by the excitation current and the leakage current, or vice versa. A simple resistor model is adapted to represent such relation; thus, Eq. (3) could be rewritten as

$$I_{ex} = \frac{V_m}{R_{leak}} + C_m \cdot \frac{dV_m}{dt}, \tag{4}$$

where R_{leak} defines the weighted resistance of the leakage current. By solving Eq. (4), the expression of the membrane potential could be determined as

$$V_m = I_{ex} \cdot R_{leak} - e^{\frac{t}{R_{leak} \cdot C_m}}. \tag{5}$$

3.4. Signal intensity encoding neuron

In order to model the input intensity-dependent firing characteristic of neurons [22, 35], the signal intensity encoding neuron (SIEN) is designed, as depicted in **Figure 9** [36].

In this design, the input current is transferred into a voltage signal by a transimpedance amplifier (TIA), such that the oscillating frequency of a current-starved-voltage controlled

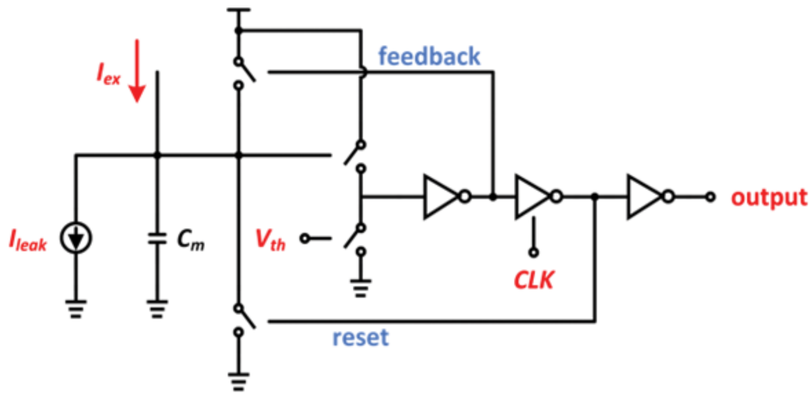

Figure 8. Simplified analog electronic circuit model of the LIF neuron.

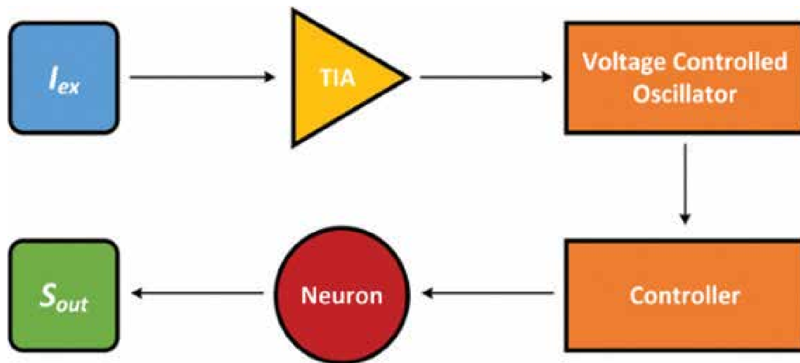

Figure 9. The diagram of the SIEN.

oscillator (VCO) can be regulated. The oscillating rate of the VCO is highly dependent upon integrated input stimulus signals. The final stage of the SIEN is formed by the parallel structure of a resistor and a capacitor to model charging and discharging behaviors of biological neurons, as depicted in **Figure 10**, whereas simulation results of the spiking signal are plotted

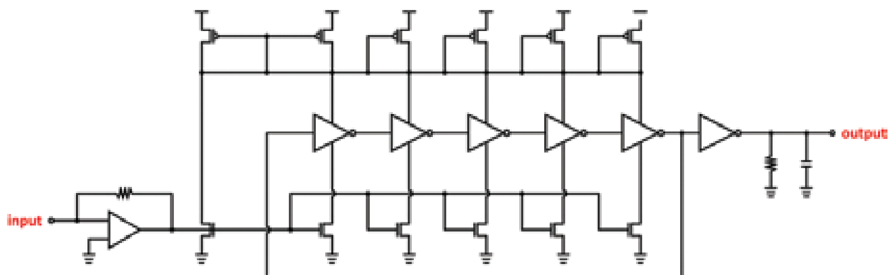

Figure 10. Simplified design scheme of the SIEN.

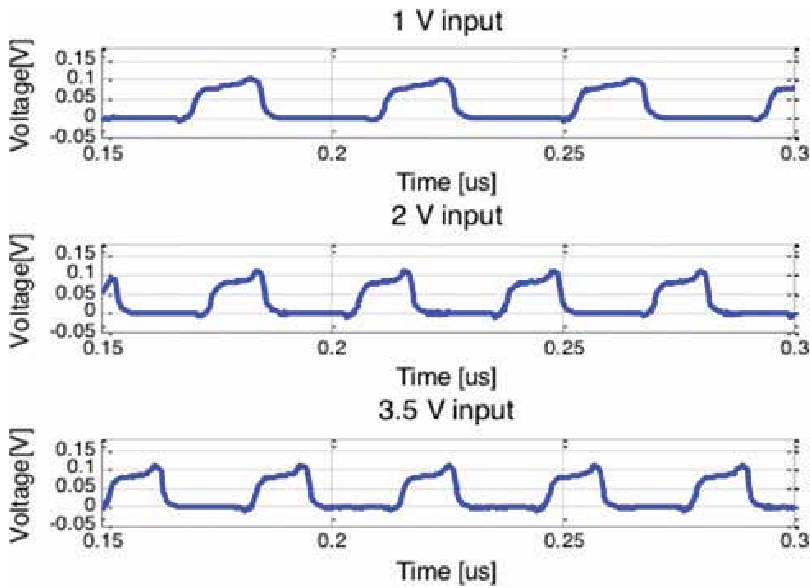

Figure 11. Spiking signals with respect to various stimulus voltage levels.

in **Figure 11**. In **Figure 11**, with higher input signal amplitudes, the firing rate increases correspondingly, which simulates the input intensity-dependent firing characteristic of the neurons in real biological systems.

4. Memristor as synapse

In the human brain, a synapse is defined as the structure connecting two neurons as shown in **Figure 12**. When a presynaptic action potential (spiking signal) approaches to the synapse, the chemical neurotransmitter molecules would be released to the synapse. The neurotransmitter would be diffused across from the presynaptic neuron cell to the postsynaptic neuron cell within the synapse. When the neurotransmitter arrived at the terminal of the postsynaptic cell, a spiking signal would be stimulated. The magnitude of the stimulated spiking signal

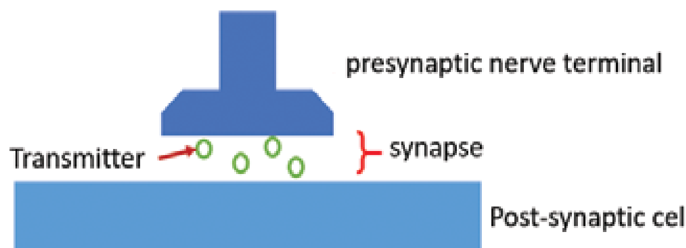

Figure 12. The structure of the synapse [22].

at the postsynaptic cell is highly dependent on the amount of the neurotransmitter received. A larger amount of neurotransmitter molecules stimulate a larger magnitude spiking signal, vice versa. In general, the large magnitude of spiking signal at the terminal of presynaptic neurons would stimulate more neurotransmitters. However, with the repeated stimulus in a short time (~hundreds of millisecond), the neurotransmitters released to the synapse from presynaptic neurons reduce gradually, which results in stimulating a smaller magnitude spiking signal in the postsynaptic neuron.

This phenomenon was investigated by Dr. Kandel's research on Aplysia [22]. In experiments depicted in **Figure 13**, the stimulus was repeatedly applied to the Aplysia's sensory neurons. When the constant stimulus was repeatedly applied to the sensory neuron multiple times (1, 2, 5, 10, 15), the magnitude of spiking signal stimulated in the response neuron ($L7_G$) decreases accordingly [22]. This indicates that the previous stimulus captured by the sensor neuron is somehow stored in the neural network system through modifying the connectivity strength between neurons. In Dr. Kandel's experiments, the neural network is relatively small that is only constructed by two neurons. The connectivity strength of the synapse is defined as the weight. The weight value can be modified in two directions (strengthen or weaken) by both excitatory and inhibitory stimuli. This feature is called as the plasticity of a synapse.

In order to physically realize the biological plasticity of a synapse, several features need to be satisfied. Firstly, the device should have only two terminals that are used for connecting the presynaptic and postsynaptic neurons, respectively. Secondly, the device should have a signal attenuation capability to mimic the plasticity of a synapse, and this capability should be reversible. All these features make the nanoscale two-terminal device memristor, also named as resistive RAM (RRAM), to be an ideal candidate for the electronic synapse implementation. The resistance of the memristor is reversibly programmable with the applied voltage pulse stimulus on its two terminals. When the voltage stimulus is applied on its two terminals, its resistance would be gradually changed between its low-resistance state (LRS) and high-resistance state (HRS). Typically, the memristor is constructed by the metal-insulator-metal (MIM) configuration as illustrated in **Figure 14(a)**. The decrease of resistance of the memristor is due to the formation of the conductive filament in the insulator layer. Transmission electron microscopy (TEM) photos of conductive filaments are demonstrated in **Figure 14(b)**. This breakdown phenomenon of the insulator can be recovered by applying

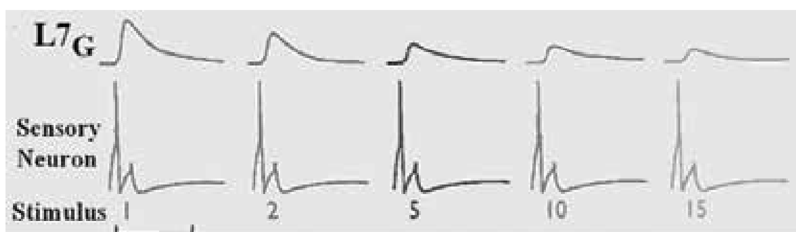

Figure 13. A sample of five identical action potential numbers 1, 2, 5, 10, and 15 along with the corresponding motor response signals of diminishing strength recorded at the motor neuron (identified by $L7_G$) (top) [37].

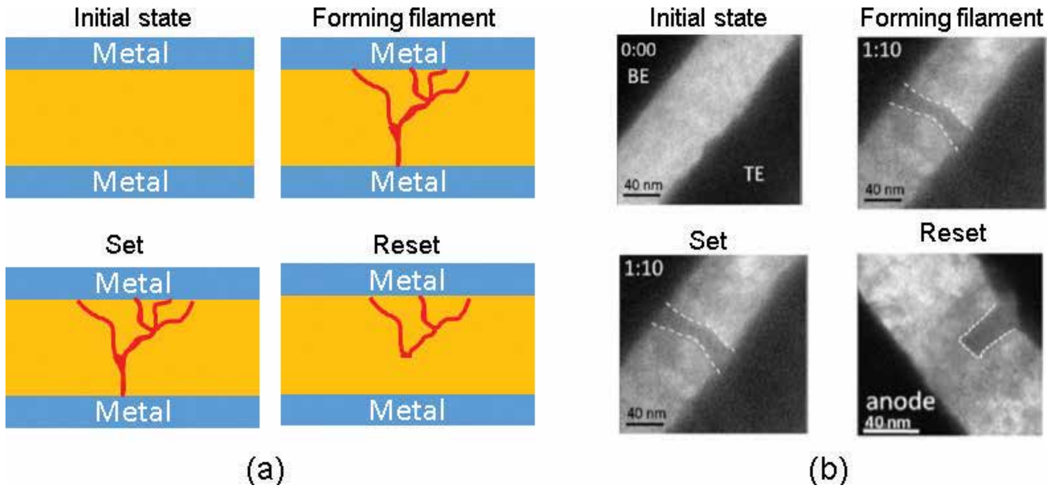

Figure 14. Illustration of the switching mechanism of a memristor: (a) switching process and (b) TEM images of the dynamic evolution of conductive filaments [38].

a reversed stimulus at the terminals, which consequently resets the memristor from its LRS to HRS. The physical mechanism of this reset behavior is the deconstruction of the conductive filament as illustrated in **Figure 14(b)**.

In general, the MIM structure of the memristor is fabricated massively in a 2D crossbar structure as depicted in **Figure 15**. In this structure, memristors are sandwiched between two layers of nanowires. The area of a single cell is $4F^2$, where the F is the minimum lithographic feature size dictated by technology node.

In order to further enhance the device density, the 2D crossbar structure of the memristor can be extended vertically into 3D space. There are two types of 3D RRAM (memristor) structures that can be used as 3D synaptic arrays: horizontal RRAM (H-RRAM) and vertical RRAM (V-RRAM), which are shown, respectively, in **Figure 16**.

In both structures, the area of the device size is $4F^2/n$, where n is the number of the stacked layers. The number of critical lithography masks for H-RRAM structure increases linearly with

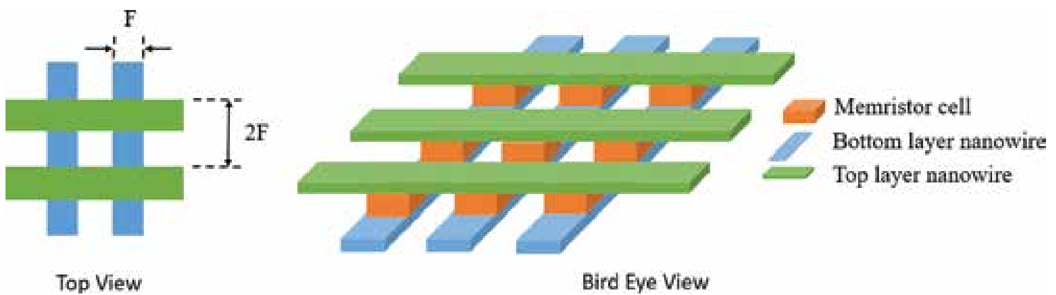

Figure 15. Two-dimensional crossbar structure of the memristor.

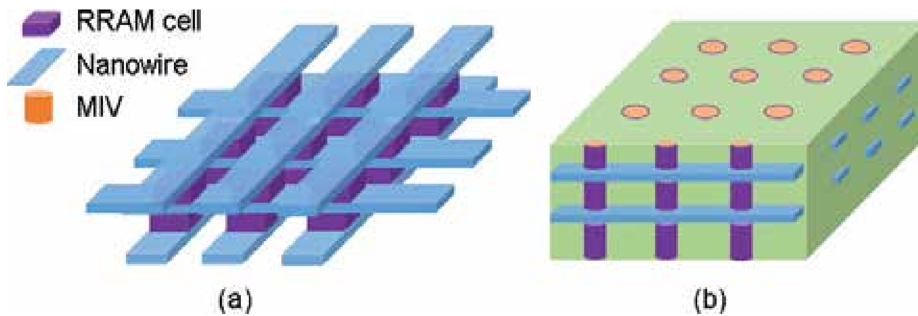

Figure 16. 3D RRAM integration structure: (a) horizontal 3D structure and (b) vertical 3D structure.

increasing number of the stacked layers, while the number of masks for V-RRAM is relatively independent of the stacking number. With increasing number of the stacked layers, V-RRAM becomes, even more, cost-effective [39, 40].

5. Memristive three-dimensional neuromorphic computing system

The recent fabricated neuromorphic chips implement neurons and synapses using traditional 2D CMOS and memory technology. In 2D placement methodology, a longer signal delivery distance is generally expected due to the routing density increment linearly with the number of connections, which inevitably increases die area, power consumption, etc. [41].

To address these limitations of the state-of-the-art neuromorphic chip designs, a novel 3D neuromorphic architecture is proposed to combine 3D-integrated circuit (3D-IC) technology with the memristor as the electronic synapse. Applying 3D integration technology to neuromorphic chips permits vertical routing paths of reduced nanoscale dimension, subsequently diminishing critical path lengths. It also decreases power consumption and shrinks die areas with high-complexity, high-connectivity, and massively parallel signal processing capability.

The benefits of applying 3D integration technology to neuromorphic chips design can be summarized as follows:

1. address the 2D neuron routing congestion problem, thereby increasing interconnectivity and scalability of the NC network and reducing the critical-path lengths [42],
2. allow numerous 3D interconnections between hardware layers that offer high device interconnection density, low-power density, and broad channel bandwidth using fast and energy-efficient links;
3. provide a high-complexity, high-connectivity, and massively parallel-processing circuital system that can accommodate highly demanding computational tasks.

The diagram structure of the proposed 3D neuromorphic computing (3D-NC) architecture is shown in **Figure 17(c)**. The multiple layers of the neural network can be implemented

through this structure. **Figure 17(a)** illustrates multiple layers of the neural network structure, in which the decomposed two layers are marked in a red box. These two layers of the neural network can be implemented through 3D integration technology, which fabricates the layer of memristor in the middle between two neuron layers as depicted in **Figure 17(b)**. Besides, with the similar structure of **Figure 17(b)**, a large scale of neural networks can be implemented by extending the 3D structure of two layers neural network repeatedly in a horizontal direction, which is demonstrated in **Figure 17(c)**.

In these structures, the electronic synaptic array implemented with memristors is not in a traditional crossbar structure (**Figure 18(a)**), which suffers the sneaking path issue. The sneaking path is an undesired current path from the adjacent memristor cells marked as the white arrows in **Figure 18(a)**. In order to eliminate this issue, the horizontal nanowires, which are used for reading/writing access, are physically disconnected in the design. Meanwhile, reading/writing access ports are located on the upper and bottom layers. Without electrical connections between adjacent memristor cells, the sneaking path issue can be fundamentally addressed.

Two 3D integration technologies have the potential for implementing the 3D-NC architecture in **Figure 17(c)**, which are TSV (through-silicon via)-based and monolithic-based 3D integration technologies. The 3D integration technology with TSVs as vertical electrical connections has been studied for many years [19]. For TSV-based 3D integration technology, transistors are initially fabricated at separated wafers by traditional CMOS technologies. After that, two wafers are bonded together. In general, the capacitance between TSVs is large, which can cause capacitive coupling issue in a high-speed circuit. However, they can be used for implementing the capacitance in neuron models, resulting in further reduction of the chip design area [43–45]. However, there are several technical challenges for the TSV-based 3D integration technology. Firstly, wafers need to be thinned to make the metal contact from TSVs for

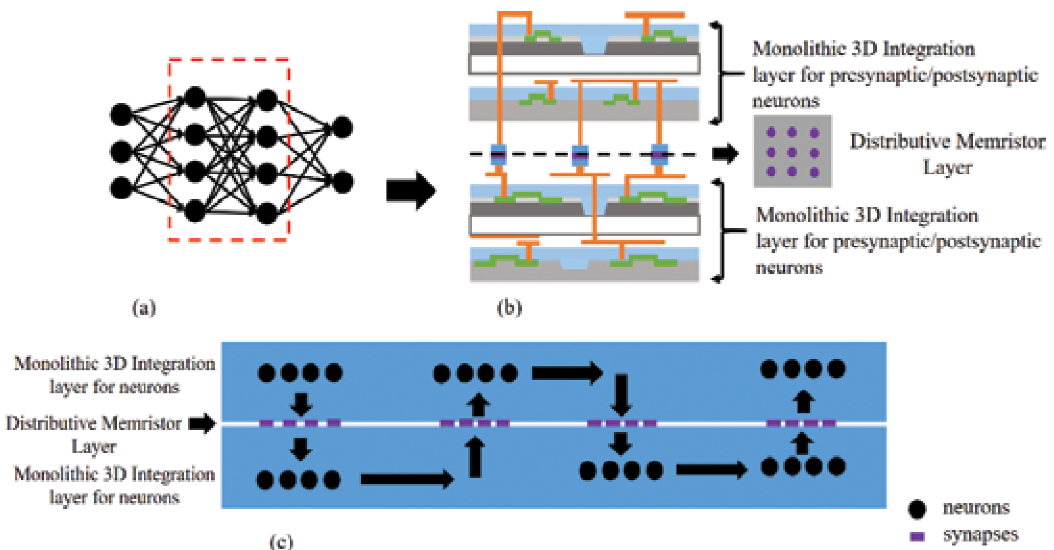

Figure 17. 3D neuromorphic computing architecture (a) Deep neural network, (b) 3D structure of two layers of neural network and (c) 3D structure of multiple layers of neural network.

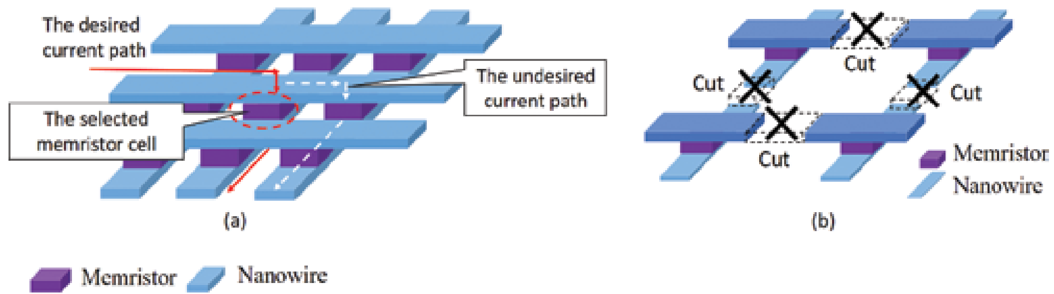

Figure 18. (a) The traditional crossbar structure of memristors and (b) disconnecting the horizontal connecting nanowire.

3D device	FinFET	Epi-like Si NWFET	Epi-like Si UTB	SOI-Si UTB	Poly-Si/Ge FinFET	IGZO OSFET
Thermal budget °C	<400	<400	<400	<650	<400	<500
I_on/I_off	$>10^7$	$>5 \times 10^5$	$>5 \times 10^5$	$>10^7$	$>10^7$	$>10^{21}$

Table 1. The emerging transistors with low-fabrication temperature [46].

the bonding process. In these thinning processes, a lot of charges would be accumulated. These charges potentially cause electrostatic discharge (ESD) issue that can damage chips in bonding processes. Secondly, bonding the microscale TSVs needs extra effort to align them precisely. To overcome these challenges, another more aggressive 3D integration technology is proposed, which is called monolithic 3D integration. Unlike the TSV-based 3D technology, which uses a separate fabricate processes, the monolithic 3D technology integrates different layers of devices at a single wafer with nanoscale intertier vias serving as vertical connections. Due to the monolithic fabrication procedure, this 3D integration technology fundamentally eliminates the thinning and bonding processes. On the contrary, the main challenge for the monolithic 3D integration technology is the low-temperature fabrication constraint for upper layers, since the high fabrication temperature in upper layers would damage the lower layer transistors previously fabricated. This low-temperature requirement restricts the traditional CMOS transistor (fabricates at more than 1000 °C) that does not fit the requirements for the upper layer circuitry implementation. Fortunately, several low-temperature transistors are the potential candidate to fit this requirement, such as FinFETs [46], carbon nanotube FETs [47, 48], etc. **Table 1** summarizes state-of-the-art transistors that are fabricated at low temperature and potentially can be employed in the monolithic 3D integration technology [46]. With these emerging technologies, the monolithic 3D-NC with memristors as electronic synapses is becoming the most promising next-generation non-von Neumann computing platform.

6. Conclusion

The conventional concept of the neuromorphic computing is to physically rebuild brain-like neural networks through very-large-scale integration (VLSI) [3]. In this chapter, we introduce a possibility to use an emerging device named memristor as an electronic synapse to construct

a memristive neural network of the neuromorphic computing system, consequently, achieving a much smaller design area and power consumption. In this chapter, we also comprehensively analyze functions of the biological synapse in cellular level and further introduce the reasons that memristor can be considered as an electronic synapse. In architecture level of neuromorphic computing, we introduce three novel architectures that are fundamentally different from the traditional von Neumann architecture by locating the computing units (neurons) and memory units (synapse) distributedly. The realization of these three neuromorphic computing architectures potentially is a roadmap for implementing a power-efficient artificial intelligent system with self-learning capability.

Furthermore, the memristive neural network is generally implemented in the two-dimensional design method. In this chapter, we introduce and discuss a novel hardware implementation trend that combines memristor and 3D-IC integration technology; such technology has the capabilities to reduce the system power consumption, provide the high-connectivity, resolve the routing congestion issues, and offer the massively parallel data processing capability. Moreover, the design methodology of applying the capacitance formed by the through-silicon vias (TSVs) to generate a membrane potential in a 3D neuromorphic computing system is discussed in this chapter.

Moreover, there are several challenges that hinder the employment of the memristors as the electronic synapse, e.g., the reliability, variability, endurance, etc. Additionally, fabrication techniques of lower temperature transistors (FinFET, carbon nanotube FETs, etc.), which can be integrated monolithically on the top layers, demand further research effort to demonstrate the memristive 3D neuromorphic computing system discussed in this chapter. The proposed novel neuromorphic computing architectures (DNCA, CNCA, and ANCA) are considered potentially to be the roadmap for achieving a self-learning artificial intelligence that can directly learn from the surrounding environment and be adaptive to it. However, mathematical foundations of these architecture concepts are still unclear and missing, which need further investigations in future.

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Memristive Anodic Oxides: Production, Properties and Applications in Neuromorphic Computing

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Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.79292

Abstract

Memristive devices generally consist of metal oxide elements with specific structure and chemical composition, which are crucial to obtain the required variability in resistance. This makes the control of oxide properties vital. While CMOS compatible production technologies for metal oxides deposition generally involve physical or chemical deposition pathways, we here describe the possibility of using an electrochemical technique, anodic oxidation, as an alternative route to produce memristive oxides. In fact, anodization allows to form a very large range of oxides on the surface of valve metals, such as titanium, hafnium, niobium and tantalum, whose thickness, structure and functional properties depend on process parameters imposed. These oxides may be of interest to build neural networks based on memristive elements produced by anodic oxidation.

Keywords: titanium dioxide, tantalum oxide, hafnium oxide, niobium oxide, memristor, resistive switching, anodizing

1. Introduction

Although still dominated by silicon technology, information storage devices—and more generally speaking nanoelectronic devices—are now facing the challenge of finding new materials and paradigms, in order to further improve features such as computation and write speed, data density, operation voltages, and fabrication costs. A variety of alternatives to traditional information processing devices have been proposed, boosting new scientific research in semiconductor principles and technologies [1]. In this frame, memristors—or resistive switching

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materials, as the two terms identify the same switching behavior [2, 3]—were identified as valuable candidates for alternative nanoelectronic devices [4–7], with particular reference to nonvolatile memories and neuromorphic applications.

Indeed, several oxides are capable of resistive switching, that is, their resistance can be switched through a suitable voltage pulse between at least two different values—a high resistance state, HRS, also addressed as OFF state, and a low one, LRS, identified as ON state, by operations of "set" (OFF-ON) and "reset" (ON-OFF). Among them, SiO_2 [8, 9], TiO_2 [3], HfO_2 [10] and Ta_2O_5 [11] are the most studied.

Oxide properties—thickness, composition, stoichiometry and defectiveness—are crucial to determine whether it shows memristive properties, and the values of main switching parameters. Hence, the production technique plays a major role, as in turn it determines oxide characteristics; yet, the most commonly employed oxide synthesis/deposition techniques imply high investment costs and rather long deposition times to achieve satisfactory results.

We here present and summarize current knowledge on the growth of oxides with resistive switching capability by anodic oxidation, a low-cost electrochemical technique that may find a new niche of application in the production of memristive metal oxides. In Paragraph 2, the principles of anodic oxidation are described to highlight the typical oxide characteristics that can be achieved. The discussion will be limited to thin oxide layers, and no reference will be made to thicker ceramic oxides produced in sparking regime, as they are not pertinent to the present application [12]. Paragraph 3 provides a comparison of the characteristics of different metal oxides that show memristive properties, focusing on those that can be obtained by anodic oxidation, and then specifically focuses on anodic oxides. Finally, in Paragraph 4, the potential application of these materials in neuromorphic computing is discussed.

2. Anodic oxidation

Generally speaking, Ti, Hf, Ta, Zr and, valve metals are potential candidates to be anodized. Anodic oxidation is an electrochemical technique that allows to grow nanometric oxide films at a metal surface, with controlled chemical composition, structure and thickness that are defined by properly choosing the relevant electrochemical parameters—cell voltage, electrolytic solution, process time [13–15].

The technique consists of polarizing the metal by imposing a current flow between the specimen and a counterelectrode immersed in a suitable electrolyte. Metal atoms are oxidized to cations, which progressively combine with oxygen (or oxygen-containing) anions from the electrolyte to form an oxide layer that deposits on the metal surface. It is both an inward and outward growth mechanism, with a slight predominance of O^{2-} charge carriers transport across the oxide to reach the metal surface where metal cations are produced, owing to the higher mobility of oxygen anions with respect to metal cations [14]. Given a determined metal or metal alloy, oxide characteristics are then determined by the set of anodizing parameters: electrolytic solution composition, concentration and temperature; feeding voltage; method of voltage application (galvanostatic, potentiostatic, potential ramp). Two main classes of anodic oxides are of interest to obtain memristive behavior and will be described in the following,

namely, compact thin films and nanotubular films; the switching behavior of anodic oxides will be addressed in Section 3.3.

2.1. Thin compact films

Ion migration that allows oxide growth during anodizing takes place in a solid film tens, or hundreds, of nanometers thick; therefore, it is associated with very high electric fields, in the order of 10^7 V/cm. To achieve such conditions, current densities of some tens or hundreds of A/m^2 are used, and cell voltages to produce thin compact films are between 10 and 100 V [12, 16]. A very large number of electrolytes can be employed, from diluted acids to neutral salts, to alkaline solutions [17–19]. Such oxides generally show an amorphous, or predominantly amorphous, structure, especially at low voltages, where only some non-stoichiometric crystal phases like Magnéli phases may appear.

Oxide thickness increases linearly with applied cell voltage: anodizing ratios are in the range of 2 ± 0.5 nm/V depending on metal composition, electrolyte and growth mode—either galvanostatic or with potential ramp [12, 17–19]. The thicker the oxide already formed, the more onerous its further thickening: indeed, at growing voltages—and hence oxide thicknesses—other parasitic processes may kick in, consuming part of the current supplied to the electrode. As a consequence, if the amount of charge employed in the process is used to estimate oxide thickness by coulometry [20, 21], the so-calculated thickness is affected by parasitic reactions, since a portion of current is dissipated, mostly in oxygen evolution, to an increasing extent with increasing cell voltage (**Figure 1**) [19, 20]. Most of research studies on the growth of thin films by anodic oxidation refer to titanium and its alloys and to aluminum [12–14, 22–25], given their relevance in already mature industrial applications. Some works are also proposed on other metals, such as zirconium, niobium, hafnium; yet, they generally focus on the obtaining of high specific surface area morphologies, such as nanotubes [26], which are described in next paragraph.

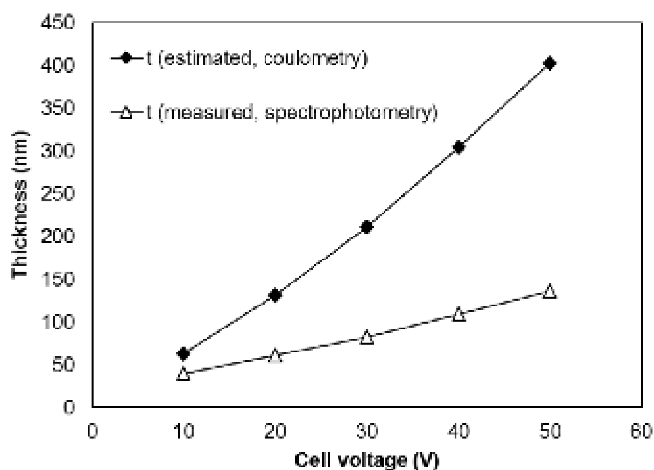

Figure 1. Thickness versus voltage curve of a typical galvanostatic anodic oxidation process performed in acid electrolyte: Measured oxide thickness grows linearly with voltage, while coulometry exponentially overestimates thickness due to parasitic reactions.

2.2. Nanotubular films

In the presence of aggressive species that are capable of localized dissolution of the growing oxide, nanotubular films can be grown, as shown in **Figure 2**. The peculiar morphology is associated with the simultaneous electrochemical growth of the oxide and its chemical dissolution operated by fluoride ions or, less frequently, other halogen ions. To achieve the formation of a nanotubular layer, a potentiostatic process is applied, where the chosen cell voltage—in the range 20–120 V—is maintained constant for various times, from few minutes to few hours [27, 28].

These nanostructures are usually developed on valve metals for applications in fields where an enhanced specific surface area is required, that is, in photocatalysis, photovoltaics, hydrogen production and sensing, where having the largest possible number of active sites of the oxide able to interact with the surrounding environment increases the material functional efficiency [27, 28]. Nevertheless, resistive switching capabilities were identified also in these nanostructures, as will be discussed in detail in Section 3.3.

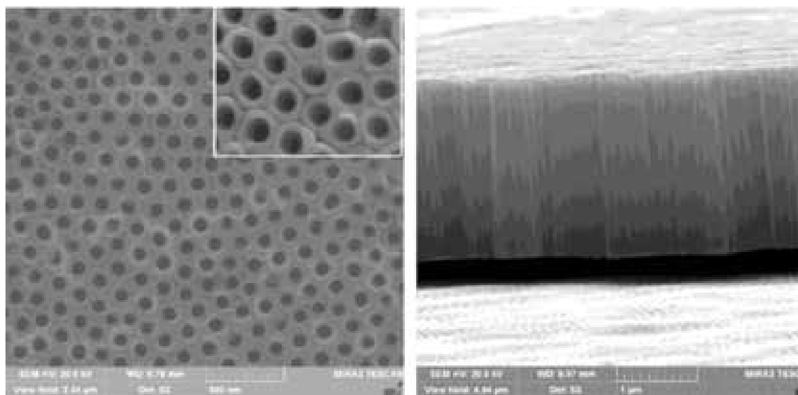

Figure 2. Top and cross-section view of TiO_2 nanotubes grown by anodic oxidation of the titanium substrate in organic electrolytes. Adapted with permission from Ref. [29].

3. Memristive metal oxides

3.1. General considerations and parameters of interest

Different switching mechanisms are observed in metal oxides—and even other mechanisms are envisioned for other materials, such as chalcogenides or polymers, which we will not refer to:

- the drift of oxide lattice defects, mostly oxygen vacancies, with consequent change in oxide valence, either localized on a restricted area called filament (**Figure 3**), or distributed over the whole area following an interface model (valence change mechanism, VCM);

- a change in stoichiometry induced by heating (thermochemical mechanism, TCM);
- the formation of conductive filaments by migration of ions from an active electrode metal and their deposition at the counterelectrode (electrochemical metallization mechanism, ECM, also called conductive bridge, CB) under the applied electrical field [4].

The most easily occurring switching mechanisms common to all metal oxides are VCM and ECM. Yet, mixed filamentary switching mechanisms, both by electrode ions migration and metal oxide reduction due to vacancies migrations, have been observed in the literature, as shown in **Figure 4**, where the two filament formation mechanisms are described [31]. Given the wide variety and complexity of switching mechanisms observed, we suggest to refer to specific reviews for a detailed explanation of the physics behind specific resistive switching mechanisms in memristive oxides [4, 32–34].

As already mentioned in the Introduction section, resistive switching implies the modification of the metal oxide of interest from a high resistance state (HRS) to a low resistance one (LRS), and vice versa (**Figure 4**). Conventionally, a set event is described as the switch from HRS to LRS, while reset, that is, restoring the initial high resistance of the oxide, causes the passage from LRS to HRS. Both events are driven by an electrical input, and more specifically by the application of a voltage. If set and reset require the application of reverse polarity, then the switching is defined bipolar, while in unipolar switching, the direction of change in resistance state depends on voltage amplitude, not on its polarity. Yet, materials usually do not show immediately a switching behavior: a first stage called electroforming is required, operated at higher voltages, which triggers the material switching ability, making subsequent cycles easier and occurring at lower voltages [35, 36]. Indeed, reset operations only allow to recover and redistribute defects (vacancies, electrode metal ions) at the oxide-electrode interface, while a conductive path remains pre-set in the inner part of the oxide [5, 37].

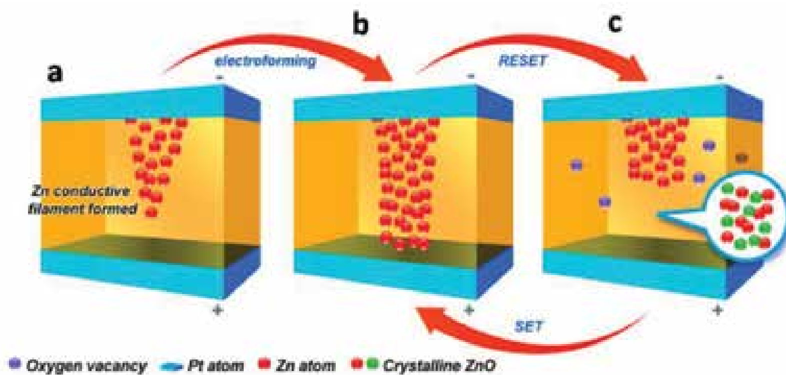

Figure 3. Schematic diagram for the mechanism of resistive switching in Pt/ZnO/Pt devices. (a) the migration of oxygen vacancies toward the cathode (oxygen ions (O^{2-}) toward the anode) and rearrangement of Zn-dominated ZnO_{1-x} leads to the formation of a conductive filament (b). (c) the rupture of the filament by joule heating. Owing to the migration of oxygen ions, the ReRAM resets back to the off state. Reprinted with permission from Ref. [30].

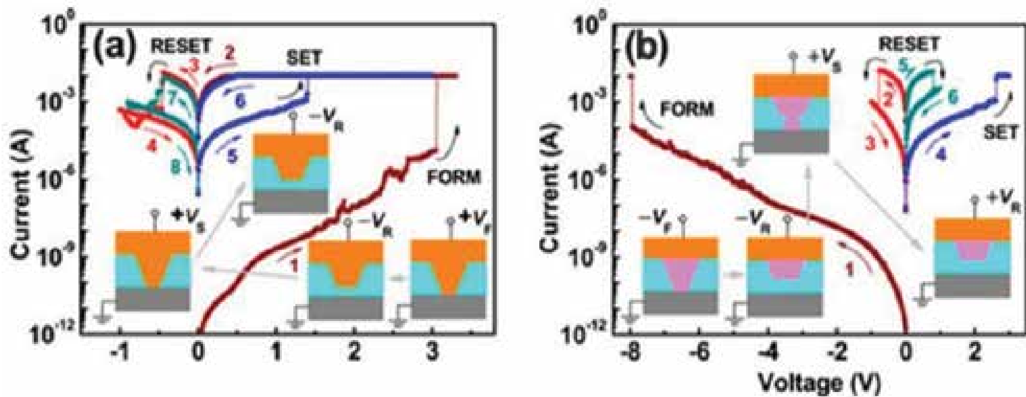

Figure 4. Four different operation modes for cu/ZnO/Pt in which the resistive switching originates from the formation and rupture/annihilation of (a) Cu, (b) Zn filaments. The insets schematically show filament evolution processes. Adapted with permission from Ref. [31].

The voltage applied in the electroforming step is larger than that needed in set/reset operations (**Figure 4**): the electroforming voltage in many cases is as high as a few volts and linearly dependent on oxide thickness [38–40]. Efforts are being made to produce forming-free devices; unfortunately, this is most often obtained by decreasing film thickness, which at the same time increases its defectiveness, reducing device reliability. The voltages that are required to operate the device are relevant as well: the key parameters are the write voltage, V_{wr}, and the read voltage, V_{rd}, which determine the entity of the signals required during the whole device operation. The write voltage is less dependent—in some cases even independent—on oxide thickness, as it only needs to recreate the conductive region at the oxide-electrode interface, and should be in the order or few hundred mV to allow good device efficiency and low energy consumption, while the read voltage is usually one order of magnitude lower to avoid possible undesired changes of resistance state during read operations.

When describing and comparing materials with memristive capabilities, another fundamental parameter is the R_{off}/R_{on} ratio, that is, the ratio between material resistance in the HRS vs. LRS, which gives an indication on the efficiency and robustness of switching. Indeed, although ratios of few units are theoretically sufficient to operate a device, a R_{off}/R_{on} ratio higher than 10 is generally recommended, to avoid uncertainties in read operations and improve reliability [4].

Another important touchstone parameter is endurance, that is, the number of cycles applicable to the material without loss of switch and no (or better, limited) decay of R_{off}/R_{on} ratio.

One last characteristic can play a major role, especially in neuromorphic computing, that is, the possibility to achieve multilevel storage, which makes the difference between binary and analog switching. This can be achieved either by multiple resistance states [41–44] or by encoding information not only in the conductive filament size, which rules resistivity, but also in its orientation through complementary switching [45, 46]. These aspects will be addressed in Paragraph 4.

3.2. Dependence of switching behavior on metal oxide characteristics

As anticipated, this section compares the switching behavior of metal oxides that hold an interest in the frame of anodic oxidation, that is, the discussion is focused on oxides of metals that are liable to anodizing. These include titanium, niobium, tantalum, hafnium, and zirconium. Oxides are often indicated as TiO_{2-x}, NbO_x, TaO_x, HfO_{2-x}, ZrO_{2-x} to take non-stoichiometry into account.

On these metal oxides, either filamentary switching or interfacial valence change has been observed, depending on oxide composition, production method, and metal electrode composition. Interestingly, a unified model was proposed: to be integrated in CMOS technology, feature size will be decreased more and more, until reaching the actual size of a filamentary conduction path—which would then occupy the whole component area [34].

When the formation of oxygen vacancies (or metal precipitates) filaments is involved, the localized current percolation path preferentially locates at grain boundaries or lattice inhomogeneities, as revealed by C-AFM and TEM measurements reported in several works (see for instance [47–49]) and represented in **Figure 5**. Moreover, multiple resistance states can be obtained and explained by considering two directional movements of vacancies: from one electrode to the other, crossing the whole oxide thickness, to generate the filament; and a lateral one, to increase filament size or create new filaments [50, 51]. From a material point of view, multiple states can be seen as a gradual increase in non-stoichiometry. As an example, for TiO_2, the memristive behavior is generally ascribed to the movement of vacancies that gradually create an oxygen depleted layer with composition TiO_{2-x}, which gains conductivity for $x > 1.5$ [52], hence the higher the quantity of vacancies formed, the wider the area that reaches low resistance conditions, which allows a gradual change in LRS that can be exploited to produce multistate devices.

Yet, grain boundaries and other structural inhomogeneities related to crystalline oxide structures may strongly affect actual device performances: in fact, grain boundaries not only make switching easier, as abovementioned, but also cause a decrease in R_{off}/R_{on} ratio, plus they alter performance evaluation with respect to single crystal devices of envisioned nanometric size. Hence, amorphous layers are often preferred, given their enhanced reproducibility and

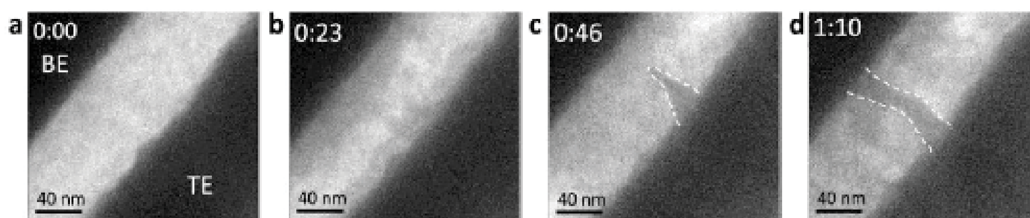

Figure 5. A series of in situ TEM images clipped from the video. (a) At the start of recording, the ZnO was in the initial state. (b) When voltage was applied, the contrast of ZnO enhanced near both electrodes. (c) A conical-shaped filament generated near the top electrode. The white dashed line highlights the filament. The specimen was still in the high-resistance state. (d) The columnar filament passed through the ZnO film connecting the top and bottom electrodes. Adapted with permission from Ref. [30].

better long term stability with respect to polycrystalline ones: these properties, ascribed to the material structural homogeneity, nicely match with an easier production with respect to single crystal oxides [53–55].

More recently, low-cost processes have been successfully employed to produce resistive switching oxides, including solution processing—sol-gel, hydrothermal synthesis—and electrochemical techniques, both electrodeposition and anodic oxidation. The former set of techniques has the advantage of producing oxides free of substrate, hence they can be deposited on any substrate, including flexible ones [56–58]. Production of the oxides generally involves mild temperatures and ambient pressures in case of sol-gel [57, 59–62], or the use of a pressurized vessel, specific for hydrothermal treatments [63–65], which in all cases represent low-cost alternatives to low pressure, high-temperature chemical or physical deposition processes.

On the other hand, the absence of a substrate implies an immobilization step—which can be performed by drop-coating, inkjet printing, and other methods—that may introduce a further level of inhomogeneity in the final device properties. Indeed, oxide particles need to be dispersed in a proper solvent, which must then be completely removed: defects such as porosities due to solvent removal, or even residual solvent may then arise. To improve homogeneity, often multiple deposition steps are performed, which increases overall film thickness and consequently electroforming voltage [59], while oxygen or argon plasma etching can be employed to introduce oxygen vacancies in the as-deposited materials, hence reducing electroforming voltages or even eliminating the need for this step [60, 66–68]. The possibility of applying multiple coating steps also opens the way to sol-gel processed double-layer structures [69], which brings potential benefits that span from increased endurance to reduced power consumption [44, 70–72]. For instance, in TiO_2-based memristors oxygen vacancies migration can lead to oxygen gas evolution at the anode, which irreversibly compromises the oxide stoichiometry: the presence of a blocking layer can act as sink of oxygen ions and limit currents involved, avoiding oxide breakdown [3, 73, 74].

Concerning the switching type, both unipolar and bipolar switching can be observed within the same material [75, 76]: which of the two is operating can be associated at a first approximation with different reset processes, being thermal dissolution the prevailing one for unipolar behavior, and ionic migration responsible for bipolar switching ([5] and references therein: [77–79]).

3.3. Anodic oxides showing memristive behavior

The choice of anodic oxidation to produce memristive elements is driven by a number of benefits over current technologies, first of all its low cost, non-vacuum and low-temperature characteristics. Moreover, it allows to produce amorphous oxides with nonstoichiometric composition [14, 49, 80], that is, already containing a non-negligible amount of oxygen vacancies, and characterized by higher density compared with sputtered films, where residual porosity is intrinsic to the production technique [81]. Eventually, anodizing allows fast oxide growth: to obtain a metal oxide few tens of nanometers thick, the general duration of an anodizing process is in the order of few seconds, and it can be performed with a relatively

low power equipment (voltage scale 0–30 V, current scale 0–100 mA) in a neutral solution of non-aggressive salts [17]. Another advantage is the possibility to use the same metal substrate as a back-end material, that is, one of the two electrodes is intrinsically integrated in the component. Currently, the biggest drawback that limits applications of anodic oxidation is the minimum device size: the technique is generally employed on full surfaces, thus not allowing the growth of space-confined nanometric or sub-micrometric pads, and the only method to reduce the size of the anodized spot is to apply insulating masks that avoid electronic contact of the metal with the electrolyte.

Keeping in mind these important general features, we here summarize current research on anodic oxides showing memristive characteristics.

The first indication of anodic oxides presenting memristive behavior was recorded on titanium oxides grown in a water-glycerol-based ammonium fluoride solution at 30 V. No clear morphological characterization of the oxide is made; yet, although the presence of fluorides may indicate typical conditions of nanotubes production, the short anodizing times applied allow to presume the growth of a compact oxide, some tens of nanometers thick. Interestingly, annealing has a detrimental effect on the memristive behavior. This is ascribed to the exceeding formation of oxygen vacancies that creates ohmic contacts; in addition, annealing is known to induce crystallization in anodic oxides which—in the anodizing conditions considered—would show amorphous structure in the as-prepared state [82]. This may have as well a role in the degradation of resistive switching. Other compact oxide films showing memristive behavior were then grown on titanium as well as on niobium and tantalum: anodizing in diluted phosphoric acid at 25 V, corresponding to an oxide thickness of approximately 60 nm, was found to allow the achievement of the best switching behavior [83].

The cited works all based their considerations on macroscale samples. A nanoscale characterization of anodic titanium oxides was performed by means of conductive atomic force microscopy (C-AFM), which allowed to assess the electrical properties of nanometer-size spots on the oxide surface: results indicated that oxide properties are far from being homogeneous, with resistive switching spots embedded in a nonconductive matrix and located mostly at grain boundaries [49]. More recently, efforts were made in the direction of producing real devices and testing the material at the microscale. Anodizing was performed on tantalum [81] and on titanium [84] metallic films deposited on glass, in borate buffer solution or in diluted phosphoric acid, respectively, at cell voltages of 5–20 V. Micrometer-size conductive metal pads (either Pt or Cu) were then deposited by lithography, allowing better characterization of the devices, which also included endurance evaluation.

In all abovementioned cases, the anodic oxides showed parameters compatible with requirements identified for resistive switching materials: high R_{off}/R_{on} ratio (> 10, with best values in the order of 80), set/reset values lower than 1 V and possibility to obtain multilevel switching [81]. Moreover, in several works, the oxides produced were electroforming-free: this can be ascribed to the anodic oxidation process itself, which is known to generate non-stoichiometric oxides, therefore the content of oxygen vacancies natively present in the oxide is already sufficient to produce the switching [49, 83, 84].

In this respect, metal electrode ions injection has also been proposed as a possible mechanism for the onset of switching, which would indicate the establishing of a CB mechanism [81]. Nevertheless, proofs of the actual onset of a VCM are provided through the observation of switching with C-AFM measurements, where no top electrode is present: analyses have been conducted both on the top surface of the anodic oxide [49], and on a lateral device, where no electrode metals are available [85].

Memristive nanotubes were also produced on titanium [86–88]. In these cases, either longer anodizing times (hours) and/or higher voltages (up to 120 V) are required, and thicker oxides, some hundreds of nanometers thick, are achieved. Yet, the limited adherence and mechanical stability of these oxides compared with compact ones, and the higher thickness introduced, make them less appealing for real applications.

4. Applications in neuromorphic computing

Recent implementations of emerging computing capabilities leverage on the capability offered by non-volatile memory (NVM) storage and information processing. Two main approaches have been proposed:

- Hybrid logic/memory integration: the logic and the memory layers are implemented in two different substrates or levels, typically an Application Specific Integrated Circuit (ASIC) is developed to emulate artificial neuron functionality while memory layers are integrated either on a separate chip or occupy a separated area. The main advantage lies in the improved communication bandwidth between the different logic and memory layers.
- Logic-in-memory: memory elements are distributed in a circuit to play a role in the realization of the logic operations, aiming both at ultra-low power and highly expressive logic circuits. Thus, general-purpose computation functions can be implemented by configuring non-volatile switches. NVMs are naturally suited for performing implication logic instead than standard logic. Recently, stateful logic operations, for which memristor devices work as gates and latches that use resistance as a physical state variable, have been demonstrated [89].

Energy efficiency benefits of array computing have also been demonstrated with various technologies (including spin-torque oscillators) in relatively small-scale circuits. For example, in [89], a data clustering algorithm mapped to a memristive array was demonstrated. In [90], the FPAA architecture was used to implement neuronal array-based sparse coding, applicable in the early stages of visual processing. Furthermore, integration of memristors and an FPAA circuit was demonstrated in small scale in [91]. Cognitive computing algorithms, which can be mapped to array processing/associative memory architectures, have also been described [92–94]. However, hardware architectures and design tools to realize these algorithms energy-efficiently on a relevant scale do not currently exist.

The challenge in the application of memristor technology for large-scale memory-based computing architectures is the development of new physical device models for memristor devices

http://dx.doi.org/10.5772/intechopen.79292

and analyzes the adaptation of algorithms with respect to device variation and scalability. Since the discovery of memristive behavior at the nanoscale at Hewlett Packard laboratories in 2008, the scientific community has devoted a large deal of efforts to derive suitable models that capture the nonlinear dynamics of memristors. Pickett's model is a reference model that is well suited for describing the physical mechanisms at the origin of memristor dynamics. Simplified versions aiming at fitting the behavior of Pickett's model are the TEAM and V-TEAM models, Biolek's model and the boundary condition model for a comprehensive review [95]. It is worth noting that such models are not oriented toward nonlinear circuit synthesis. In order to effectively analyze the dynamic behavior of memristors, and also in view of their simulation and emulation, it is fundamental to develop circuit memristor models, that is, models obtained by interconnecting basic nonlinear blocks. This will be pursue along the lines of the general method for device modeling in [96] and exploiting recent techniques for the identification of switching and PWA (piece-wise-affine) systems.

There is an increasing interest in the implementation of oscillators using nanoscale devices as memristors. As remarked in [97], a source of controllable chaotic behavior that can be implemented by a single scalable electronic device and incorporated into a neural-inspired circuit may be an essential component of future computational systems. In this framework, the memristor is required to display a quasi-static voltage-current characteristic with a negative differential resistance (NDR). Various classes of relaxation oscillators displaying a tunable range of periodic and chaotic self-oscillations have been implemented during recent years and their importance in neuromorphic applications, such as pattern recognition and signal processing tasks in real time, have been demonstrated. They can also be used as core devices with a rich variety of nonlinear dynamics within the framework of reservoir computing architectures. Work so far has been mainly based on experimental and phenomenological observations of oscillations and complex phenomena, while a circuit model and a clear analytic understanding of the underlying nonlinear dynamics and bifurcations is basically missing. Recently, a new method, named Flux-Charge Analysis Method (FCAM), has been developed to effectively analyze a wide class of nonlinear circuits containing ideal memristors in the flux-charge domain [98]. FCAM permits to bring back the dynamic analysis to that of a lower-order circuit, with respect to that in the standard voltage-current domain, using flux and charge as state variables. This enables to obtain a clear picture of the dynamical behavior displayed by memristor circuits. In particular, some peculiar aspects, such as the presence of invariant manifolds and the coexistence of different dynamics for the same set of (fixed) circuit parameters, are singled out. Also, it is possible to assess the presence of a new interesting phenomenon of bifurcations which emerge without changing the system parameters, namely, bifurcations due to changing the initial conditions for the state variables for a fixed set of circuit parameters (BWP) [99]. Using FCAM, the dynamics of classes of oscillators and chaotic circuits with ideal memristors have been deeply analyzed assessing the occurrence of Hopf and period-doubling BWPs and quite rich complex dynamics. In addition, it has been shown that FCAM can be combined with techniques, such as the harmonic balance method citare, to effectively analyze and control such BWPs. Moreover, by suitably exploiting BWPs, it turned out that different chaotic dynamics in a class of Chua's oscillators can be programmed by means of suitable current or voltage pulses [100]. Synchronization aspects in arrays of coupled oscillators have been analyzed as well [101].

5. Conclusions

We here provided an overview of the typical oxide materials used to produce memristive devices and of their switching behavior. With specific reference to anodic oxides, their potential as switching components has been demonstrated, and the possibility to have an easy control over their thickness and composition with excellent repeatability is particularly appealing for the specific application envisioned. Yet, some open issues can be identified in this frame, namely, the downscaling of oxide area, and related problems of technological transfer at the sub-micrometric scale, and the verification of compatibility of such electrochemical wet process with CMOS fabrication.

Acknowledgements

The authors would like to acknowledge the financial support of Fondazione Cariplo and Regione Lombardia, project ProACTIV-MOX—PROmoting research on AnodiC memrisTIVe Metal OXide films for nanoelectronics.

Conflict of interest

The authors declare no conflict of interest.

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Section 3

New Materials Based on Memristor Properties

Chapter 4

Memristive Systems Based on Two-Dimensional Materials

Gennady N. Panin and Olesya O. Kapitanova

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.78973

Abstract

The unique electronic and optical properties of newly discovered 2D crystals such as graphene, graphene oxide, molybdenum disulfide, and so on demonstrate the tremendous potential in creating ultrahigh-density nano- and bioelectronics for innovative image recognition systems, storage and processing of big data. A new type of memristors with a floating photogate based on biocompatible graphene and other 2D crystals with extremely low power consumption and footprint is considered. The photocatalytic oxidation of graphene is proposed as an effective method of creating synapse-like 2D memristive devices with photoresistive switching for nonvolatile electronic memory of ultrahigh density. Particular attention is paid to the new concept of the formation of self-assembled nanoscale memristive elements interfacing artificial electronic neural networks. 2D photomemristors with a floating photogate exhibit multiple states controlled in a wide range of electromagnetic radiation and can be used for neuromorphic computations, pattern recognition and image processing needed to create artificial intelligence.

Keywords: 2D memristor, graphene, graphene oxide, molybdenum disulfide, resistive memory, photoresistive switching, photomemristor, artificial neural networks

1. Introduction

Memristive electronic systems, similar to biological synapses in neural networks, are a new type of electronic logic switches and memory with extremely low energy consumption and footprint. These new electronic components can solve the problem of physical and technological limitations of modern CMOS technology and create an elemental base for artificial intelligence. The unique electronic and optical properties of newly discovered atomic two-dimensional (2D) crystals, such as graphene, graphene oxide, molybdenum disulfide, and so

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on demonstrate a huge potential for designing ultrahigh density nano- and bioelectronics for innovative information systems.

The chapter consists of the Introduction (Paragraph 1) and five sections that describe a brief history of the memristor and nonlinear effects in semiconductor electronics (Paragraph 2), the discovery of 2D crystals and a multilevel ultrafast nonvolatile memory based on graphene oxide (Paragraph 3), a memristor with a floating photogate (Paragraphs 3 and 4), a photonic chip with a photon synapse (Paragraph 5), a 2D TMD memory obtained on large-scale substrates (6) and Conclusion (Paragraph 7). Here we present a modern state of memristive systems, where signaling is analogous to signaling in biological neural networks. The focus is on 2D nonvolatile resistive memory based on molybdenum and graphene/graphene oxide (G/GO), which is biocompatible and allows the use of a neuromorphic architecture for analog computation and self-assembly technology. Photocatalytic and electron-beam oxidation-reduction of graphene/graphene oxide is considered as an effective method of manufacturing 2D memristors with photoresistive switching for nonvolatile memory of ultrahigh capacity. A new type of multifunctional memristor with a photogate, controlled electrically and optically over a wide range of wavelengths, can be used for image processing, pattern recognition and recognition of sounds, movements and speech needed to create artificial intelligence.

2. Memristor and nonlinear effects in solid state electronics

The definition of the memristor as a nonlinear resistive element was introduced by Leon Chua in 1971 to describe the missing fourth base element of the electrical circuit [1]. The memristor, along with other known circuit elements, such as a capacitor, a resistor and an inductor, could describe nonlinear effects in solid state electronics that were already well known. In 1922, Oleg Losev observed a new phenomenon of negative differential resistance in a two-electrode point device—a cristadyne [2, 3]—which was then used to generate and detect a signal for radio broadcasting around the world. Losev's cristadyne allowed to work at frequencies up to 100 MHz, at that time not conceivable and not understandable for applications. Later, Oleg Losev improved his cristadyne, adding to it a third electrode, which could control the current in this device. The article on the new nonlinear three-electrode device, sent by Losev to the "Physical Review" in 1942 from besieged Leningrad was lost and not published. The great interest in this topic was also in other laboratories. In 1948, John Bardeen of Bell Labs received a patent for a point-contact three-electrode element [4] and, together with Walter Brattein, described the physical principles of the transistor effect [5–9]. In 1956, for the discovery of the transistor effect, William Shockley, John Bardeen and Walter Brattein received the Nobel Prize in Physics. In 1957, Leo Esaki demonstrated independently a similar nonlinear device—a tunnel diode—and in 1973 received for the discovery of this effect the Nobel Prize in Physics.

Interest in the nonlinear two-electrode memristive device increased sharply in 2008, when the memristor was detected experimentally in the HP laboratory [10]. This device consisted of two nanoscale regions, doped and undoped, the relative displacement of which controlled

the on and off states. The first matrix of memristors was made on the basis of TiO_2 on a CMOS chip in the HP laboratory in 2012. A memristor with two platinum electrodes was a nonlinear dynamic structure whose resistance depended on the electric field and the current flow (**Figure 1**). This nonlinear device made it possible to form nonvolatile states that allow storing information with the power supply off, had the ability to obtain ultrahigh recording density, low switching energy, high operating speed, long storage time and the possibility of multilevel recording using discrete or continuous states.

The memristor is a memory resistor with variable resistance and is described by the conductivity depending on the flux and field. In 2016, Fujitsu Semiconductor and Panasonic Semiconductor demonstrated the first serial product of 4 Mb RRAM. Using a nonlinear dynamic approach allows you to effectively solve a number of complex computational problems for image processing and pattern recognition. For example, a commercial product Toshiba Smart Photo Sensor with a universal chip based on a cellular neural network (CNN) is capable of processing images, similar to the human brain, which allows to calculate the elementary problems of image recognition within nanoseconds. It was shown that the CNN chip is so fast that it can detect a bullet in flight and have enough time to program another bullet in order to knock it down.

Memristors, which are similar to synapses in biological neural networks, can become an elemental base for creating high-performance intelligent machines and computers with a neuromorphic architecture similar to the brain. It is known that the human brain, containing 10^{10} neurons and 10^{14} synapses (**Figure 2**), processes analog information and consumes only about 20 Watts. A modern supercomputer with digital processing of information to simulate the operation of a neural network of only 1% of the number of neurons of the human brain requires about 10^6 Watts. To simulate the work of the human brain within 1 s, the supercomputer "K Computer" (up to 10 petaflops, 10^{16} billion operations per second, 1 petabyte of RAM)—the development of the Japanese corporation "Fujitsu"—takes about 40 min. Thus, an analog processor based on a neuromorphic memory system is much more efficient than a modern digital supercomputer. The key moment of this system is special processes of signal transmission in neural networks, which are paid great attention to by researchers. In 2000, the Nobel Prize in Physiology was awarded to Arvid Karlsson, Paul Gringard and Erik R. Kandell for "discoveries in the transmission of signals in the nervous system." Neural networks have

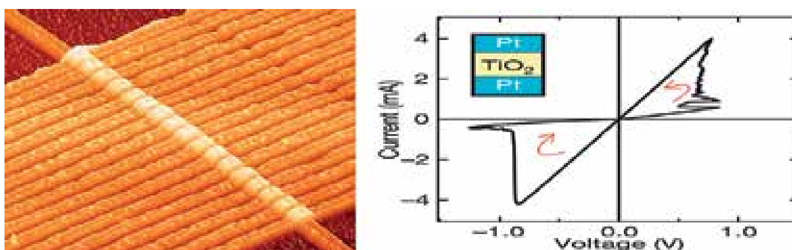

Figure 1. Memristors on CMOS chip (HP 2012) and the I/V-characteristic of $Pt/TiO_2/Pt$ memristor.

Figure 2. Neural network.

associative memory and the ability to learn deeply, the knowledge of which was laid down in the works of the Russian physiologist Ivan Pavlov, who received the Nobel Prize in Physiology in 1904. The study of digestion pushed him to the idea of conditioned reflexes. Such acquired reflexes arise under certain conditions and disappear when conditions are not observed.

3. Atomic 2D graphene crystal

Graphene is a crystalline two-dimensional layer of carbon with the thickness of one atom (**Figure 3**). A huge interest in this material appeared in 2004 after the joint publication of researchers from IMT RAS and Manchester University on the effect of an electric field in atomic-thin carbon films [11]. Six years later in 2010, Andrei Geim and Konstantin Novoselov were awarded the Nobel Prize in Physics for “pioneering experiments with 2D graphene material.”

Graphene consists of two symmetric carbon sublattices that form the Dirac cone of the linear energy dispersion of the electrons, which are called Dirac fermions. The peculiarity of these particles is that they are massless and behave like photons. In consequence, graphene demonstrates magical properties. Graphene transparent (97.7%), resistant to an extremely high current density (one million times higher than that of copper), has the highest electron mobility of known materials (~10^6 cm^2 B^{-1} s^{-1}, three orders of magnitude higher than in silicon) and a very high thermal conductivity ($K > 5 \times 10^3$ W/(m × K)), which is higher than that of a diamond. Graphene is a well stretchable (25%) material with a unique mechanical strength $E > 10^{12}$ Pa (six times higher than steel). In addition, graphene shows very good biocompatibility.

3.1. Memristor based on graphene/graphene oxide

In 2010, researchers from IMT RAS and Dongguk University demonstrated a graphene/graphene oxide (G/GO) memristor that switched at 0.7 V and 1 nA, with an on/off ratio of about 10^3 (**Figure 4**) [12, 13]. The electron beam-induced current method made it possible to reveal, with a high spatial resolution, the formation of randomly distributed current filaments (**Figure 5**) and to study the switching mechanism in this device like a synapse. The resistance of this device varied nonlinearly in the electric field, and the values of high and low resistance were nonvolatile.

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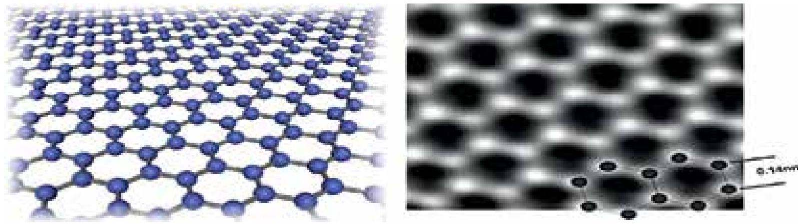

Figure 3. The crystal lattice of graphene.

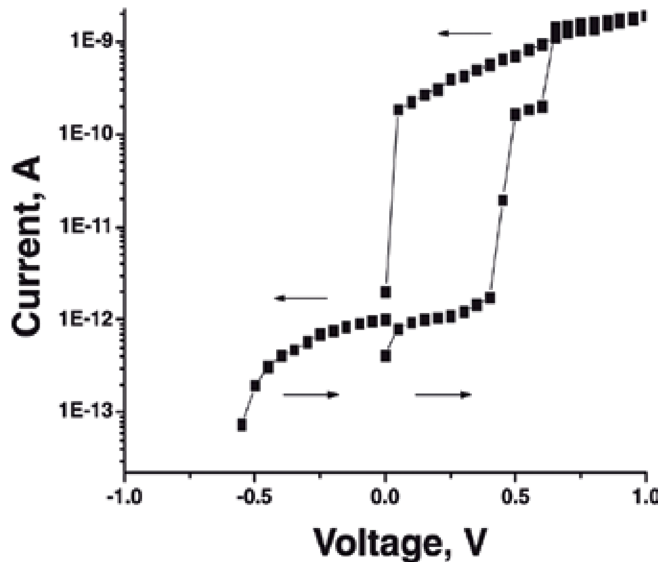

Figure 4. Resistive switching of the Al/GO/Al structure, performed at 5 V [12].

3.2. The mechanism of resistive switching in graphene/graphene oxide

The mechanism of resistive switching in G/GO was studied in detail in a number of works [12–17] in which it was shown that the migration of oxygen-containing groups in GO plays an important role. One sp^3 carbon-oxygen or carbon-hydroxyl bond on 10^6 sp^2 bonds reduced conductivity in carbon nanomaterials by 50% [18]. Graphene oxide with a sp^3 carbon configuration possessing low electrical conductivity was switched in an electric field locally in the sp^2 configuration of carbon (**Figure 6**), which led to high electrical conductivity. This process can be controlled both by adsorption/desorption of oxygen and by migration of oxygen-related groups.

3.3. Self-organization of memristors based on graphene/graphene oxide

The photocatalytic oxidation of graphene coated with a layer of 10–15 nm ZnO nanoparticles under ultraviolet (UV) irradiation conditions led to the formation of self-organized G/GO memristors with very high density (10^{12} cm^{-2}) [16, 17]. **Figure 7** shows the scheme of photocatalytic oxidation of graphene with ZnO nanoparticles. A 2–3-layer graphene coated with

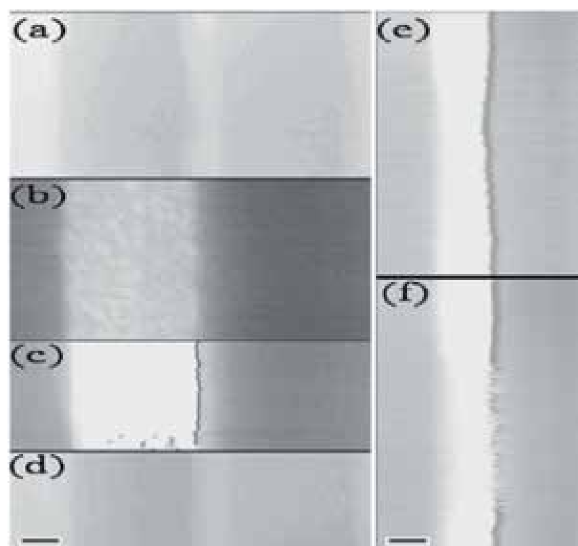

Figure 5. Scanning electron microscope (SEM)-remote induced current (REBIC) images of the Al/GO/Al structure with the modulation of the built-in potential barrier near the negatively biased Al electrode at different bias (V_b) and forming (V_f) voltages. (a) $V_b = 0$; $V_f = 0$ (SE mode); (b) $V_b = 0$; $V_f = 0$ (REBIC mode); (c) $V_b = 0$; $V_f = 5$ V (REBIC mode); (d) $V_b = 0$; $V_f = 5$ V (SE mode); (e) $V_b = 0.2$ V; $V_f = 7$ V (REBIC mode); (f) $V_b = 0.5$ V; $V_f = 7$ V (REBIC mode, same area as in (e)). A scale mark of 100 μm (e) and (f), 50 μm in (a)–(d). The images in (a)–(d) were obtained by sequentially switching signals of secondary electrons (SE) and remote induced current (REBIC) during scanning of the electron beam [12].

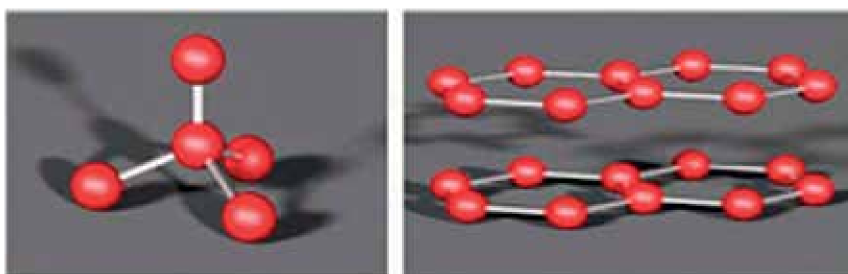

Figure 6. sp^3 (left) and sp^2 (right) of the carbon configuration.

particles was irradiated in a moist air stream at room temperature or above (80°C) using a quartz UV lamp with a light flux of 0.03 J $min^{-1} \times cm^2$. Light with a wavelength exceeding 365 nm was filtered. The time of ultraviolet irradiation ranged from 5 to 90 min. After ultraviolet treatment, the ZnO nanoparticles were dissolved in dilute 0.1 M HCl, the graphene substrate was washed with deionized water and dried in nitrogen.

ZnO nanoparticles play a key role in the process of photooxidation of graphene. **Figure 8** shows the electronic diagram of graphene/ZnO interface under UV irradiation. The bending of the bands upward in the ZnO nanoparticles is caused by a lower electron work function in ZnO (3.6 eV) compared to graphene (4.5 eV). Electron–hole pairs generated in ZnO (3.3 eV) under UV irradiation (reaction 1) are separated in a built-in electric field at the graphene/ZnO

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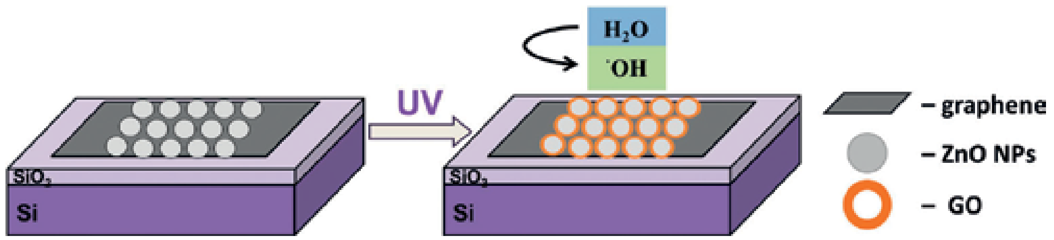

Figure 7. Scheme of photocatalytic oxidation of graphene coated with ZnO nanoparticles under UV light to form G/GO heterostructures on a Si/SiO_2 substrate [17].

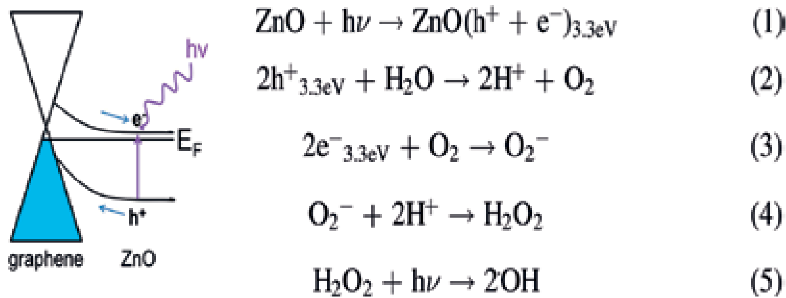

Figure 8. Schematic electronic diagram of the G/ZnO interface under UV irradiation. Electron-hole pairs generated in ZnO (3.3 eV) under UV irradiation (reaction 1) are separated in a built-in electric field at the G/ZnO interface, providing a flux of holes to graphene [16].

interface, which provides a hole flux (3.3 eV) to graphene. As a result, graphene is decorated with highly reactive hydroxyl radicals (· OH) through O_2^- and H_2O_2 (reactions 3–5) processes of photodecomposition of water molecules from moist air.

3.4. Memristors based on graphene with a floating gate of ultrahigh density

Controlling the distribution of ZnO nanoparticles on graphene with a well reproducible size (10–15 nm) makes it possible to create highly scalable nanoheterojunctions of G/GO for ultra-high-density memory (up to 10^{12} cm^{-2} or 1 Tb on a chip for the vertical geometry of crossing electrodes, **Figure 9**).

Memristors with a floating photogate are electrically read with or without optical excitation. The I-V curve of the graphene sample before oxidation demonstrates linear behavior and high conductivity of graphene (**Figure 10(a)**, black curve). The photocatalytic process leads to a decrease in current through the sample by two orders of magnitude and a nonlinear behavior indicating the formation of a bandgap in the oxidized graphene (**Figure 10(a)**, red curve).

The rise in the temperature of moist air reduces the oxidation time of graphene. The G/GO heterostructures obtained by photocatalytic oxidation by blowing moist air at room temperature for 30 min and at 80°C for 5 min demonstrate a nonlinear behavior with a GO band width of about 3 eV, which reduces the conductivity of oxidized graphene by two orders of magnitude compared to graphene. The formed G/GO nanostructures demonstrated good

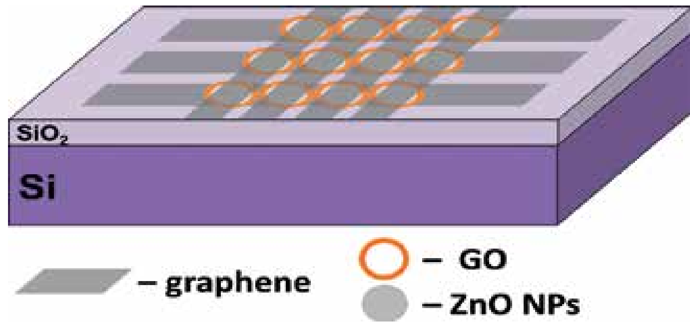

Figure 9. Scheme of arrays of G/GO photomemristors in vertical geometry obtained by photocatalytic oxidation of graphene with ZnO nanoparticles [17].

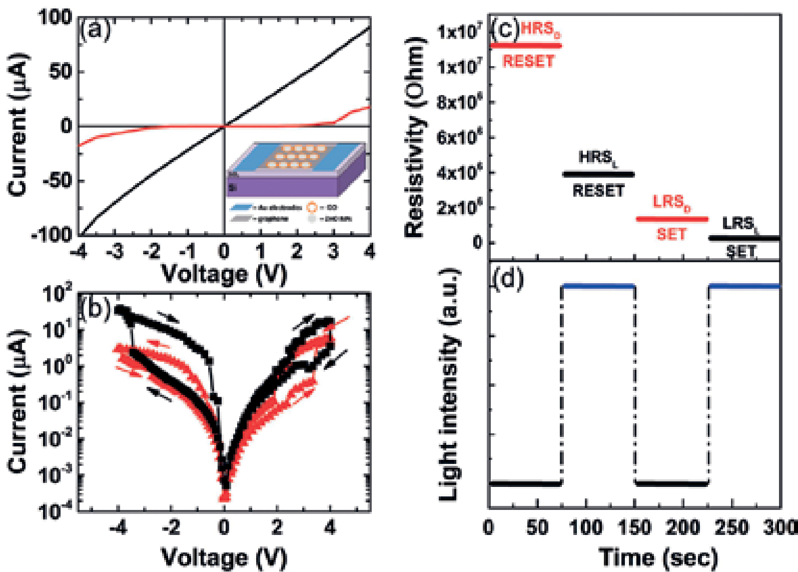

Figure 10. (a) I-V characteristics of the 2–3 layer G/ZnO structure before (black) and after (red) photocatalytic oxidation in moist air for 30 min at room temperature. Insert-scheme for measuring the structure with lateral gold electrodes. (b) I-V characteristics for the G/GO nanostructure preliminarily polarized (+5 V, 15 min) with white light (black) and in the dark (red). (c) Resistive states of the G/GO photomemristor, which are switched by a voltage of −3.8/3.3 V (Reset/Set) in the dark and −3.5/4 V (Set/Reset) under white light pulses (d) and read at 2.5 V [17].

photosensitivity to white light and photoresistive switching. The photocurrent increased approximately six times at a bias voltage greater than 3 V. This indicates that the electron–hole pairs generated by light are effectively separated in the biased G/GO heterojunctions. **Figure 10(b)** shows the I-V characteristics of the preformed G/GO nanostructure (+5 V, 15 min) when sweep voltage of −4 to 4 V under white light (black) and in the dark (red). Well reproducible bipolar hysteresis indicates a resistive switching of the structure with an on/off ratio of about 10 for 4 different resistive states HRSD, LRSD, LRSL and HRSL in the dark and light with switching voltages of −3.8/3.3 V (Reset/Set) and −3.5/4 V (Set/Reset), respectively (**Figure 10(c)** and **(d)**). To form vertical memristive structures, ZnO nanorods (NR) grown on graphene can also be used instead of ZnO nanoparticles (**Figure 11**) [16].

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The vertical structure of the G/GO/ZnO nanorods (NR) allows selective excitation with UV light of 380 nm. Resistive switching in heterostructures of G/GO/ZnO NR was observed at voltages <1 V with the ratio of high/low resistance of 10^3 after the forming process at 1 V (**Figure 12(b)**).

The structure of resistive memory based on graphene and ZnO NR is promising for memristive devices with high density and low power consumption.

3.5. Graphene/graphene oxide memristors formed by an electron beam

Electron beam annealing GO stimulates a radical mechanism for the reduction of GO due to the formation of hot electrons. These electrons destroy the weak C-O and C-H bonds (in comparison with strong C-C bonds) and form highly reactive radicals $O^{\cdot}$ and $H^{\cdot}$, which

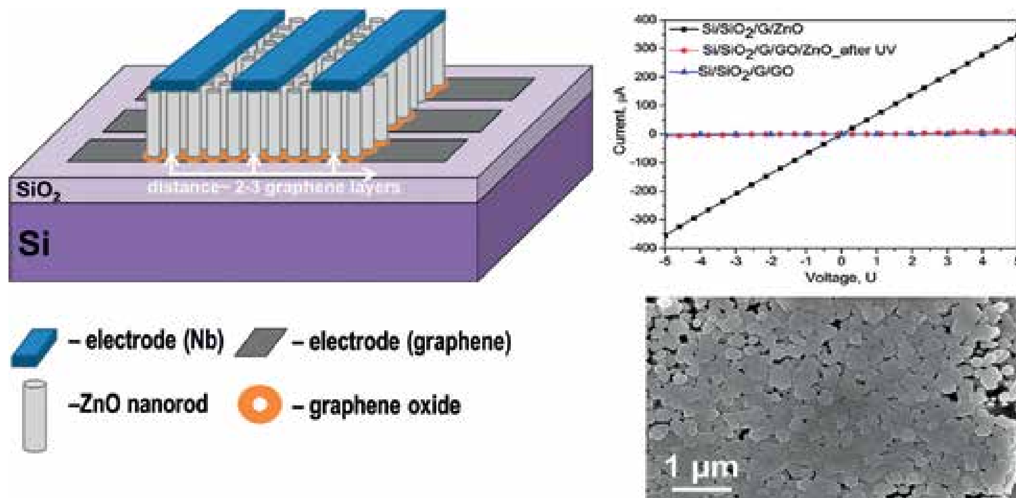

Figure 11. Scheme of arrays of G/GO/ZnO NR photomemristors in vertical geometry (left) and a SEM image of the structure (lower right) with their current-voltage characteristics (upper right) [16].

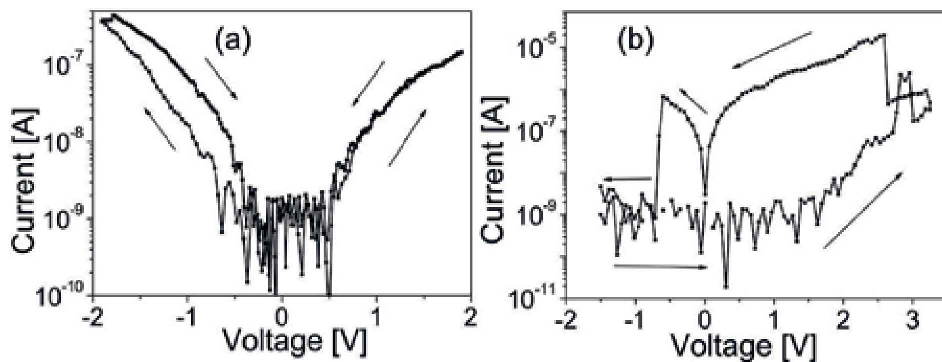

Figure 12. I-V characteristics of the vertical structure G/GO/ZnO in a semilogarithmic scale (a) without forming and (b) after the forming process [16].

recombine in H_2O, H_2, O_2, and the uncompensated charge in GO is used to restore the sp^2 carbon bond. It should be noted that the electron beam annealing process excites the electronic subsystem selectively, and the energy of the generated hot electrons can be resonantly absorbed by the functional groups of graphene oxide. To remove oxygen groups, several eV are required, which is comparable to the energy between orbitals. Primary beam electrons are high-energy and can participate in annealing only through the process of energy absorption by graphene oxide to form hot electrons with an energy close to the GO bandgap (E_g). Electron-stimulated annealing of GO can occur due to the generation of a high concentration of charge carriers in this material (E_g = 1–6 eV) (an electron beam with an electron energy of 3–10 keV creates 10^3 electron-hole pairs per incident electron). The process of electron-stimulated annealing by an electron beam is more effective than laser annealing, in which one photon produces only one electron-hole pair, and therefore the thermal effects in laser annealing make the main contribution. Electron beam annealing allows the direct formation of rGO/GO memristive nanostructures with controlled reduction without the use of a mask. **Figure 13** shows a SEM image of a GO film with a superimposed stripe pattern (green) for electron-beam exposure (a) and a rGO/GO/rGO structure obtained by direct "writing" by an electron beam with a dose of 150 mA × s/cm^2 (b, c). The change in image contrast in the secondary electron emission (SEE) of graphene oxide after electron beam processing (b, c) indicates a change in composition and its electronic properties.

The electron beam annealing of GO allows for more efficient formation of a resistive switching structure. The lateral structure of rGO/GO/rGO obtained by electron beam irradiation with a dose of 200 mA × s/cm^2 exhibited soft resistive switching without the forming process. The curve of the I-V structure, after irradiation, was nonlinear with a small hysteresis

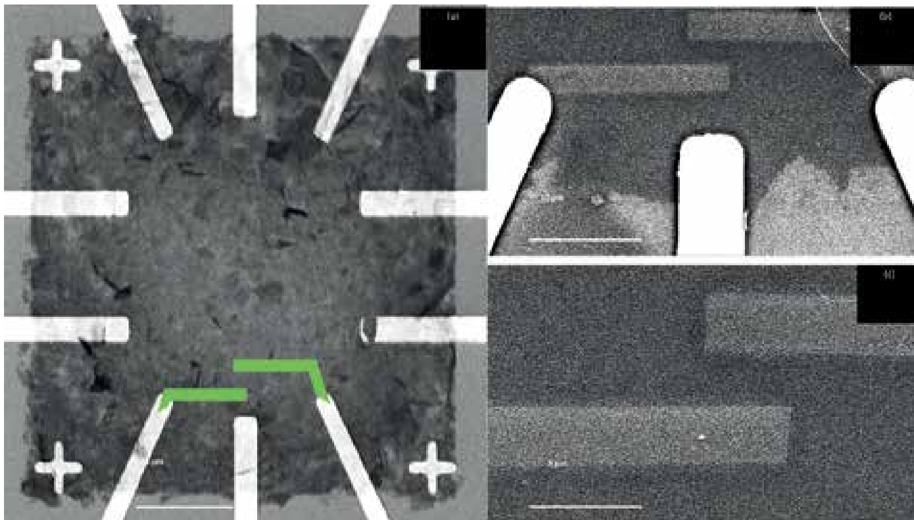

Figure 13. SEM images of a GO film on a SiO_2/Si substrate with Pt electrodes (white) and superimposed stripe pattern (green) for electron beam writing (a) and rGO/GO/rGO structure after irradiation with an electron beam (b, c). The narrow bands of the brighter SEE contrast are regions of the reduced rGO after irradiation.

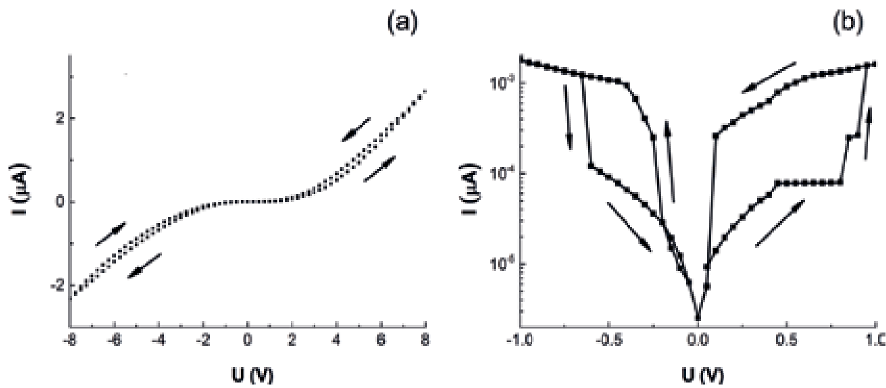

Figure 14. I-V characteristics of the Pt/GO/Pt structure after electron irradiation before (a) and after (b) the forming process.

(**Figure 14(a)**). The forming process at 20 V led to an increase in the conductivity of the structure by several orders of magnitude and to a pronounced nonlinearity. A bipolar hysteresis was observed that indicated a resistive switching of the structure from the high-resistive resistive state (HRS) ($(1.2 \pm 0.1) \times 10^{11}$ Ω) to the low-resistive resistive state (LRS) ($(6.7 \pm 0.4) \times 10^8$ Ohm) (~2 orders of magnitude) at a low switching voltage of 0.8–0.9 V (**Figure 14(b)**). The electron beam annealed structures showed good reproducibility with a small spread of switching voltages (0.05–0.1 V).

3.6. Multilevel ultrafast nonvolatile memory based on graphene oxide

Memory with the ability to store more than one bit per cell, that is, having multilevel memory states, is very attractive, since it offers a simple and economical way to increased memory capacity (e.g., modern CMOS NAND-Flash usually stores 2 or 3 bits per cell). Combining this capability with tiered storage with extremely high scalability is especially effective for implementing memory with ultrahigh storage volumes. Access to four very well-separated and stable memory states in nanoscale GO cells by monitoring the duration and amplitude of the write pulse was recently demonstrated at IBM [19]. Excitation pulses with amplitudes from 2 to 6 V and duration from 20 to 80 ns were used to determine the conditions for successful recording and erasing of multilevel memory states in Pt/GO/Ti/Pt and monitoring of the resulting cell resistance, see **Figure 15(a)** and **(b)**.

The cells were completely switched from the RESET state, which can be considered as state 00 to memory states 01, 10 and 11 using pulses of −2.5 V/60 ns, −3.5 V/60 ns and − 4.5 V/60 ns respectively (**Figure 15(a)**). Erasing of cells from 01, 10 and 11 states back to state 00 was successfully achieved for pulses +3 V/60 ns, +4 V/60 ns and +5 V/60 ns, respectively (**Figure 15(b)**). Separation of intermediate resistance levels is very good (see **Figure 15(a)**), which allows a reliable reading process. Intermediate levels showed excellent reliability (**Figure 15(c)**) and were stable over time (**Figure 15(d)**), both on rigid and flexible substrates. The reversible resistive switching observed in these devices was due to the migration of oxygen, which led to a change in the conductivity.

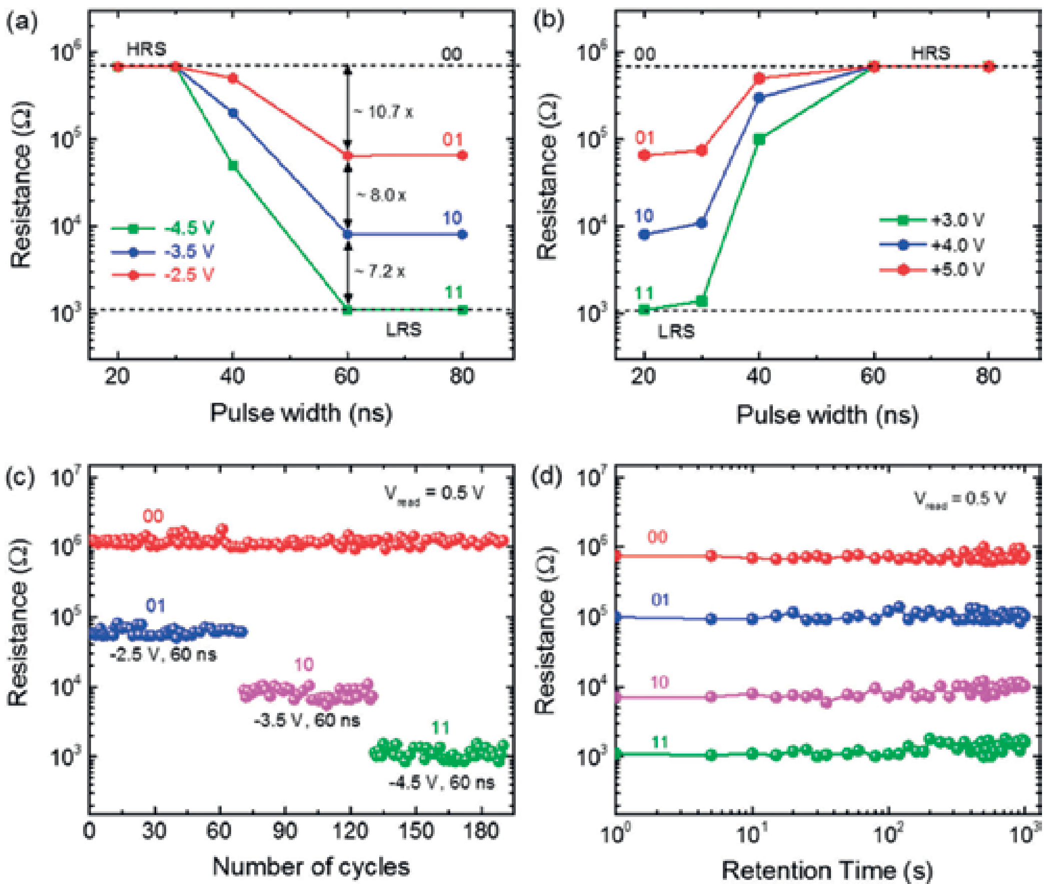

Figure 15. (a) Record and (b) erase multilevel states in a 75 nm GO memory cell (8 nm-thick GO layer) by controlling the amplitude and pulse width. (c) reliability and (d) storage of states of a multilevel, nanoscale graphene oxide cell [19].

4. Memristor with floating MoS_2 photogate

A memristor with a floating MoS_2 photogate polarized in an electric field under different lighting conditions demonstrates a multilevel switching [20]. **Figure 16** shows the current–voltage curves (I-V) of the Au/MoS_2/Au structure (an inset in **Figure 16(a)**) after polarization at 3 and 6 V. The nonlinear characteristics of a device with hysteresis indicate a memristive behavior. Furthermore, the memristor demonstrates a high photoresponse when illuminated with white light. When the device is polarized at 3 V, a smooth switching from HRSL3 to LRSL3 is observed under light illumination and from HRSD3 to LRSD3 in the dark with a ratio of on/off currents of about 2 and 4 at 1.2 V and 0.7 V, respectively (**Figure 16(a)**). At a higher voltage (6 V), the device shows a sharp switching when excited by white light, from HRSL6 to LRSL6 at −2.9 V with an on/off ratio of about 10 and a smooth switching from HRSD6 to LRSD6 in the dark with an on/off ratio of about 3 at 0.7 V (the SET process of

writing the ON state, **Figure 16(b)**). When the applied voltage changes from 0 to positive voltage (4.2 V), the device returns to HRSL6 (RESET operation to clear the state ON to OFF). The memristive behavior of the device in darkness and in light is well reproduced up to 1000 cycles (**Figure 16(c)** and **(d)**) and demonstrates the possibility of obtaining in the device a multilevel resistive switching and its control by means of an electric field in the dark and when excited by light.

It should be noted that resistive switching controlled by the polarization of MoS_2 nanospheres is a faster process than ion transport, and the frequency of optical access is much higher than electrical addressing.

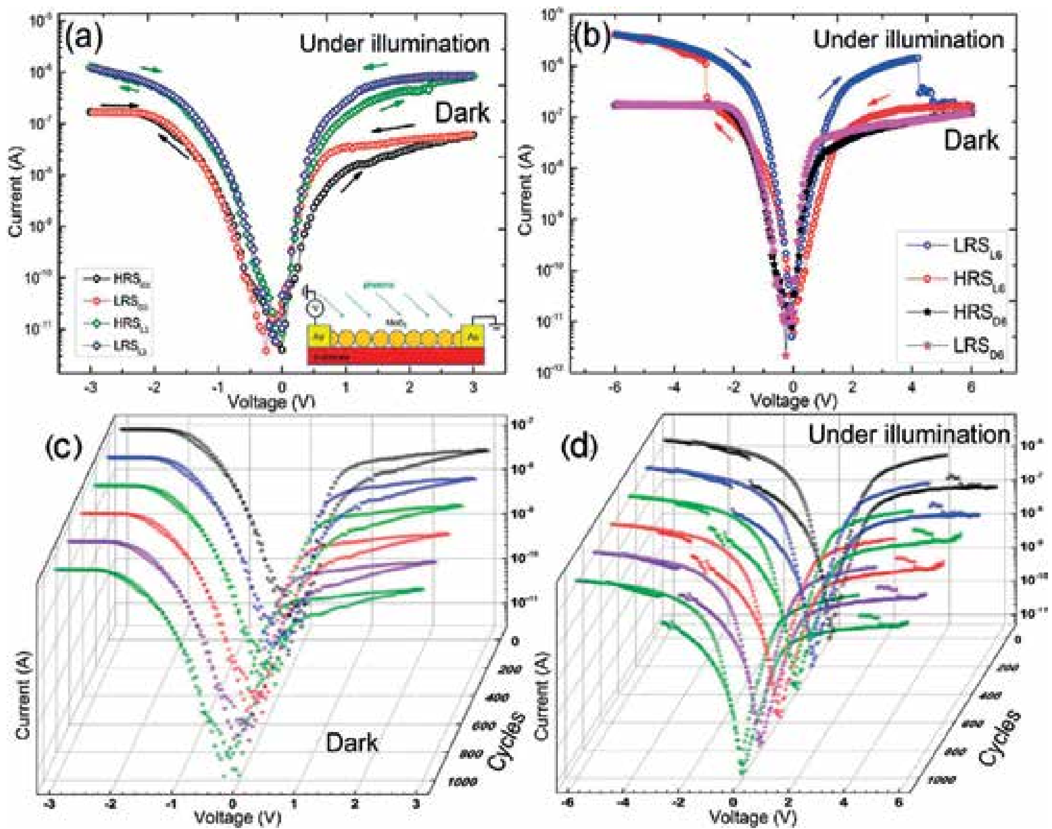

Figure 16. Resistive switching of the nanospheric photomemristor Au/MoS_2/Au. I-V characteristics in the dark or under white light (spectral maxima at 2.7 eV and 1.8 eV; device diagram on the inset in **Figure 16(a)** with light excitation). The arrows on the curves indicate the direction of the voltage sweep; (a) I-V curves after 3 V voltage polarization. The device smoothly switches from HRSL3 to LRSL3 under light and from HRSD3 to LRSD3 in the dark with an on/off ratio of about 2 and 4 at 1.2 V and 0.7 V, respectively; (b) I-V curves after a 6 V voltage polarization. The device shows abrupt changeover of resistance when excited by light, from HRSL6 to LRSL6 at −9.2 V with an on/off ratio of about 10 and a smooth transition from HRSD6 to LRSD6 without light excitation with a switching factor on/off about 3 at 0.7 V. (c) Memristive characteristics of the device without excitation by light after several cycles. (d) Memristive characteristics of the device when excited by white light after several cycles [20].

4.1. 8-Level memristor system with an MoS_2 floating photogate

The diagram of the operation of the 8-level memristor system with the MoS_2 floating photodetector is shown in **Figure 17**, where the resistance states formed after the SET/RESET operation of the MoS_2 memristor polarized at voltages of 3 V and 6 V in the dark or when excited by light are shown. A memristor polarized at 3 V in darkness or in white light demonstrates four states that are read at a voltage of 0.7 V (HRSD3 and LRSD3) and 1.2 V (HRSL3 and LRSL3) in the dark or in white light (**Figure 17(a)**).

Polarization of the memristor at 6 V in darkness or under light leads to the formation of four more states that are read at a voltage of 0.7 V (HRSD6 and LRSD6) and 4 V (HRSL6 and

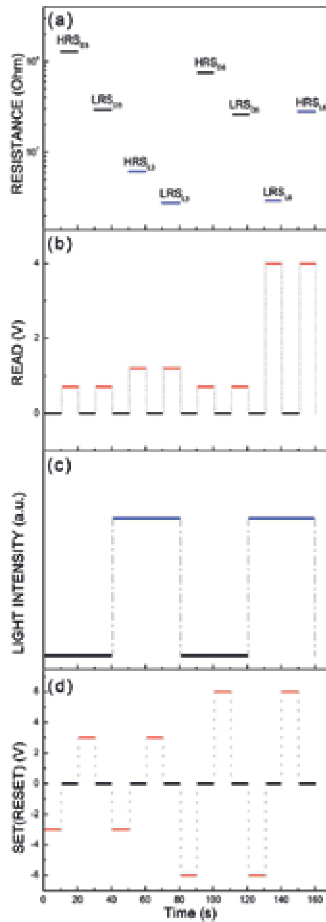

Figure 17. The operation of the MoS_2 photomemristor, polarized at different voltages in the dark or when excited by light. (1) high and low resistive states obtained using SET/RESET operations at −3 V/3 V and −6 V/+6 V in the dark (HRSD3, LRSD3 and HRSD6, LRSD6) and under white light (HRSL3, LRSL3, LRSL6 and HRSL6). (2) reading diagram under impulse voltage. Resistive states are read at 0.7 V (HRSD3, LRSD3, HRSD6 and LRSD6), 1.2 V (HRSL3 and LRSL3) and 4 V (LRSL6 and HRSL6) in dark (D) or white light (L). (3) excitation scheme by pulses of white light. SET/RESET and the READ operation is controlled by switching off the light pulses (black) (HRSD3, LRSD3, HRSD6 and LRSD6) and turned on (blue) (HRSL3, LRSL3, HRSL6 and LRSL6). A 3 V polarized memristor demonstrates four states that are read as HRSD3, LRSD3, HRSL3 and LRSL3, while a memristor polarized at 6 V demonstrates the other four states: HRSD6, LRSD6, HRSL6 and LRSL6, which can be read in the dark or in the light [20].

LRSL6) in darkness or in light (**Figure 17(a)**). These states are controlled electrically and optically, which is confirmed by the iterative operation of the memristor under various conditions of writing and reading (**Figure 17(c)** and **(d)**) Polarization of nanospheres in a photomemristor using an electric field and light pulses creates multilevel states. An analysis of the conductivity in these states of resistance shows that the polarization of nanospheres when excited by light leads to the formation of conductive paths. Reducing the gap between the electrodes can greatly minimize the operating voltage of the device. Modulation of the barrier height at the boundaries of the nanospheres in an external electric field by light due to repolarization is a highly efficient process for high-speed signal processing. The memristor polarized at 3 V and 6 V has different states that can be electrically read at optical excitation in the form of four high-resistance states and four low-resistance states. The optical and electrical polarization of the memristor provides several nonlinear dynamic processes that allow us to build a system with a neuromorphic architecture, similar to a neural network.

5. Photonic chip with photon synapse

A photonic chip containing 70 photon synapses was demonstrated in 2017 by a team from the universities of Oxford, Münster and Exeter [21]. The recording, erasure and reading of information in this case are carried out completely by optical methods (**Figure 18**). The photon synapse consists of a cone-shaped waveguide (dark blue) with discrete islands of phase-change

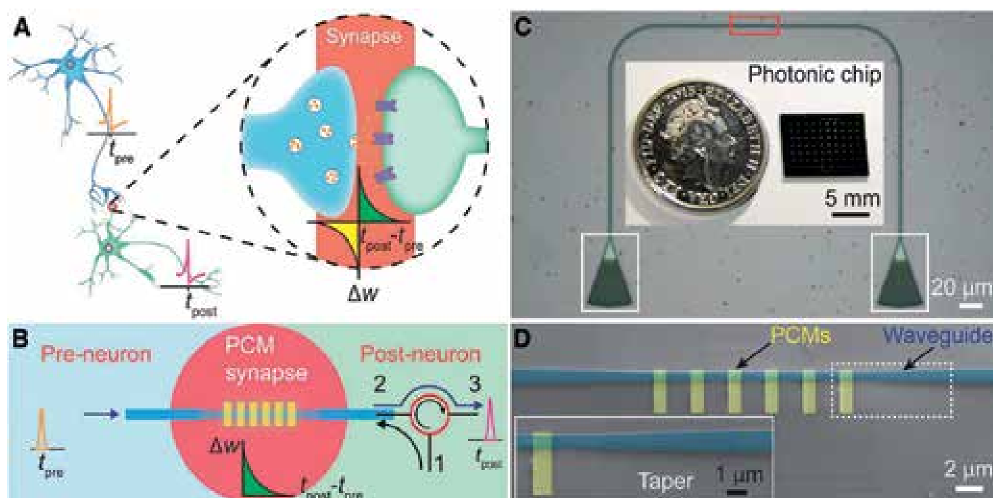

Figure 18. Photon synapse on a crystal. (A) The structure of the neuron and the synapse. Insert: Illustration of the synapse junction. (B) Scheme of the integrated photon synapse resembling the function of a neural synapse. The synapse is based on a cone-shaped waveguide (dark blue) with discrete PCM islands from the top, optically connecting presynaptic (preneural) and postsynaptic (postneural) signals. The red open circle is a circulator with port 2 and port 3, connecting the synapse and postneuron; weighing pulses are fed through port 1 to the synapse. (C) An optical microscope image of a device with an active region (red rectangle) as a photon synapse. The optical input and output of the device is carried out through apodized diffraction couplers (white rectangles). Box: A typical photonic chip containing 70 photon synapses is smaller than a coin. (D) Scanning electron microscope image of the photon synapse active region corresponding to the red rectangle in (C) with six $Ge_2Sb_2Te_5$ (GST) strips (1 × 3 μm, yellow) at the tip of the waveguide (blue). Insert: An increased conical waveguide structure, marked with a white dotted frame [21].

material (PCM) from the top optically connecting the presynaptic (preneuronal) and postsynaptic (postneuronal) signals. The use of purely optical means provides ultrafast operation speed, virtually unlimited bandwidth and no loss of electrical power on interconnects. It is significant that the synaptic weight can be randomly installed simply by changing the number of optical pulses that create a system with continuously changing synaptic plasticity, reflecting the true analog nature of the biological synapses.

5.1. Synaptic weight and plasticity

Synaptic adjustment of the device when switching between crystalline and amorphous states of GST islands with a recorded change in the relative transmission coefficient is shown in **Figure 19**. Five weight states of the photon synapse are obtained by switching the energy of the optical pulse (404.5 pJ, 50 ns). The photon synapse demonstrates good reproducibility of weight numbers with cyclic measurements (**Figure 19(B)**). In this case, the photon synaptic weight is determined by the number of optical pulses (**Figure 19(C)**).

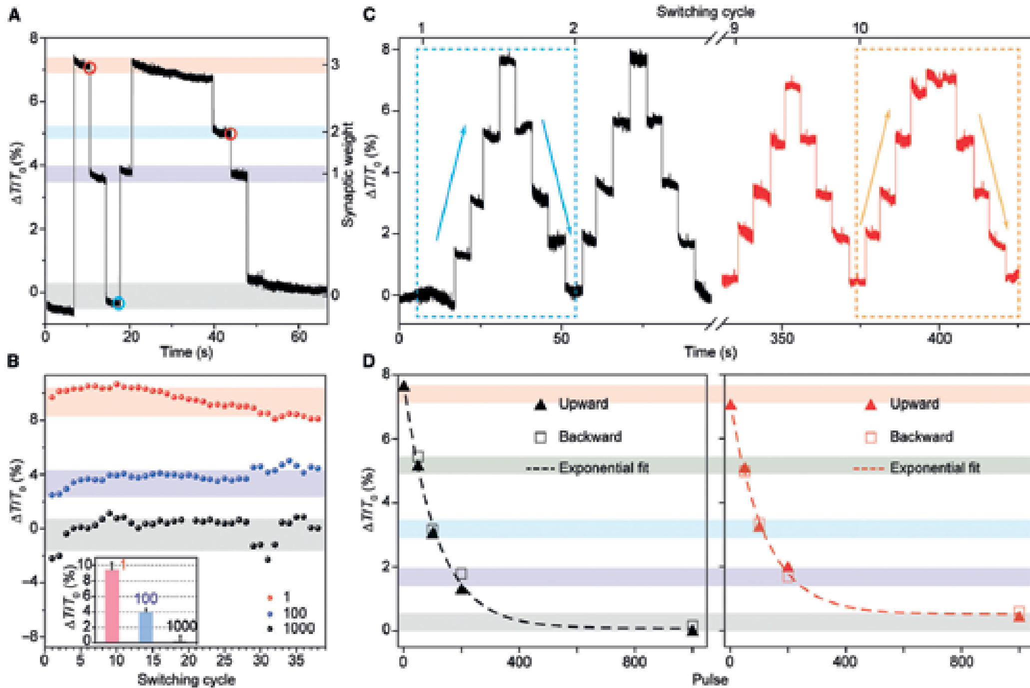

Figure 19. Synaptic weight and plasticity. (A) Demonstration of the differential synaptic weight of the device in **Figure 18** when switching between crystalline and amorphous GST island states with recorded relative coefficient change ($\Delta T/T_0$). Each weight can be achieved with the same number of pulses (50 ns at 243 pJ, 1 MHz) from any previous weight. (B) Weight repeatability for several cycles. Box: Statistical analysis of the change in readings for the weight "0," "1" and "4". The applied pulse was 50 ps at 320 pJ, slightly larger than in (A). (C) Five weights of the photon synapse are obtained when the energy of the optical pulse is switched (404.5 pJ, 50 ns). Dotted blue (yellow) rectangles correspond to the first (last) weight cycle. The up and down arrows in the rectangles are the weighing directions. (D) Photon synaptic weight ($\Delta T/T_0$) as a function of the number of optical pulses. The left (right) panel corresponds to the data of the marked blue (yellow) field in (C). Painted triangles (not filled squares) represent data from the upward (downward) direction of weighing. The dashed lines represent the exponential curves closest to the experimental data [21].

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6. 2D Transition metal dichalcogenides (MoS_2, $MoSe_2$, WS_2 and WSe_2) memory

MOCVD growth of semiconductor monolayer MoS_2 films and tungsten disulfide (WS_2) on silicon oxide at 500°C on a 4-inch wafer allows to obtain excellent electrical characteristics and structure for 2D memristors (**Figure 20**).

6.1. Atomistor: nonvolatile atomic resistive TMD memory

In 2017, the Argonne National Laboratory demonstrated an atomistor: a nonvolatile atomic resistive 2D TMD (MoS_2, $MoSe_2$, WS_2 and WSe_2) memory (**Figure 21**), which scales to a sub-nanometer [23]. New device concepts in nonvolatile flexible memory and brain-like (neuromorphic) computing can significantly benefit from the tremendous possibilities for designing

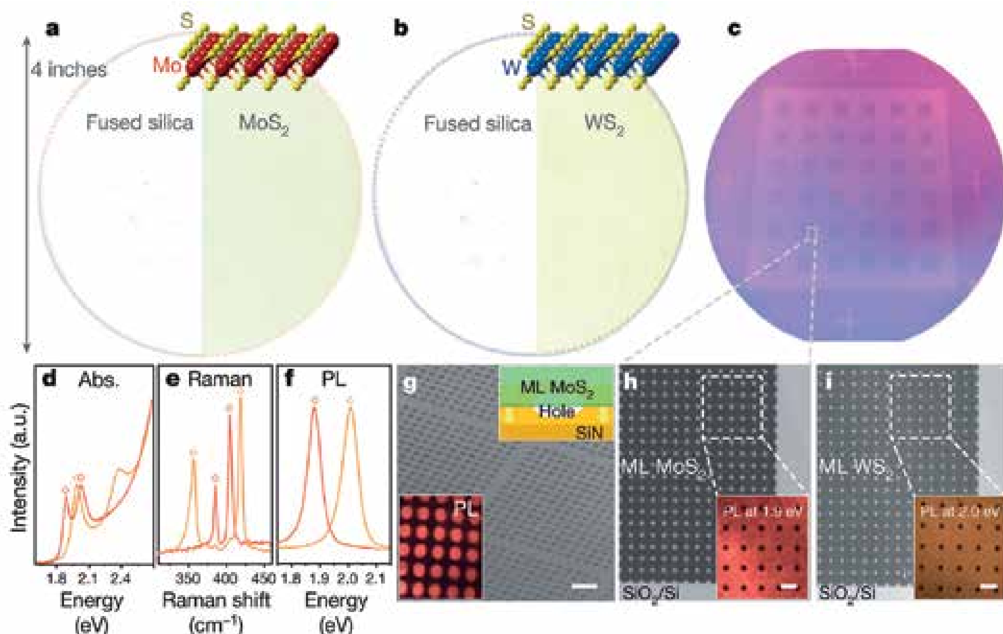

Figure 20. Single-layer transition metal dichalcogenides (TMD) films on 4-inch wafers. a, b, photos of MoS_2 (a) and WS_2 (b) monolayers of films grown on 4-inch substrates with diagrams of their respective atomic structures. The left halves show a quartz substrate for comparison. (c) Photo of a patterned monolayer MoS_2 film on a 4-inch SiO_2/Si wafer (the darker areas are covered with MoS_2). (d) Optical absorption spectra of the MOCVD-grown monolayer MoS_2 (red line) and WS_2 (orange line) in the photon energy range from 1.6 to 2.7 eV. (e) The Raman spectra of the grown monolayer MoS_2 and WS_2 normalized to the intensity of the silicon peak. (f) Normalized photoluminescence spectra of monolayers MoS_2 and WS_2 grown. The peak positions in d–f are consistent with the positions of the peaks obtained from the peeled samples (diamonds). (g) SEM image and photoluminescence (PL) (bottom insert, at 1.9 eV) of monolayer (ML) MoS_2 membranes suspended on a SiN TEM mesh with holes of 2 μm (the suspended film scheme is shown in the upper inset). Label, 10 microns. (h), (i) Optical images (normalized to the area of a clean substrate) of the patterned monolayer MoS_2 (h) and WS_2 (i) on SiO_2 taken from films with a wafer-scale pattern. The insets show photoluminescent images for energies of 1.9 eV (h) and 2.0 eV (i). Scale mark, 10 microns [22].

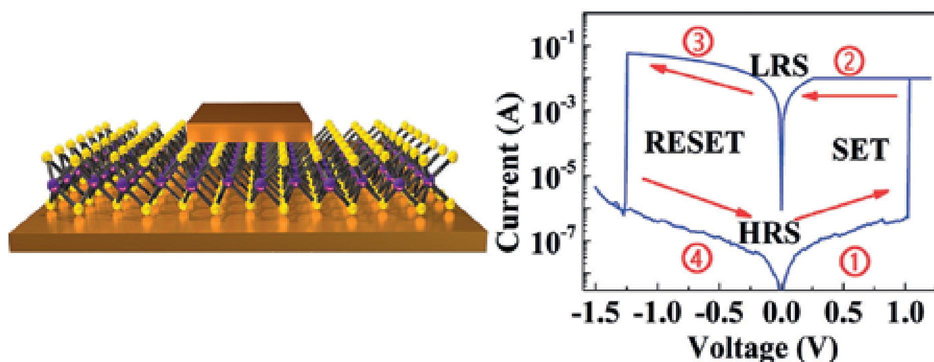

Figure 21. Scheme of a TMD sandwich based on MoS_2 grown on Au foil (left) and a representative curve of I-V behavior of bipolar resistive switching in a MoS_2 monolayer with a lateral area of 2 × 2 μm^2 (on the right). Step 1: The voltage increases from 0 to 1.2 V. At ~ 1 V, the current rises sharply to the limiting current, indicating the transition (SET) from the high resistance state (HRS) to the low resistance state (LRS). Step 2: The voltage decreases from 1.2 to 0 V. The device remains in the LRS. Step 3: The voltage increases from 0 to 1.5 V. At −1.25 V, the current drastically decreases, indicating a transition (RESET) from LRS to HRS. Step 4: The voltage decreases from −1.5 to 0 V. The device remains in HRS mode until the next cycle [23].

2D materials. A new large application, a static radio frequency (RF) switching, was demonstrated using a MoS_2 monolayer operating at 50 GHz.

Multilayer atomic materials [24] can be used to construct the elemental base of neuromorphic computers. One of the new directions is the creation of solid-state memory of the next generation with phase changes and TMO devices. The devices from 2D crystals have certain advantages in obtaining vertical scaling up to the atomic layer. When replacing metal electrodes with graphene, the entire memory cell can be scaled below 2 nm. In addition, the transparency of graphene and the unique spectroscopic features of 2D materials make it possible to obtain a direct optical characteristic of the device on the production line. At present, manual testing of the device's durability (**Figure 22(a)** and (**b**)) is not enough to meet the requirements for solid-state memory and is a reflection of the emerging state of 2D atomistors in comparison with TMO memories [25]. Through engineering or doping, the durability of the device can be improved, similar to what was observed for amorphous carbon storage devices [26]. Retention of nonvolatile states tested up to a week (**Figure 22(c)**) is already sufficient for certain neuromorphic applications with short-term and medium-term plasticity [27]. The subnanometric thickness of monolayers is promising for the realization of ultrahigh densities. With a free step of 10 nm, the atomic density of 10^{15}/mm^3 would provide sufficient space to simulate the density of human synapses (~10^9/mm^3) [28]. For a single-bit single-level storage device, this corresponds to a theoretical surface density of 6.4 Tbit/inch^2.

6.2. High-frequency 2D MoS_2 memristors

Modern switches are implemented using transistor or microelectromechanical devices, both of which are volatile, and the latter also requires a large switching voltage that is not suitable for mobile technologies. Recently, phase change switches have attracted interest [29], but the

requirements for high-temperature phase melting and long switching times have limited their use. 2D memristors offer unprecedented advancement for high-frequency systems due to their low voltage operation, small form-factor, high switching speed and low temperature integration compatible with Si or flexible substrates. Nonvolatile RF switches show promising results with acceptable insertion loss of ~ 1 dB and isolation of >12 dB up to 50 GHz (**Figure 22(d)**). The extracted resistance when the state is On, $R_{ON} \approx 11$ ohms and capacitance when the state is Off, $C_{OFF} \approx 7.7$ fF. This results in a cut-off frequency, which is used to estimate the RF switches (a figure of merit (FOM)) [29, 30] $f_{co} = 1/(2\pi R_{ON} C_{OFF}) \approx 1.8$ THz. Further improvements, especially in terms of scaling, are expected to lead to a significant increase in FOM. A unique combination of independent LRS resistance and area-dependent HRS capacity gives a FOM that can be scaled to 100 s of THz by reducing the area of the device that determines advantages over phase-change switches [29, 30], where the capacitance is proportional to the width, but R_{ON} is inversely dependent, hence, prevents frequency scaling without significant compromise losses. In addition, the high stress of mechanical rupture and the easy integration of 2D materials onto soft substrates enable the production of flexible nonvolatile digital and analog/RF switches capable of withstanding mechanical cycling (**Figure 22(e)**).

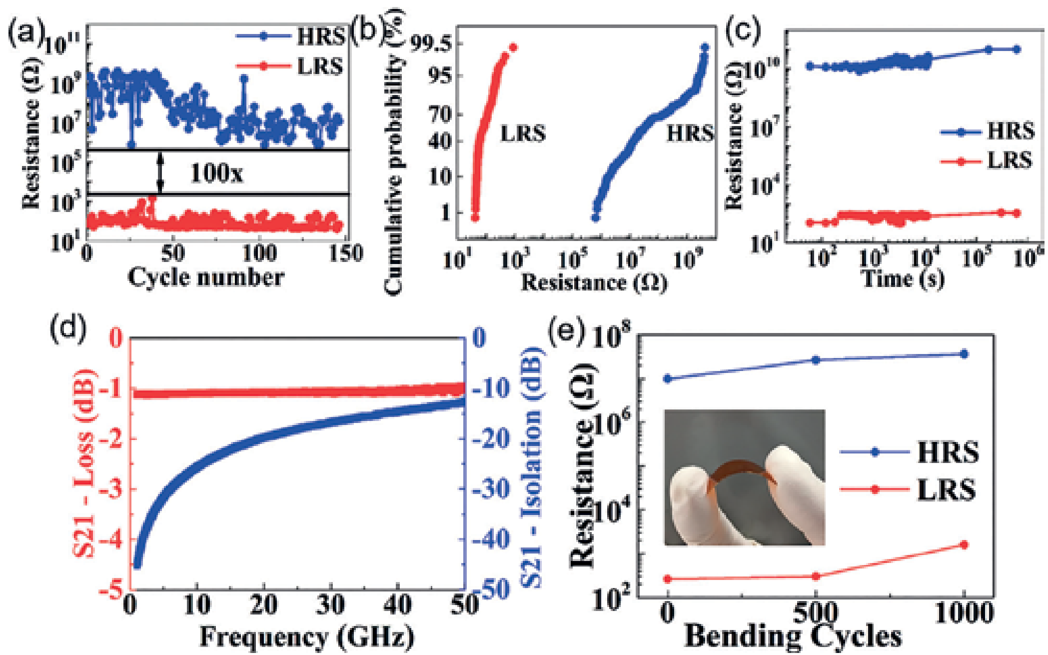

Figure 22. Characteristics of the atomistor. (a, b) Resistance spread of MoS_2 crossbar MIM devices for 150 manual dc switching cycles. (c) Time-dependent measurements of the MoS_2 switch with stable storage of information for a week at room temperature. Resistance of HRS and LRS is determined by measuring the current at a small bias voltage of 0.1 V. The area of this transverse device 2 L-MoS_2 is 2 × 2 μm^2. (d) Experimental, nonvolatile RF switches based on a 1 × 1 μm^2 MoS_2 monolayer show promising characteristics with an insertion loss of ~1 dB and isolation >12 dB up to 50 GHz. The cut-off frequency is ~1.8 THz. (e) Stable resistance of states with high resistance and low resistance after 1000 cycles of bending at 1% strain [23].

7. Conclusion

Memristive systems based on 2D-crystals, a new class of nonvolatile electronic components, are capable of solving the problem of scaling. Self-organized synapse-like memristive systems controlled by transitions between sp^3 and sp^2-configurations of carbon in an electric field can be applied in artificial neural networks and intelligent machines. The high-efficient switching of nonvolatile resistance in atomic single-layer TMD (MoS_2, $MoSe_2$, WS_2, WSe_2) memory is due to the inherent nature of layered crystallinity, which creates clear interfaces and clean tunnel barriers, which prevents excessive leakage and creates stable states. 2D memory can be used for existing applications in the memory/calculation area, as well as in new applications for radio frequency switching with extremely low power consumption. 2D photomemristors with a floating photogate show multiple states controlled in a wide range of electromagnetic radiation and can find application for a wide range of tasks related to neuromorphic computations, image processing and recognition of sounds, movements and speech necessary to create artificial intelligence. The future development of 2D memristive systems should use the possibility of self-organizing technology to form artificial neural networks and hetero-interface interactions of biocompatible 2D crystals, such as graphene, with natural neurons.

Acknowledgements

This research was supported by Basic Science Research Program (2017R1D1A1B03035102) through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Republic of Korea and by the Russian Foundation of Basic Research (N16-33-60229).

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Section 4

Pattern Recognition Using Memristor Models

Charge-Controlled Memristor Grid for Edge Detection

Arturo Sarmiento-Reyes and
Yojanes Rodríguez Velásquez

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.78610

Abstract

Nonlinear resistive grids have been extensively used in the past for achieving image filtering, focused on both smoothing and edge detection, by resorting to the nonlinear constitutive branch relationships of the elements in the array in order to carry out in fact a minimization algorithm. In this chapter, a specially tailored fully analytical charge-controlled memristor model is introduced and used in a memristive grid in order to handle the edge detection. The performance of the grid has been tested on a set of 500 images (clean and noisy) and shows an excellent agreement with the outcomes produced by humans.

Keywords: memristor modeling, memristive grids, symbolic memristor modeling, edge-detection, image processing

1. Introduction

An indispensable preprocessing for image signal treatment is edge detection, which consists in decomposing the original image into a family of topographical curves that corresponds with measured depth levels of intensity. The main outcome of edge detection is an image that contains diminished information which allows further complex forms of image processing.

In plain words, an edge is regarded as a sharp change in brightness or when the image fence contains physical discontinuities. As a preprocessing step to edge detection, a smoothing filter, typically Gaussian smoothing, is widely applied; as a clear consequence, the edge-detection methods differ in function of the smoothing filter used [1].

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In order to detect edges, several methods are reported in the study. In 1986, John Canny proposed a computational method for image edge detection. He introduced the notion of non-maximum suppression, which means that given the pre-smoothing filters, edge points are defined as points where the gradient magnitude assumes a local maximum in the gradient direction [2]. Although the method was developed in the early years of computer vision, it is still in the state of art.

Another method is based on anisotropic diffusion, which is a technique aiming at reducing the image noise without removing significant parts of the image such as edges, lines, or other details that are important for the interpretation of the image [3]. This method has evolved to nonlinear anisotropic diffusion, which consists in considering the original image as an initial state of a parabolic (diffusion-like) process and extracting filtered versions from its temporal evolution [4].

As a direct result, nonlinear resistive grids have been used to explicitly implement edge detection based on nonlinear anisotropic diffusion [5]. The nonlinear resistive grid and the elements of this processor are presented in **Figure 1(a)**; the voltage sources represent each pixel of the image to be processed and the node voltages represent each pixel of the processed image. It is important to note that each branch in the grid is composed of a nonlinear resistive element called fuse.

Because of the temporal evolution of the procedure, memristive grids naturally fit the features needed for achieving edge detection [6, 7]. A memristive grid has the same structure of its resistive counterpart, but the nonlinear resistors have been substituted by memristors, as depicted in **Figure 1(b)**.

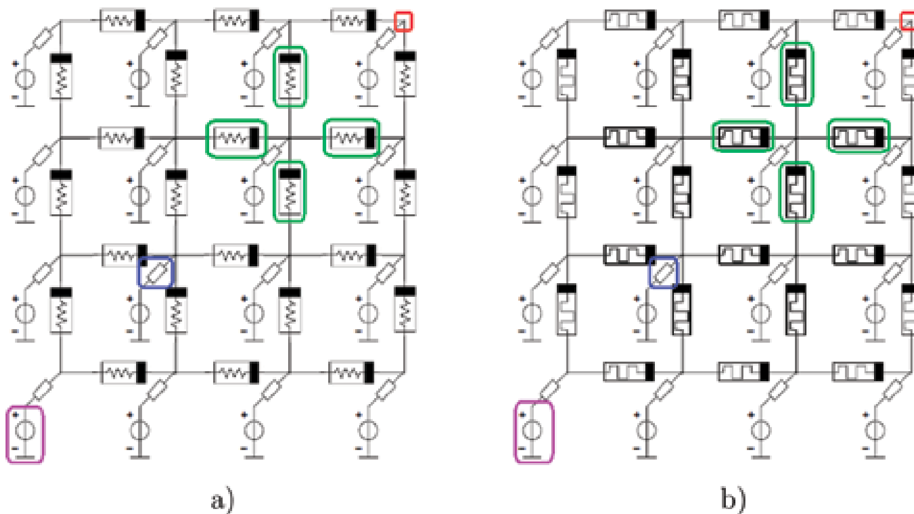

Figure 1. Structure and components of the (a) resistive grid and (b) memristive grid.

http://dx.doi.org/10.5772/intechopen.78610

The rest of this chapter is organized as follows: Section 2 deals with the development of the proposed model, and the resulting analytic expressions for the memristance are obtained. In Section 3, the characterization of the model is carried out in order to demonstrate that it fulfills the main fingerprints of the device. Section 4 highlights the main characteristics of the memristive grid and its components. In Section 5, the results of the application of the memristive grid to edge detection are presented. Finally, in Section 6, some conclusions are drawn and future lines of research are proposed.

2. Development of a charge-controlled memristor model

Professor Leon O. Chua predicted in 1971 the existence of the fourth basic circuit element [8]. He called it memristor and defined it as a passive device with two terminals, which branch constitutive function relates the magnetic flux linkage and the electric charge. In 2008, the R. Stanley Williams group at Hewlett-Packard Laboratories presented a device whose behavior exhibits the memristance phenomenon [9].

Novel memristor applications became the main thrust in the search for better and more reliable models of the device that can predict the behavior of the electronic system application. With the goal of developing a memristor model that can achieve edge detection with the memristive grid, several features are pursued:

- The model must be charge-controlled in order to reflect the dynamics of the edge detection.
- The model must be recast in a fully symbolic form in order to express the memristance as a function of the device parameters.
- The model must fulfill the fingerprints of the device [10].

The modeling methodology can be described as follows: first, the nonlinear drift mechanism is expressed as a function of charge instead of time; then, a symbolic solution $x(q)$ to the nonlinear equation is found, and finally, $x(q)$ is used to generate the memristance expression.

The nonlinear drift mechanism that governs the functioning of the HP memristor [9] is given hereafter as the ordinary differential equation (ODE) which is expressed in terms of the charge derivative:

$$\frac{dx(q)}{dq} = \eta\kappa f_w(x(q)) \tag{1}$$

where $\kappa = \frac{\mu_v R_{on}}{\Delta^2}$, μ_v is the mobility of the charges in the doped region, Δ is the total length of the device, η describes the displacement direction of $x(q)$ ($\eta = -1$ or $+1$), and R_{on} is the ON-sate resistance. Besides, $f_w(x(q))$ is the window function. We have selected the window given by [11]

$$f_w = 1 - (2x(q) - 1)^{2k} \tag{2}$$

where k controls the level of linearity, as k increases, the linearity increases in the range $0 \to 1$.

It is possible to find an analytical solution to Eq. (1) for $k = 1$; however, for $k > 1$, the solution can only be assessed by resorting to numeric analysis methods [11]. In this chapter, we resort to the homotopy perturbation method (HPM) reported in [12, 13] to obtain a symbolic solution $x(q)$ that contains the parameters of the memristor. In this method, different solutions are obtained for the choice made on the Joglekar exponent k and the order of the homotopy. Besides, it must be pointed out that a pair of solutions do indeed exist in every case because η takes values of $+1$ and -1 depending on the direction of the charge displacement.

As an example of the solution, the equation obtained for order-1, $k = 3$ and $\eta = -1$ is given as follows:

$$\begin{aligned} x_{k1,O3,\eta^-} = &\left(X_0^4 + X_0^3 + X_0^2 + X_0\right)e^{-4\kappa q} - \left(3X_0^4 + 2X_0^3 + X_0^2\right)e^{-8\kappa q} \\ &+ \left(3X_0^4 + X_0^3\right)e^{-12\kappa q} - X_0^4 e^{-16\kappa q} \end{aligned} \tag{3}$$

where X_0 corresponds to the initial value of the state variable (when the charge is zero). It can be noted that the model only converges for positive values of q, and the function tends to 0 when $q \to \infty$.

The solution for $\eta = +1$ and positive values of q are given by

$$\begin{aligned} x_{k1,O3,\eta^+} = &1 + \left(-X_0^4 + 5X_0^3 - 10X_0^2 + 10X_0 - 4\right)e^{-4\kappa q} + \left(3X_0^4 - 14X_0^3 + 25X_0^2 - 20X_0 + 6\right)e^{-8\kappa q} \\ &+ \left(-3X_0^4 + 13X_0^3 - 21X_0^2 + 15X_0 - 4\right)e^{-12\kappa q} + \left(X_0^4 - 4X_0^3 + 6X_0^2 - 4X_0 + 1\right)e^{-16\kappa q} \end{aligned} \tag{4}$$

In order to establish a comparison, the numerical solution to Eq. (1) is obtained with the Backward Euler method. **Figure 2** shows the plots of the solution $x(q)$ obtained with the numeric method and with HPM for homotopy orders 1–3 with $k = 1, 2$ for both directions. **Table 1** shows the values of the parameters used in these evaluations.

2.1. Memristance expressions

Once the solution $x(q)$ is obtained, it is substituted in the coupled resistor equivalent:

$$M(q) = R_{on}x(q) + R_{off}(1 - x(q)) \tag{5}$$

The expressions for the memristance for order-1 with $k = 1 - 5$ are given hereafter.

Expressions for $\eta = -1$

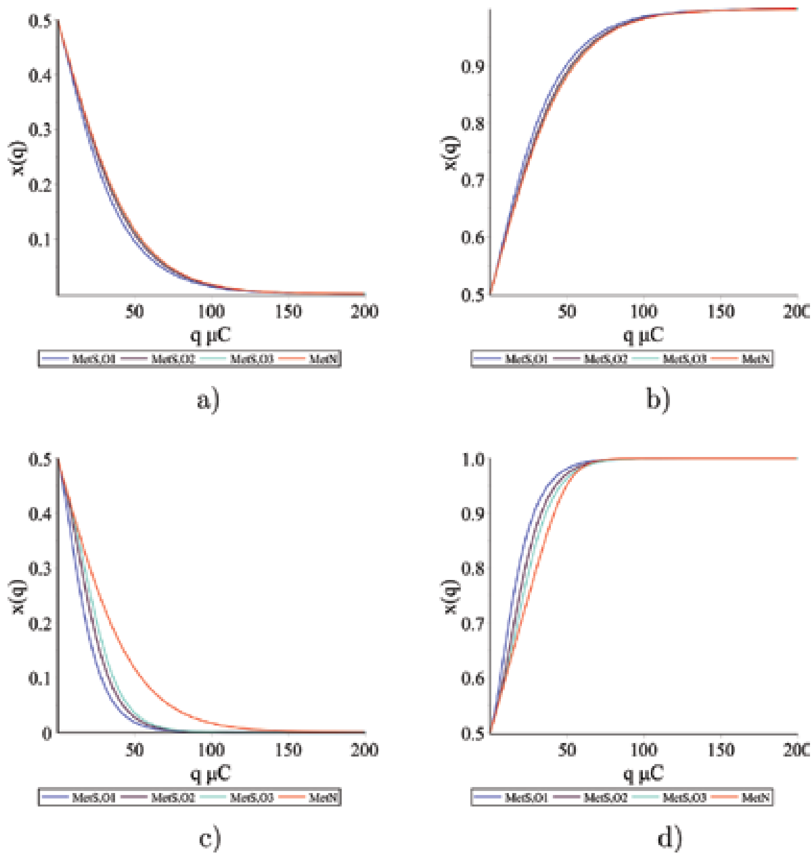

Figure 2. Plots of $x(q)$ for $k = 1, 2$. Numerical solution (red) and HPM solutions for order 1 (blue), order 2 (violet), and order 3 (cyan).

μ_v $(\mathbf{m^2/Vs})$	Δ (nm)	κ $(\mathbf{m/As})$	X_0
1×10^{-14}	10	10,000	0.5

Table 1. Parameters for the plots of $x(q)$.

$$M_{k1,O1,\eta^-} = \begin{cases} R_d(X_0 - 1)\left[(X_0 - 2)e^{4\kappa q} - (X_0 - 1)e^{8\kappa q}\right] + R_{on} & q \le 0 \\ R_d X_0\left[X_0 e^{-8\kappa q} - (X_0 + 1)e^{-4\kappa q}\right] + R_{off} & q > 0 \end{cases} \quad (6)$$

with $R_d = R_{off} - R_{on}$.

$$M_{k2,\,O1,\,\eta^-} = \begin{cases} R_d(X_0-1)\begin{bmatrix} \frac{1}{3}\left(2X_0^3+3X_0-8\right)e^{8\kappa q} - 3(X_0-1)e^{16\kappa q} \\ \\ -2(X_0-1)^2 e^{24\kappa q} - \frac{2}{3}(Xo-1)^3 e^{32\kappa q} \end{bmatrix} + R_{on} & q \leq 0 \\ R_d X_0 \begin{bmatrix} \frac{2}{3}X_0^3 e^{-32\kappa q} - 2X_0^2 e^{-24\kappa q} + 3X_0 e^{-16\kappa q} \\ \\ -\frac{1}{3}\left(2X_0^3 - 6X_0^2 + 9X_0 + 3\right)e^{-8\kappa q} \end{bmatrix} + R_{off} & q > 0 \end{cases} \tag{7}$$

$$M_{k3,\,O1,\,\eta^-} = \begin{cases} R_d(X_0-1)\begin{bmatrix} \frac{1}{15}\begin{pmatrix} 16X_0^5 - 20X_0^4 + 20X_0^3 \\ +15X_0 - 46 \end{pmatrix} e^{12\kappa q} \\ \\ -5(X_0-1)e^{24\kappa q} - \frac{20}{3}(X_0-1)^2 e^{36\kappa q} \\ \\ -\frac{20}{3}(Xo-1)^3 e^{48\kappa q} - 4(X_0-1)^4 e^{60\kappa q} \\ \\ -\frac{16}{15}(X_0-1)^5 e^{72\kappa q} \end{bmatrix} + R_{on} & q \leq 0 \\ R_d X_0 \begin{bmatrix} \frac{16}{15}X_0^5 e^{-72\kappa q} - 4X_0^4 e^{-60\kappa q} + \frac{20}{3}X_0^3 e^{-48\kappa q} \\ \\ -\frac{20}{3}X_0^2 e^{-36\kappa q} + 5X_0 e^{-24\kappa q} \\ \\ -\frac{1}{15}\left(16X_0^5 - 60X_0^4 + 100X_0^3 - 100X_0^2 + 75X_0 + 15\right)e^{-12\kappa q} \end{bmatrix} + R_{off} & q > 0 \end{cases} \tag{8}$$

$$M_{k4,O1,\eta^-} = \begin{cases} R_d(X_0-1)\left[\begin{array}{l} \frac{1}{105}\begin{pmatrix} 240X_0^7 - 560X_0^6 + 672X_0^5 \\ -420X_0^4 + 210X_0^3 + 105X_0 - 352 \end{pmatrix} e^{16\kappa q} \\ -7(X_0-1)e^{32\kappa q} - 14(X_0-1)^2 e^{48\kappa q} \\ -\frac{70}{3}(Xo-1)^3 e^{64\kappa q} - 28(X_0-1)^4 e^{80\kappa q} \\ -\frac{112}{5}(X_0-1)^5 e^{96\kappa q} - \frac{32}{3}(X_0-1)^6 e^{112\kappa q} \\ -\frac{17}{7}(X_0-1)^7 e^{128\kappa q} \end{array}\right] + R_{on} & q \le 0 \\ R_d X_0 \left[\begin{array}{l} \frac{16}{7}X_0^7 e^{-128\kappa q} - \frac{32}{3}X_0^6 e^{-112\kappa q} \\ +\frac{112}{5}X_0^5 e^{-96\kappa q} - 28X_0^4 e^{-80\kappa q} \\ +\frac{70}{3}X_0^3 e^{-64\kappa q} - 14X_0^2 e^{-48\kappa q} \\ +7X_0 e^{-32\kappa q} \\ -\frac{1}{105}\begin{pmatrix} 240X_0^7 - 1120X_0^6 + 2352X_0^5 - 2940X_0^4 \\ +2450X_0^3 - 1470X_0^2 + 735X_0 + 105 \end{pmatrix} e^{-16\kappa q} \end{array}\right] + R_{off} & q > 0 \end{cases} \tag{9}$$

$$M_{k5,O1,\eta^-} = \begin{cases} R_d(X_0-1)\left[\begin{array}{l} \frac{1}{135}\left(\begin{array}{l}1792X_0^9 - 6048X_0^8 + 9792X_0^7 - 9408X_0^6 \\ +6048X_0^5 - 2520X_0^4 + 840X_0^3 + 315X_0 - 1126\end{array}\right)e^{20\kappa q} \\ -9(X_0-1)e^{40\kappa q} - 24(X_0-1)^2 e^{60\kappa q} \\ -56(Xo-1)^3 e^{80\kappa q} - \frac{504}{5}(X_0-1)^4 e^{100\kappa q} \\ -\frac{672}{5}(X_0-1)^5 e^{120\kappa q} - 128(X_0-1)^6 e^{140\kappa q} \\ -\frac{576}{7}(X_0-1)^7 e^{160\kappa q} - 32(X_0-1)^8 e^{180\kappa q} \\ -\frac{256}{45}(X_0-1)^9 e^{200\kappa q} \end{array}\right] + R_{on} & q \leq 0 \\ R_d X_0 \left[\begin{array}{l} \frac{256}{45}X_0^9 e^{-200\kappa q} - 32X_0^8 e^{-180\kappa q} \\ +\frac{576}{7}X_0^7 e^{-160\kappa q} - 128X_0^6 e^{-140\kappa q} \\ +\frac{672}{5}X_0^5 e^{-120\kappa q} - \frac{504}{5}X_0^4 e^{-100\kappa q} \\ +56X_0^3 e^{-80\kappa q} - 24X_0^2 e^{-60\kappa q} \\ +9X_0 e^{-40\kappa q} \\ -\frac{1}{135}\left(\begin{array}{l}1792X_0^9 - 10080X_0^8 + 25920X_0^7 - 40320X_0^6 \\ +42336X_0^5 - 31752X_0^4 + 17640X_0^3 - 7560X_0^2 + 2835X_0 + 315\end{array}\right)e^{-20\kappa q} \end{array}\right] + R_{off} & q > 0 \end{cases} \tag{10}$$

Expressions for $\eta = +1$

$$M_{k1,O1,\eta^+} = \begin{cases} R_d X_0\left[X_0 e^{8\kappa q} - (X_0+1)e^{4\kappa q}\right] + R_{off} & q \leq 0 \\ R_d(X_0-1)\left[(X_0-2)e^{-4\kappa q} - (X_0-1)e^{-8\kappa q}\right] + R_{on} & q > 0 \end{cases} \tag{11}$$

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$$M_{k2,O1,\eta^+} = \begin{cases} R_d X_0 \begin{bmatrix} \frac{2}{3} X_0^3 e^{32\kappa q} - 2X_0^2 e^{24\kappa q} + 3X_0 e^{16\kappa q} \\ \\ -\frac{1}{3}\left(2X_0^3 - 6X_0^2 + 9X_0 + 3\right) e^{8\kappa q} \end{bmatrix} + R_{off} & q \leq 0 \\ R_d (X_0 - 1) \begin{bmatrix} \frac{1}{3}\left(2X_0^3 + 3X_0 - 8\right) e^{-8\kappa q} - 3(X_0 - 1) e^{-16\kappa q} \\ \\ -2(X_0 - 1)^2 e^{-24\kappa q} - \frac{2}{3}(Xo - 1)^3 e^{-32\kappa q} \end{bmatrix} + R_{on} & q > 0 \end{cases} \tag{12}$$

$$M_{k3,O1,\eta^+} = \begin{cases} R_d X_0 \begin{bmatrix} \frac{16}{15} X_0^5 e^{72\kappa q} - 4X_0^4 e^{60\kappa q} + \frac{20}{3} X_0^3 e^{48\kappa q} \\ \\ -\frac{20}{3} X_0^2 e^{36\kappa q} + 5X_0 e^{24\kappa q} \\ \\ -\frac{1}{15}\left(16^5 - 60X_0^4 + 100X_0^3 - 100X_0^2 + 75X_0 + 15\right) e^{12\kappa q} \end{bmatrix} + R_{off} & q \leq 0 \\ R_d (X_0 - 1) \begin{bmatrix} \frac{1}{15}\left(16X_0^5 - 20X_0^4 + 20X_0^3 + 15X_0 - 46\right) e^{-12\kappa q} \\ \\ -5(X_0 - 1) e^{-24\kappa q} - \frac{20}{3}(X_0 - 1)^2 e^{-36\kappa q} \\ \\ -\frac{20}{3}(Xo - 1)^3 e^{-48\kappa q} - 4(X_0 - 1)^4 e^{-60\kappa q} \\ \\ -\frac{16}{15}(X_0 - 1)^5 e^{-72\kappa q} \end{bmatrix} + R_{on} & q > 0 \end{cases} \tag{13}$$

$$M_{k4,O1,\eta^{+}} = \begin{cases} R_d X_0 \left[\begin{array}{l} \frac{16}{7} X_0^7 e^{128\kappa q} - \frac{32}{3} X_0^6 e^{112\kappa q} + \frac{112}{5} X_0^5 e^{96\kappa q} \\ -28 X_0^4 e^{80\kappa q} + \frac{70}{3} X_0^3 e^{64\kappa q} - 14 X_0^2 e^{48\kappa q} + 7 X_0 e^{32\kappa q} \\ -\frac{1}{105} \left(\begin{array}{l} 240X_0^7 - 1120X_0^6 + 2352X_0^5 - 2940X_0^4 \\ +2450X_0^3 - 1470X_0^2 + 735X_0 + 105 \end{array} \right) e^{16\kappa q} \end{array} \right] + R_{off} & q \leq 0 \\ R_d (X_0 - 1) \left[\begin{array}{l} \frac{1}{105} \left(\begin{array}{l} 240X_0^7 - 560X_0^6 + 672X_0^5 - 420X_0^4 \\ +210X_0^3 + 105X_0 - 352 \end{array} \right) e^{-16\kappa q} \\ -7(X_0 - 1) e^{-32\kappa q} - 14 (X_0 - 1)^2 e^{-48\kappa q} \\ -\frac{70}{3} (Xo - 1)^3 e^{-64\kappa q} - 28 (X_0 - 1)^4 e^{-80\kappa q} \\ -\frac{112}{5} (X_0 - 1)^5 e^{-96\kappa q} - \frac{32}{3} (X_0 - 1)^6 e^{-112\kappa q} \\ -\frac{17}{7} (X_0 - 1)^7 e^{-128\kappa q} \end{array} \right] + R_{on} & q > 0 \end{cases} \tag{14}$$

$$M_{k5,O1,\eta^{+}} = \begin{cases} R_d X_0 \left[\begin{array}{l} \frac{256}{45} X_0^9 e^{200\kappa q} - 32 X_0^8 e^{180\kappa q} + \frac{576}{7} X_0^7 e^{160\kappa q} \\ -128 X_0^6 e^{140\kappa q} + \frac{672}{5} X_0^5 e^{120\kappa q} - \frac{504}{5} X_0^4 e^{100\kappa q} \\ +56 X_0^3 e^{80\kappa q} - 24 X_0^2 e^{60\kappa q} + 9 X_0 e^{40\kappa q} \\ -\frac{1}{135} \left(\begin{array}{l} 1792X_0^9 - 10080X_0^8 + 25920X_0^7 - 40320X_0^6 + 42336X_0^5 \\ -31752X_0^4 + 17640X_0^3 - 7560X_0^2 + 2835X_0 + 315 \end{array} \right) e^{20\kappa q} \end{array} \right] + R_{off} & q \leq 0 \\ R_d (X_0 - 1) \left[\begin{array}{l} \frac{1}{135} \left(\begin{array}{l} 1792X_0^9 - 6048X_0^8 + 9792X_0^7 - 9408X_0^6 + 6048X_0^5 \\ -2520X_0^4 + 840X_0^3 + 315X_0 - 1126 \end{array} \right) e^{-20\kappa q} \\ -9(X_0 - 1) e^{-40\kappa q} - 24 (X_0 - 1)^2 e^{-60\kappa q} \\ -56 (Xo - 1)^3 e^{-80\kappa q} - \frac{504}{5} (X_0 - 1)^4 e^{-100\kappa q} \\ -\frac{672}{5} (X_0 - 1)^5 e^{-120\kappa q} - 128 (X_0 - 1)^6 e^{-140\kappa q} \\ -\frac{576}{7} (X_0 - 1)^7 e^{-160\kappa q} - 32 (X_0 - 1)^8 e^{-180\kappa q} \\ -\frac{256}{45} (X_0 - 1)^9 e^{-200\kappa q} \end{array} \right] + R_{on} & q > 0 \end{cases} \tag{15}$$

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3. Characterization of the model

The developed model is tested in order to verify that it fulfills the main fingerprints of the device [10]. The nominal values of the HP memristor [9] are used, as shown in **Table 2**, where A_p is the amplitude of the sinusoidal stimuli.

On one side, the $v(t)$-$i(t)$ characteristic of a memristor must be a pinched hysteresis loop (PHL). Besides, the area of the PHL must decrease with the frequency. In the limit as the frequency tends to infinity, the memristor behaves as a linear resistor. In **Figure 3**, the PHLs are shown for $k = 1, 5$ and $\omega = 1, 2, 5, 10$.

Figure 4 shows the area as a function of the frequency. It can be verified that the lobe area decreases monotonically with the frequency from a critical value ω_c. **Table 3** shows these values for $k = 1 - 5$.

On the other side, as the frequency tends to infinity, the value of the memristance becomes constant and the device acts as a linear resistor [10]. The limit of the memristance when the frequency $\omega \to \infty$ can be expressed as

$$\lim_{\omega \to \infty} \left(M_{k_i, O_j} \right) = X_0 R_{on} + (1 - X_0) R_{off} = R_{init} \tag{16}$$

where k_i and O_i are the selected k and homotopy order, respectively.

μ_v (m²/Vs)	Δ (nm)	κ (m/As)	R_{on} (Ω)	R_{off} (Ω)	X_0	A_p (μA)	η
1×10^{-14}	10	10,000	100	16×10^3	0.5	40	+1

Table 2. Parameter values used in the characterization.

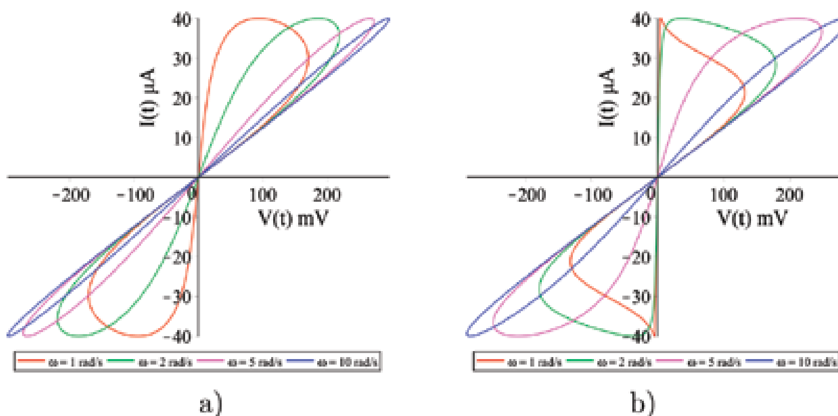

Figure 3. Frequency behavior of the pinched hysteresis loops for (a) $k = 1$ and (b) $k = 5$.

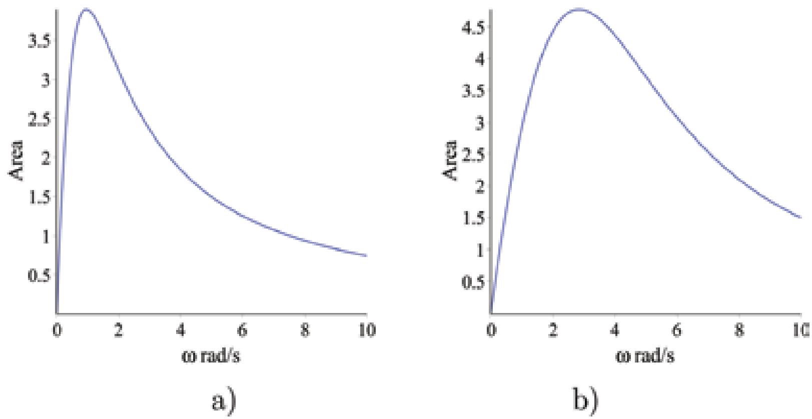

Figure 4. PHL lobe area as a function of the frequency (units of area in μm^2) for (a) $k = 1$ and (b) $k = 5$.

k	1	2	3	4	5
ω_c	0.947	1.252	1.656	2.013	2.828

Table 3. Critical frequencies for different values of k.

3.1. Comparison with other models

Several models are already reported in the study, which have been developed for different applications. A first scheme is reported in [14] in the form of a macro-model implemented in the SPICE circuit simulator. The second model is reported in [15], which is a mathematical model implemented in MATLAB. **Figure 5** shows the $v(t) - i(t)$ characteristics of these models and our charge-controlled model. For the sake of comparison, the model $M_{k1,O3}$ is used.

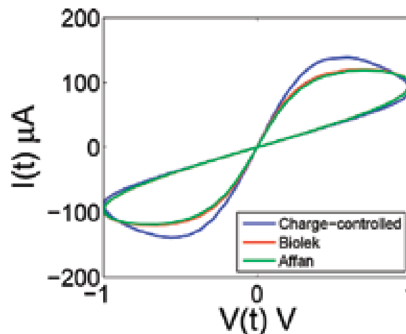

Figure 5. Comparison of the $v(t) - i(t)$ curves.

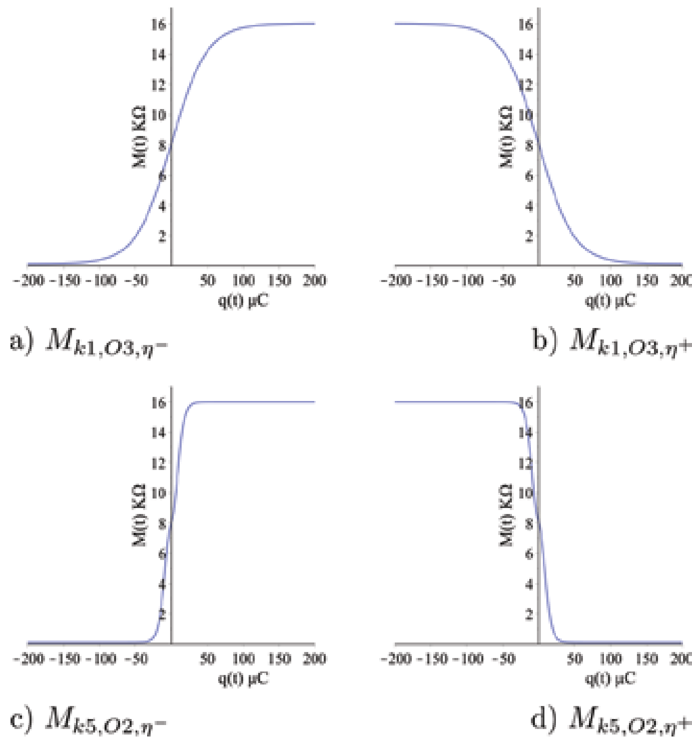

Figure 6. Memristance-charge characteristics.

3.2. Memristance-charge characteristic

Figure 6 shows the $M - q$ curves of the model for both cases of η. It can be seen that for $\eta = -1$, the memristance tends to R_{off} in the positive range of the charge and tends to R_{on} in the negative range of q. On the contrary, when $\eta = +1$, the memristance tends to R_{on} in the positive range of the charge and to R_{off} in the negative range. Besides, the curves with higher k show a sharper transition.

4. Memristive grid for edge detection

Figure 1(b) shows the memristive grid used for edge detection. In fact, each fuse of the grid consists of two memristors in an anti-series connection, that is, the series connection of two memristors connected back to back, as shown in **Figure 7(a)**. The combined $M - q$ characteristic of the memristive fuse has the shape depicted in **Figure 7(b)**. Ideally, the ON-state memristance is zero and the slope from the ON-state to the OFF-state around Q_t is infinite. In

practice, M_{on} has a very low value, and M_{off} takes a very high value. The value of Q_t defines the degree of smoothing: more smoothing is related to larger M_q, which implies longer settling times in the edge detection. Besides, the memristance threshold M_{th}, which is related to Q_t, is selected to define which pixel is identified as an edge of the original image.

Figure 7(c) shows the $M - q$ characteristic of the fuse to be used in the memristive grid. The parameters of the model are recast in **Table 4**.

The importance of a smart selection on the $M - q$ characteristic resides in the fact that it allows us to achieve an appropriate smoothing preprocessing [16]. A figure of merit of great significance is the relation between the smoothing level L and the branch memristance in the grid, M_{branch}. In fact, L is a space constant that serves to measure the smoothing as a number of pixels:

$$\lambda = \frac{M_{branch}}{R_{in}}; \qquad \varsigma = \cosh^{-1}\left(1 + \frac{\lambda}{2}\right); \qquad L = \frac{1}{\varsigma}; \tag{17}$$

Some additional considerations must be taken into account for processing images with a memristive grid, due to the fact that the memristive grid implements a nonlinear anisotropic method. Namely, the method needs a stop criterion to find a solution [17]. The images processed with the memristive grid are in gray scale, and a threshold to stop the process is selected.

4.1. Solving the memristive grid

The equations emanating from the memristive grid form a set of differential algebraic equations (DAEs) that is solved with MATLAB. The number of pixels of the image determines the size of the grid and therefore the number of DAEs.

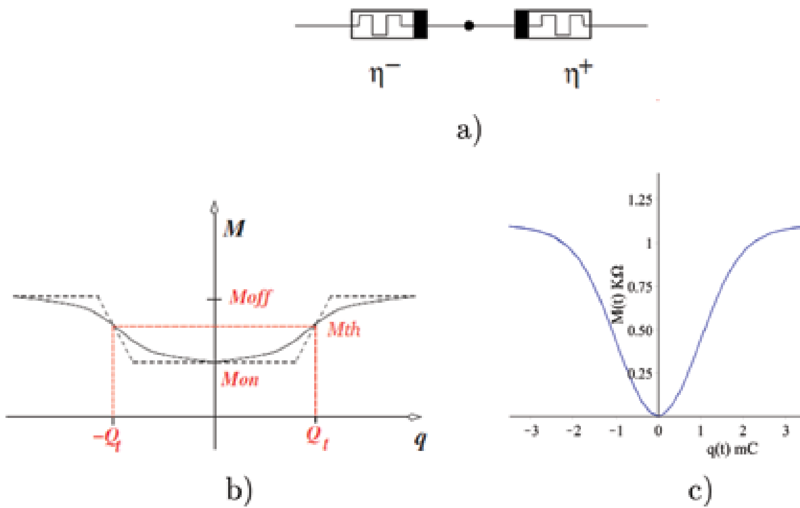

Figure 7. Memristive fuse: (a) anti-series connection, (b) schematic M-q characteristic, and (c) M-q characteristic of the fuse.

http://dx.doi.org/10.5772/intechopen.78610

Parm.	μ_v (m^2/Vs)	R_{on} (Ω)	Δ (nm)	R_{init} (Ω)	X_0	R_{off} (Ω)	M_{on} (Ω)	M_{off} (Ω)	R_{in} (Ω)
Value	1×10^{-14}	1	10	1.1	0.999	1100	2.2	1101	50

Table 4. Nominal parameter values.

Figure 8 shows a single node of the grid (node $N_{i,j}$). Herein, the voltage source $d_{i,j}$ is associated with the pixel i, j, which takes values between $0 \rightarrow 1 \; V$. KCL analysis of the output node $N_{i,j}$ yields

$$I_{in} + I_{i-1,j} + I_{i+1,j} + I_{i,j-1} + I_{i,j+1} = 0 \tag{18}$$

This can be established as

$$\frac{d_{i,j} - u_{i,j}}{R_{in}} + \frac{u_{i-1,j} - u_{i,j}}{M_{i-1,j}} + \frac{u_{i+1,j} - u_{i,j}}{M_{i+1,j}} + \frac{u_{i,j-1} - u_{i,j}}{M_{i,j-1}} + \frac{u_{i,j+1} - u_{i,j}}{M_{i,j+1}} = 0 \tag{19}$$

where $M_{i-1,j}, M_{i+1,j}, M_{i,j-1}, M_{i,j+1}$ are the memristances incident to the node.

For an $m \times n$ image, KCL analysis on the complete grid yields a system of $m \times n$ DAEs that is solved for the nodal voltages $u_{i,j}$. Moreover, the associated charges of the memristors are calculated by the numerical integration of their currents by using the trapezoidal integration rule. In a last step, the memristance is updated in the charge-controlled model.

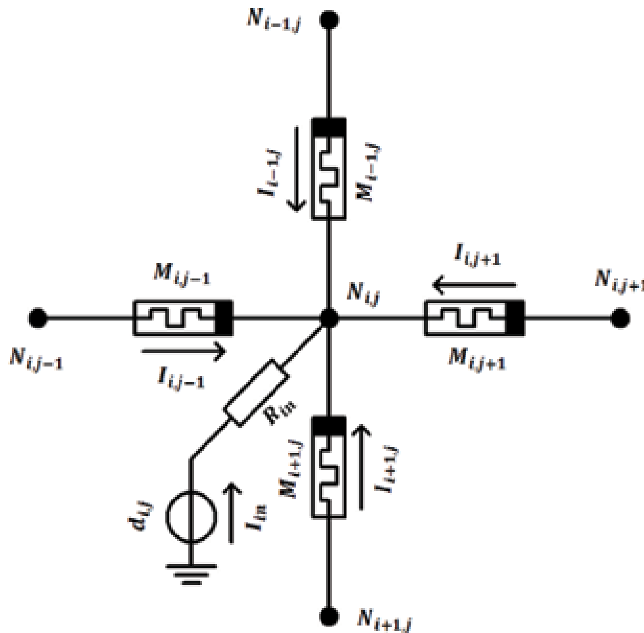

Figure 8. Current contributions at node $N_{i,j}$.

As shown in Eq. (17), the level of smoothing depends on the rate $\frac{M_{branch}}{R_{in}}$, that is, the equivalent of each memristance arriving to the node $N_{i,j}$ divided by the input resistance. The initial condition of the memristive grid is $\frac{M_{on}}{R_{in}} = 0.044$ which corresponds to $L = 4.78$ pixels.

The dynamics of the grid comes from the time-dependent behavior of the memristance, which implies that the value of M_{branch} increases with t causing in turn a low level of smoothing. In fact, after a long period of time, the output image gets closer to the original image. It clearly results that a stop criterion is needed.

This criterion is the smoothing time t_{smooth}, since it defines when the smoothing level of the output image is reached. At this point, the edges are determined by those nodes in the grid where the fuses have reached M_{th}. This threshold is referred to as a fraction of the maximum value of the memristance. A percentage of 2 of M_{off} has been used, allowing edges to be detected when the output image still retains a high level of smoothing. As a result, edge detection can be efficiently performed even for images with high levels of noise.

5. Results and comparisons

A benchmark image and its edges drawn by five human observers are presented in **Figure 9** (extracted from the database BSD300 [18]). This image is used to evaluate the performance of the memristive grid.

Figure 10 shows the output image for several levels of smoothing at different transient values. It allows us to verify that as the time increases, the smoothing level decreases, that is, the original image tends to be unveiled.

5.1. Figures of merit for the edge-detection procedure

A way of evaluating the efficiency is by means of the precision-recall curve and the parameter F [19]. On one side, the precision (P) is given as

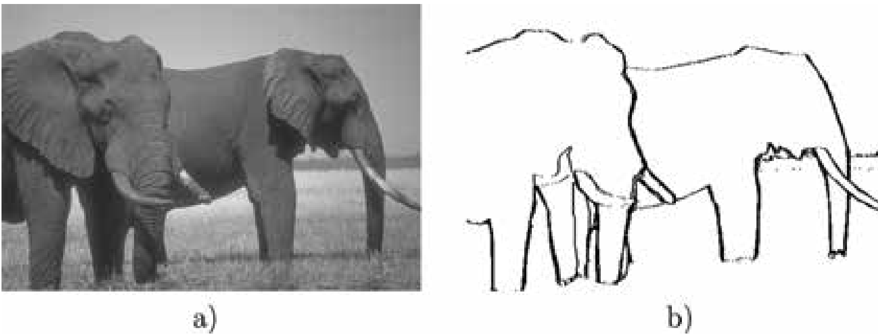

Figure 9. (a) Benchmark image and (b) ground truth for the edges of the benchmark image.

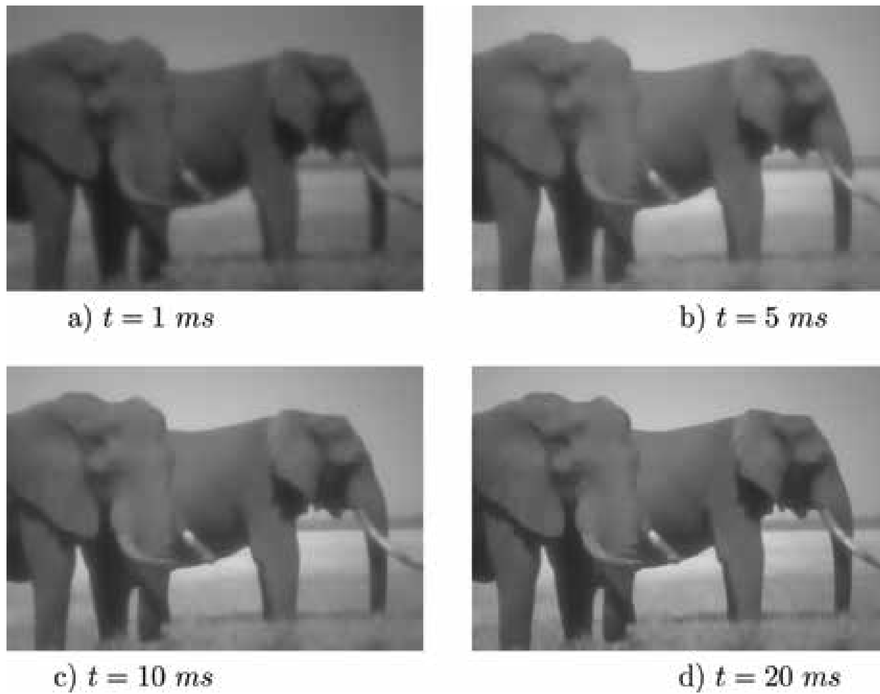

Figure 10. Smoothing procedure: output image.

$$P = \frac{T_P}{T_P + F_P} \tag{20}$$

where T_P is the number of pixels that belong to the evaluated edge as well as to the reference edge (true positives), and F_P is the number of pixels that belong to the evaluated edge but not to the reference edge (false positives). In fact, the precision denotes the quality of the detector.

On the other side, the recall parameter is defined as

$$R = \frac{T_P}{T_B} \tag{21}$$

where T_B is the total number of pixels that belong to the edge in the reference image. Actually, the recall factor indicates the probability for an edge to be detected.

Another commonly used parameter is the precision-recall cost ratio F:

$$F = \frac{PR}{\beta P + (1 - \beta)R} \tag{22}$$

where $\beta \in 0 \rightarrow 1$. In order to have a balanced ratio, $\beta = 0.5$ has been used.

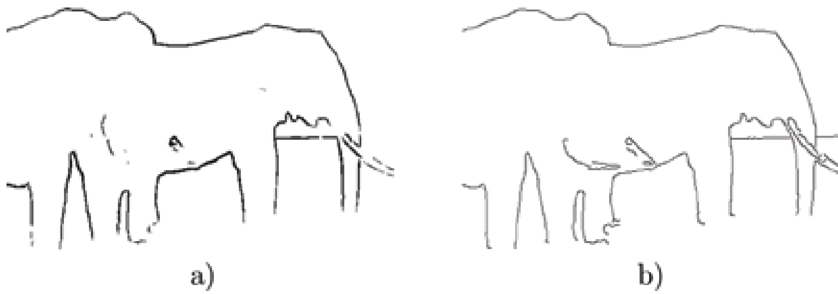

Figure 11. Edge detection: (a) memristive grid at $t = 20.45$ ms, (b) Canny's method [2] for a threshold 0.422.

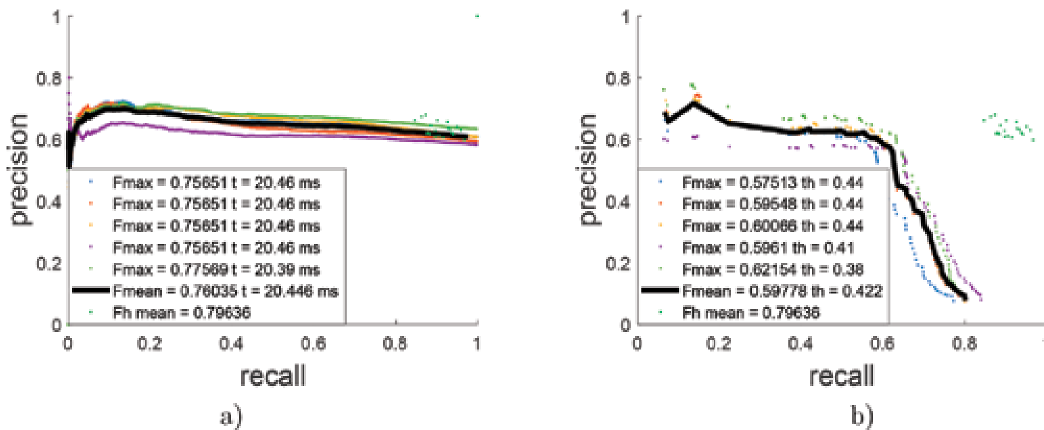

Figure 12. Precision-recall plots: (a) memristive grid and (b) Canny's method [2].

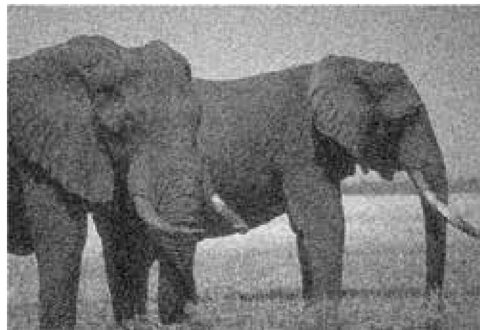

Figure 13. Benchmark image with Gaussian noise.

The result of the edge-detection procedure is shown in **Figure 11(a)** for the memristive grid and in **Figure 11(b)** for Canny's method [2].

The precision-recall ($P - R$) curves are given in **Figure 12(a)** for the memristive grid and (b) for Canny's method. In these plots, the black line represents the average of five curves obtained for

http://dx.doi.org/10.5772/intechopen.78610

Figure 14. Edge detection for the benchmark image with noise: (a) memristive grid at $t = 19.65\,\text{ms}$ and (b) Canny's method [2] for a threshold 0.443.

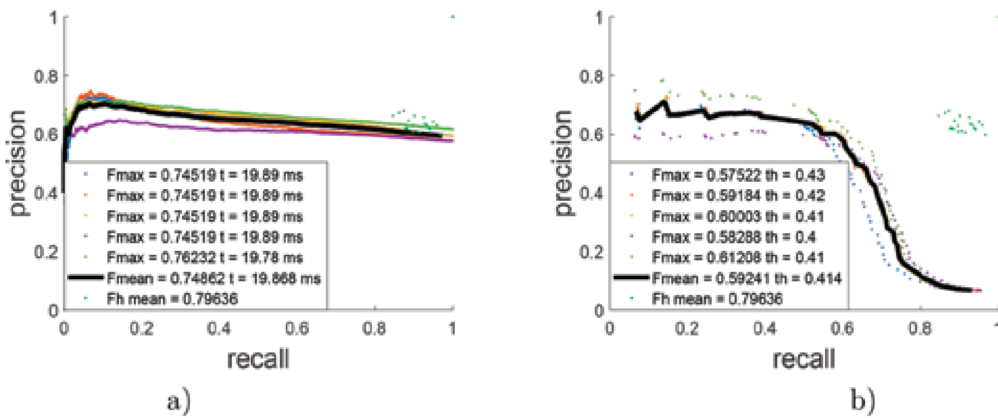

Figure 15. Precision-recall plots for the benchmark image with noise: (a) memristive grid and (b) Canny's method [2].

different transients for the memristive grid and five curves with different thresholds for Canny's method. In addition, the ground truth subjects have been cross-compared and the results are denoted by the green points, which are close to the human average as reported in [19].

The maximum F for the memristive grid is 0.76, and it was obtained at $t_{smooth} = 20.45$ ms, while for Canny's method, the maximum F is 0.59 for a threshold of 0.422. In this case, the smoothing time is measured when the maximum of F parameter is reached, and this is the stop criterion of the method; however, when there is no ground truth to compare the detected edge, the stop criterion must be t_{smooth}. The human average F (for the five test observers) is 0.80 [19]. Therefore, the outcomes of the memristive grid exhibit an excellent agreement with outcomes made by humans.

5.2. Processing the noisy image

In order to evaluate the performance of the memristive grid in edge detection for images with noise, Gaussian noise is added to the benchmark image depicted in **Figure 9**. The noisy image

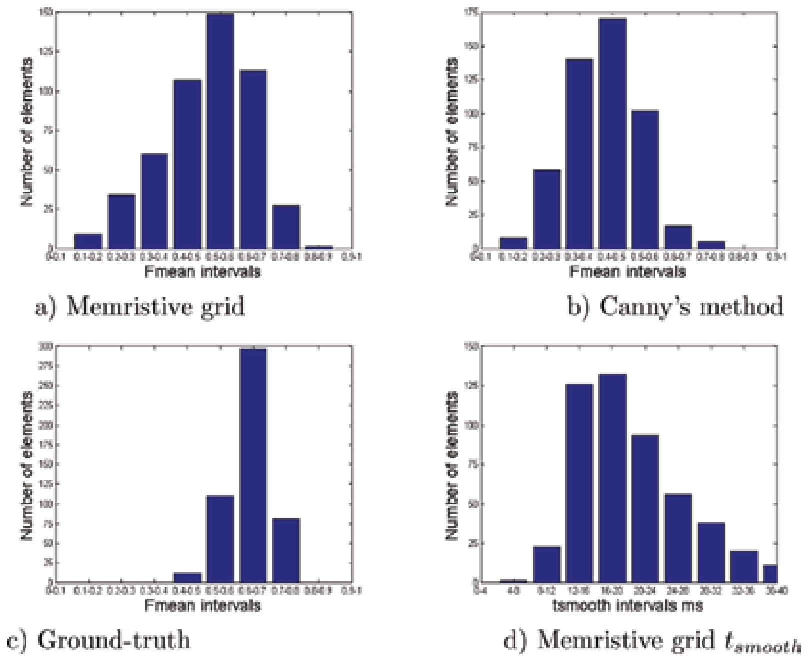

Figure 16. Histograms for 500 images from the database BSD500 [19].

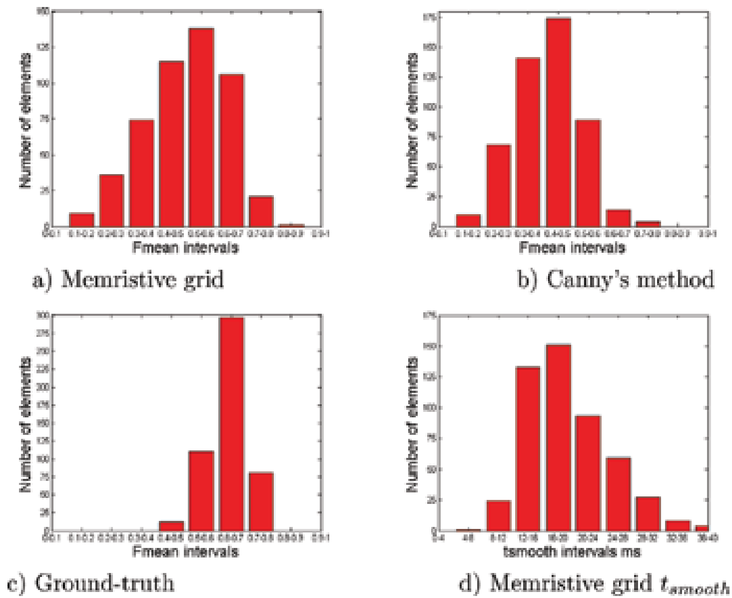

Figure 17. Histograms for 500 images with Gaussian noise from the database BSD500 [19].

(**Figure 13**) is processed with the memristive grid and Canny's method; the edges detected are shown in **Figure 14(a)** and **(b)**, respectively.

Figure 15 shows the $P - R$ curves for the memristive grid and for Canny's method. The maximum F for the memristive grid is 0.75, and it was obtained at $t_{smooth} = 19.87$ ms, while for Canny's method, the maximum is 0.59 for a threshold of 0.414. For the image under test, the F measure does not show a significant difference between the noisy and the original image.

5.3. Comparative results on a set of 500 images

In this paragraph, the performance of the grid is evaluated for 500 images extracted from the database BSD500 [19]. **Figure 16** shows the statistics on the F value for the memristive grid, Canny's method, and the human observers. Also, the histogram for the smoothing time in the memristive grid is presented. It can be noticed that the memristive grid produces 149 images with the average F, while Canny's method produces 174. However, it must be pointed out that these average images are obtained with better F with the memristive grid. In addition, the human F results from the database show a less spread distribution centered in the class 0.6–0.7 for nearly 300 images.

A similar analysis is carried out on the set with noisy images. Gaussian noise with mean 0 and variance 0.01 has been added to the input images. The statistics are shown in **Figure 17**.

6. Conclusions

A symbolic model for a charge-controlled memristor has been developed. The model has been incorporated to a memristive grid that has been used as a filter for image smoothing and edge detection. A simple evaluation of the memristance expression confirmed that the model fulfills the fingerprints for the $i - v$ pinched hysteresis loop. Besides, special attention was devoted to the memristance-charge characteristic of the anti-series connection because it constitutes the key element in the memristive grid for achieving edge detection.

The methods for image edge detection usually use a smoothing filter as the first step to improve edge detection. However, in the memristive grid, the smoothing filter is naturally implemented by the same circuit, which allows to have an analog processor that implements both functions. In addition, the grid presents a good performance in edge detection in comparison with the human outcomes.

Future lines of research are mainly devoted to speed up the edge-detection procedure for high-resolution images. A relevant topic is to solve the DAEs emanating from the memristive grid by performing parallel computations on multicore computers. In this case, the edge detection can be applied to images arising from data-intensive scenarios, such as medical imaging and remote-sensing imagery.

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Edited by Calin Ciufudean

Nowadays, scientific research deals with alternative solutions for creating non-traditional computing systems, such as neural network architectures where the stochastic nature and live dynamics of memristive models play a key role.

The features of memristors make it possible to direct processing and analysis of both biosystems and systems driven by artificial intelligence, as well as develop plausible physical models of spiking neural networks with self-organization.

This book deals with advanced applications illustrating these concepts, and delivers an important contribution for the achievement of the next generation of intelligent hybrid biostructures.

Different modeling and simulation tools can deliver an alternative to funding the theoretical approach as well as practical implementation of memristive systems.

Published in London, UK
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