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Edited by Dhanasekaran Vikraman and Hyun-Seok Kim

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Contributors

Dian Lei, Xiao Gong, Soheli Farhana, Erping Deng, Qiye Wen, Yu-Lian He, Zhi Chen, Qing-Hui Yang, Huai-Wu Zhang, Rupam Goswami, Brinda Bhowmick, Juan Antonio Delgado Notario, Vito Clerico, Kristel Fobelets, Enrique Velazquez, Yahya Moubarak Meziani, Lucas Fugikawa Santos, Giovani Gozzi, Guilherme De Lima, João Paulo Braga

Notice

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Meet the editors

Dr. Dhanasekaran Vikraman is an Assistant Professor at the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, Korea. He received his bachelor's degree from Mannai Rajagopalaswamy Govt. Arts College, Mannargudi, affiliated to Bharathidasan University, Tiruchirappalli, India. After that, he completed his Master's and PhD degrees at the Department of Physics, Alagappa University, India. Later, he received a visiting scientist position at KIST, Korea; a Marie Curie Experienced Researcher Fellowship at the Department of Physics, Aristotle University of Thessaloniki, Greece; and a post-doc position at Sejong University and Ajou University, Korea. Dr. Dhanasekaran Vikraman has authored 84 international journal papers, 71 conference papers and 1 book chapter. His research interests are mainly focused on low-cost synthesis of inorganic materials and 2D materials for electronics and energy applications.

Professor Hyun-Seok Kim received his MSc and PhD degrees in electrical engineering from the University of Wisconsin-Madison, USA, in 2003 and 2007, respectively. He was a post-doctoral researcher at the University of Wisconsin-Madison where he was involved in the design and fabrication of nanoelectromechanical single electron transistors. He then joined Intel Corporation in the USA as a senior R&D engineer from 2008 to 2011. He is currently an Associate Professor in the Division of Electronics and Electrical Engineering, Dongguk University, Seoul, South Korea. His main research interests are nano- and microelectronics and their application in sensors and energy-saving devices.

Contents

Preface

Field effect transistors (FETs) are the fundamental building blocks of microelectronics. In recent years, research on microelectronics has been specifically focused on the proposition of efficient alternative methodologies and materials to fabricate feasible integrated circuits. This book provides a general background of thin film transistors and their simulations. Recent developments in the realm of microelectronics are elaborated with evidence. The FET models and various related issues are also carefully described. The contents of the book are broadly classified into two topics: design and simulation of FETs and construction of FETs. The design and simulation of transistors section is elaborated in Chapters 1 to 5. Chapter 1 describes the 14-nm technology node to model nanosized transistors. Chapter 2 gives a brief account of the existing works on FET-based biosensors, the principle of dielectric modulation in tunnel field effect transistors (TFETs), and TFET simulations using technology computer-aided design (TCAD). Also, a circular gate TFET is presented as a dielectric-modulated biosensor and its practical implications are explained. Chapter 3 presents TFET bandgap modulation, which is supported by simulation results. The different TFET electrical parameters are also propounded in Chapter 3 using TCAD simulations. Chapter 4 reports an experimental and theoretical study of Schottky-gated strained-Si modulation-doped field-effect transistors (MODFETs) with different sub-micron gate lengths of 100, 250, and 500 nm. This chapter also elaborates the performance of strained-Si MODFETs at room temperature detection of 0.15 and 0.3 THz via TCAD simulations . Chapter 5 demystifies the role of clamping force on insulated gated bipolar transistors.

The construction of transistors is explained in Chapters 6 to 8. Chapter 6 demonstrates the effect of sulfur passivation on the surface of $Ge_{0.83}Sn_{0.17}$ for p-channel metal-oxide-semiconductor field-effect transistors (p-MOSFETs). In addition, it also explains the growth conditions, characterization, and construction parameters of p-MOSFETs. Chapter 7 provides a short review of THz modulators and graphene FETs. The device structure, its construction, and the experimental observation of modulation characteristics of graphene FET-based THz modulators are also probed in detail for both rigid and flexible devices. Chapter 8 gives a brief introduction to TFTs based on transparent semiconducting metal oxides (SMOs) with special focus on solution-processed devices. It also explains the electrical properties of TFTs with the different active layer compositions such as intrinsic zinc oxide (ZnO), aluminum-doped ZnO, and indium-doped ZnO.

All the authors anticipate that the provided chapters will act as a single source of reference for the design, simulation, and construction of FETs. We are deeply grateful to all the authors for their great efforts and outstanding input in writing these chapters. We honestly hope that this book will be a guide to young researchers who are interested in researching FETs in the near future. We believe that the book will be a great addition to semiconductor physics.

Dhanasekaran Vikraman and Hyun-Seok Kim
Division of Electronics and Electrical Engineering
Dongguk University-Seoul, South Korea

Section 1

Design and Simulation of FETs

Chapter 1

Modeling of Nano-Transistor Using 14-Nm Technology Node

Soheli Farhana

Additional information is available at the end of the chapter

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Abstract

Latest process technologies in transistor development demonstrate massive changes in the size of transistor chip. In this chapter, a 14-nm technology node is used to model nanosize transistor. The 14-nm technology node consists of multiple numbers of carbon nanotube. Carbon nanotube is a very good energy efficient and low-cost material. Carbon nanotube demonstrates excellent characteristics in metallic and semiconducting characteristics by analyzing electrical properties. At first, the nanotube device physics and material properties are briefly explained in this chapter. Further, a nanotube device is designed for semiconducting properties. The gate length of nanotube is 14 nm which is placed on the gate channel. Finally, the model of 14-nm nano-transistor will be demonstrated for low-energy consumption which can be considered as a better replacement of CMOS.

Keywords: nano-transistor, 14 nm, electrical properties, I-V characteristics, low energy

1. Introduction

Nanoelectronics research is upgrading due to the increases of consumer demand of electronics device in small scale. Nanotechnology research area encourages the researchers to work on nanomaterials as an immerging technology for future. Carbon nanotube (CNT) is a potential material in the field on nanotechnology that has the ability to overcome almost all the limitations of other nanomaterials for its excellent electrical and mechanical properties. Therefore, one of the potential uses of CNT is to place as gate channel of a FET is called carbon nanotube field effect transistor (CNTFET). Silicon-based circuit is moving towards its physical limitation point according to the proven experiment [1]. Due to similar ballistic transport and high career portability of silicon material, CNTFET can be a good replacement of silicon [2] while CNT can

be acted as a semiconducting material [3, 4]. Nanotube is able to show its excellent electrical properties in designing digital devices [5, 6] in small scales. Another special characteristic also to be highlighted for nanotube is I-V features which enable to use the CNT in MOS transistors [7–10]. According to device physics, the performance of the chip can be improved by reducing the size but there is a limitation about the reduction of silicon device size. Nano-hardware, which was created from the 1990s, has turned out to be a standout amongst the most dynamic research subjects in this day and age. The nanoelectronics innovation, which can fundamentally diminish the transistor measure, is particularly alluring to individuals. Single-walled carbon nanotube is mostly used in transistor [11]. Ballistic transport properties of MOS transistor are unchanged while the gate channel Si is substituted by nanotube [12]. In perspective of the outstanding size-lessening issues of traditional Si-based hardware, there have as of late been serious examinations on new advances in light of nano-organized materials which are shaped by sorted-out development and self get-together strategies. CVD process was used in the laboratory to grow nanotube from dielectrophoresis in early ages of its generation [13]. The first CNTFET was fabricated for prototype testing [14] which allows the researchers to work on this promising field of nanotechnology. CNTFET shows good performance in designing logic gates for integrated circuit modeling [15, 16]. Therefore, CNTFET can be a promising research in the near future.

2. Carbon nanotubes properties

2.1. Geometry of carbon nanotubes

A carbon nanotube can be characterized by chiral vector and its length and a vector called the chiral vector. Chiral vector is the sum of the multipliers of the two base vectors, like Eq. (1) [17–20]

$$C_h = m\mathrm{a}_1 + n\mathrm{a}_2 \tag{1}$$

The coordinates of the graphene sheet (m,n) allows finding the chiral vector (C_h) of the nanotube.

The two-dimensional graphene lattice in real space can be created by translating one unit cell by the vectors $\overline{T} = n\overline{a}_1 + m\overline{a}_2$ with integer combinations (n, m), where $\overline{a}_1$ and $\overline{a}_2$ are basis vectors and is shown in **Figure 1**,

$$\begin{aligned} \overline{a}_1 &= a_0\left(\frac{\sqrt{3}}{2}\widehat{x} + \frac{1}{2}\widehat{y}\right) \\ \overline{a}_2 &= a_0\left(\frac{\sqrt{3}}{2}\widehat{x} - \frac{1}{2}\widehat{y}\right) \end{aligned} \tag{2}$$

$a_0 = 3a_{cc}$ is the length of the basis vector, and $a_{cc} \approx 1.42$ Å is the nearest neighbor C-C bonding distance.

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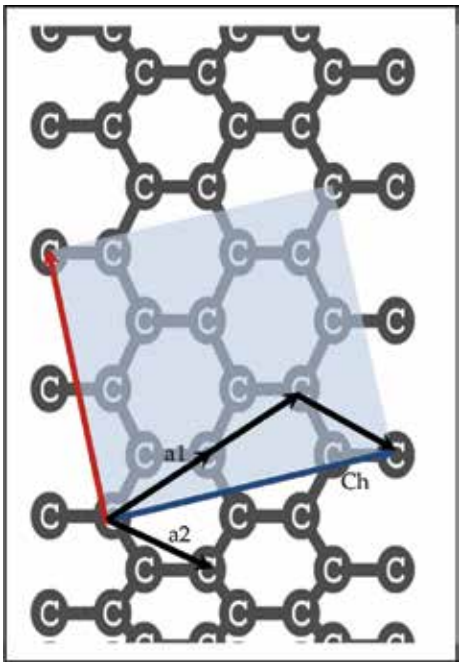

Figure 1. The nanotube unit cell.

To all the more decisively acquire the moment vector T, we can get it from the m, n segments of the C_h vector. On the off-chance that we demonstrate the parts of T with t_1 and t_2, as T is opposite to the C_h, the inward result of these vectors is equivalent to zero and we can conclude Eq. (3)

$$t_1 * a_1 + t_2 * a_2 = 0 \tag{3}$$

The briefest vector t_1 and t_2 that are legitimate as per Eq. (3) can be isolated t_1 and t_2 by their most prominent normal devisor or in short shape most noteworthy basic divisor (gcd), to acquire the briefest nuclear site vector towards the path, opposite to the C_h vector. d_R as in Eq. (4), t_1, t_2 can be accomplished in Eqs. (5) and (6)

$$d_R = \gcd\,(m+n, 2n+m) \tag{4}$$

$$t_1 = \frac{2m+n}{d_R} \tag{5}$$

$$t_2 = \frac{2n+m}{d_R} \tag{6}$$

The angle between the chiral vector and the a_1 base vector is called the chiral angle, the twist angle or the helix angle and is denoted by θ_c and can be obtained in Eq. (7)

$$\theta_c = Arctg\left(\frac{\sqrt{3}m}{2n+m}\right) \tag{7}$$

Here, we should take note of that to consider a one of a kind chiral plot for each nanotube; the point is expressed by an incentive in the locale (0, 30°). Utilizing these definitions, the breadth of the tube can be processed utilizing the balance of the length of the C_h and the nanotube's periphery; lastly, we can acquire the measurement characterized by

$$\mathrm{d_t} = \frac{\mathrm{L}}{\pi} = \frac{\mathrm{a}}{\pi}\sqrt{\mathrm{n^2 + nm + m^2}} \tag{8}$$

The length of the chiral vector is the peripheral length of the nanotube:

$$L = |C_h| = a\sqrt{n^2 + nm + m^2} \tag{9}$$

The bandgap of a single wall nanotube (SWNT) is defined by

$$E_g = 2\gamma_0 a_{cc}/d_t \tag{10}$$

From Eq. (4), if (n-m) is divisible by 3, then nanotube is metallic, otherwise the nanotube is semiconducting.

Now, the number of atom of the nanotube is defined by

$$N_{at} = 4*\frac{n^2 + m^2 + nm}{d_R} \tag{11}$$

2.2. Classification of carbon nanotubes

Carbon nanotube (CNT) is classified into three groups as shown in **Figure 2**: (1) armchair, (2) zigzag and (3) chiral, based on the geometrical arrangements of the graphene during the form tube formation.

If the C_h is defined as $(n, 0)$, it is given the name zigzag nanotube and if the C_h is defined as (n, n), then the tube is called armchair, and these refer to the form shaped on the circumference of the tube.

2.3. Carbon nanotube formation

2.3.1. Armchair tubes

If the chiral indices (m, n) of a nanotube in a zone-folding region can be divisible by 3, then it becomes metallic. These nanotubes are called 'zone folding metallic', or shortly, $Z_{F\text{-}M}$ tubes.

2.3.2. Zigzag tubes (semiconducting tubes with bandgap)

The primary band gap of a nanotube is considered as semiconducting material if the Chirality (m, n) in the zone folding area is not divisible by 3. We should allude to these nanotubes as 'zone collapsing semiconducting', or in a matter of seconds, ZF-S tubes.

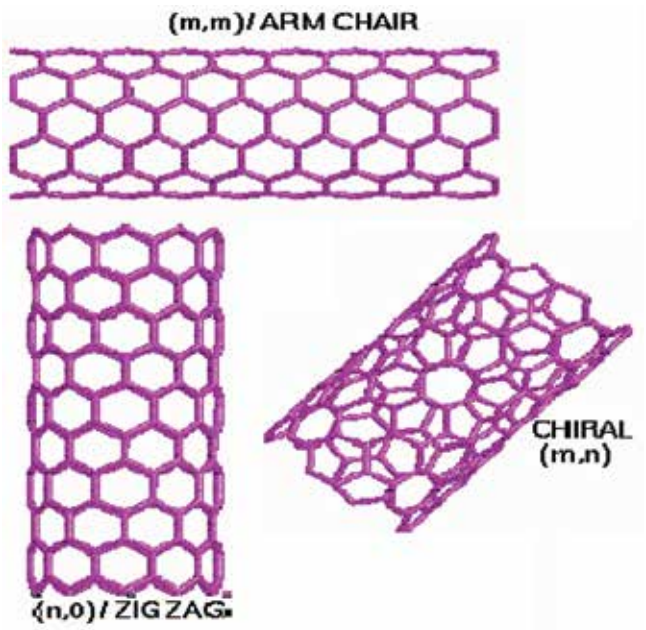

Figure 2. Classifications of different CNTs: (a) armchair, (b) zigzag and (c) chiral (François, 2009).

2.4. Electrical properties

Carbon nanotubes (CNTs) have outstanding electrical properties based on the chirality. There are two types of carbon nanotube, such as single-walled carbon nanotube (SWCNT) and multiple-walled carbon nanotube (MWCNT) based on the requirements of the CNT in the integrated circuit (IC) design [21–23]. **Figure 3** shows the different types of carbon nanotube. A single-walled carbon nanotube has only one shell with a small diameter usually less than 2 nm.

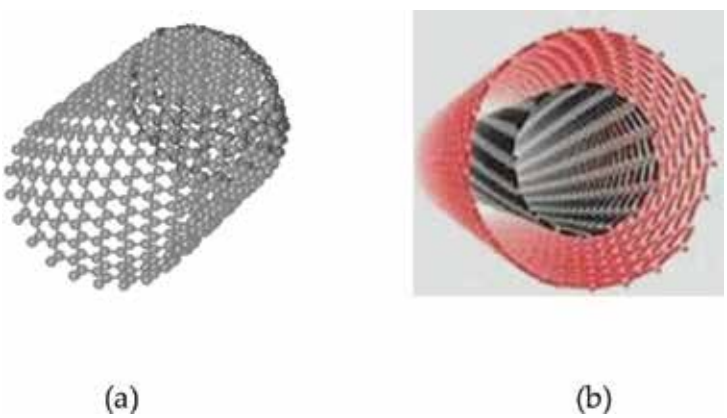

Figure 3. Diagram of carbon nanotube: (a) single-walled and (b) multi-walled (François, 2009).

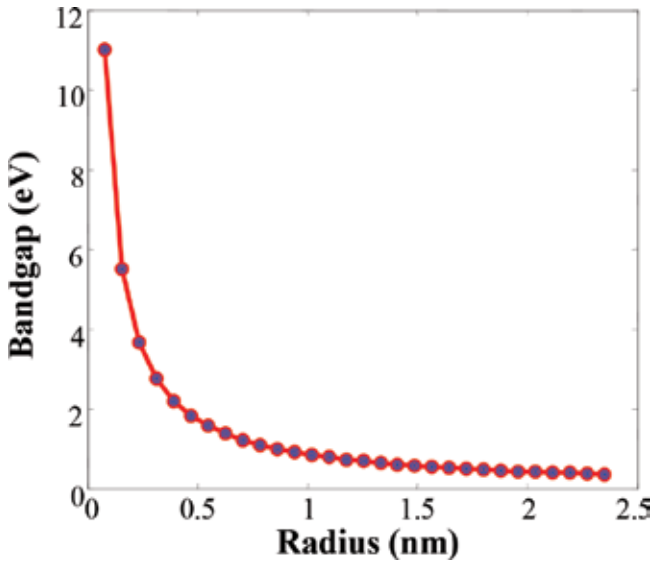

Figure 4. Bandgap versus radius for zigzag nanotube.

As well as multi-walled carbon nanotube consists of two or more concentric cylindrical shells with the diameter of 2–30 nm.

The electrical properties of a nanotube can be realized from its bandgap. Semiconducting nanotube is a novel choice for the transistor development. Thus, **Figure 4** shows bandgap versus radius for semiconducting (zigzag) nanotubes. The bandgap decreases inversely with an increase in diameter. The points with a zero bandgap correspond to metallic nanotubes which satisfy n = 3i, where i is an integer.

3. Modeling process of 14-nm CNTFET

This research consists of the design and verification of the CNTFET device's small signal model. **Figure 5** shows a solid model of CNTFET with a built-in circuit model in this work.

3.1. CNTFET biasing

Three different types of biasing structure are seen in the CNTFET device. They are common-drain, common-gate and common-source structure. Common-source transistor circuit is considered in this modeling. The common-source circuit is shown in **Figure 6**; the DC shows bias on drain and gate with an AC signal present as the input at the gate.

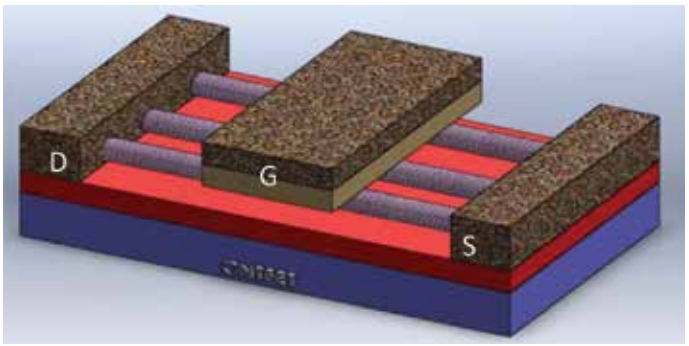

Figure 5. Perspective view of the CNTFET 3D solid model.

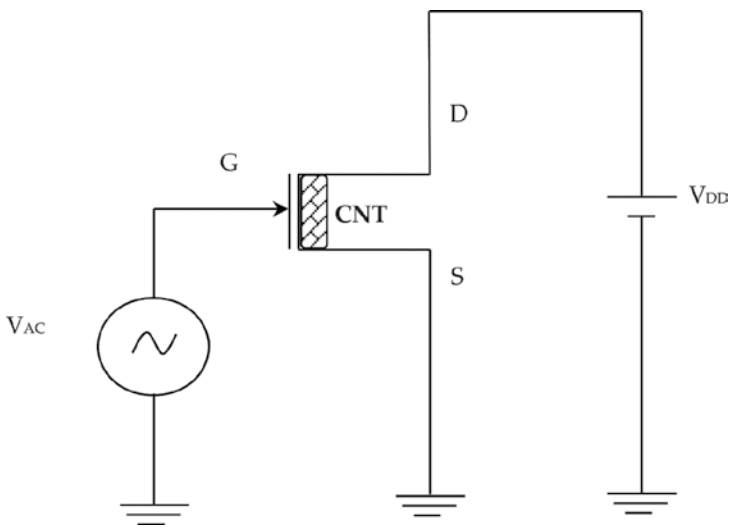

Figure 6. Common-source biasing circuit.

3.2. CNTFET small signal model

This section describes about the design and analysis of the small signal model circuit for CNTFET. The proposed small signal model of a CNTFET is shown in **Figure 7**. In **Figure 7**, $C_{g\text{-}CNTS}$ refers to the capacitance between gate electrodes to source, $C_{g\text{-}CNTD}$ refers to the capacitance between gate electrodes to drain, $C_{g\text{-}CNTS}$ refers to the capacitance between gate electrodes to source, and Ri represents the internal resistance. Furthermore, g_m refers to the intrinsic transconductance and g_d refers to the drain conductance of the circuit as shown in **Figure 7**. In this circuit, the parasitic elements are excluded for the analysis purpose.

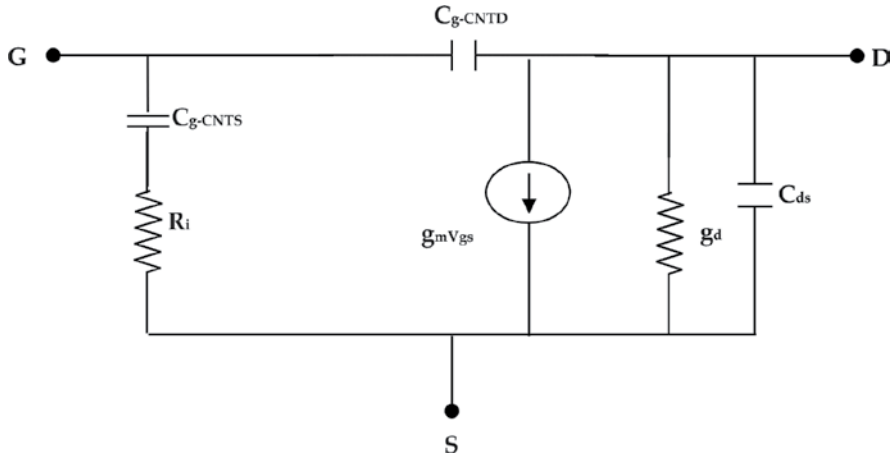

Figure 7. Intrinsic circuit model for CNTFET.

4. Analysis of CNTFET model

4.1. Transconductance of CNTFET SPICE model

Figure 8(a) and **(b)** shows the simulation results of frequency versus transconductance while the transconductance is increased linearly. This is as a result with μS through the stage of the lower frequency as well as mS through the stage of increasing frequency. Therefore, high-frequency small signal model of CNTFET is obtained in 10 THz with 1.8 mS. On analyzing the data, we first calculate and simulate the transconductance value in μS and in mS.

Figure 8(a) shows the plot for the value of transconductance in μS and **Figure 8(b)** shows the plot for the value of transconductance in mS.

Tables 1 and **2** show the selected values of transconductance necessary for the small signal model obtained from the analysis of the model as shown in **Figure 8(a)** and **(b)**. By comparing the two tables, transconductance in mS performs the higher frequency rather than to use in μS. Therefore, we consider transconductance in mS in this research.

4.2. I-V characteristics of CNTFET

The proposed CNTFET circuit model is implemented in PSpice. A CNTFET DC characteristic is analyzed and simulated to check the output characteristics. Modeling of CNTFET with the I-V characteristics analysis is obtained from the channel length of 14 nm and width of two times the length of the proposed CNTFET. The I-V characteristic curves validate the proposed circuit model by getting drain current of 6.9×10^5 A at the applied gate voltage of 0.4 V as shown in **Figure 9**.

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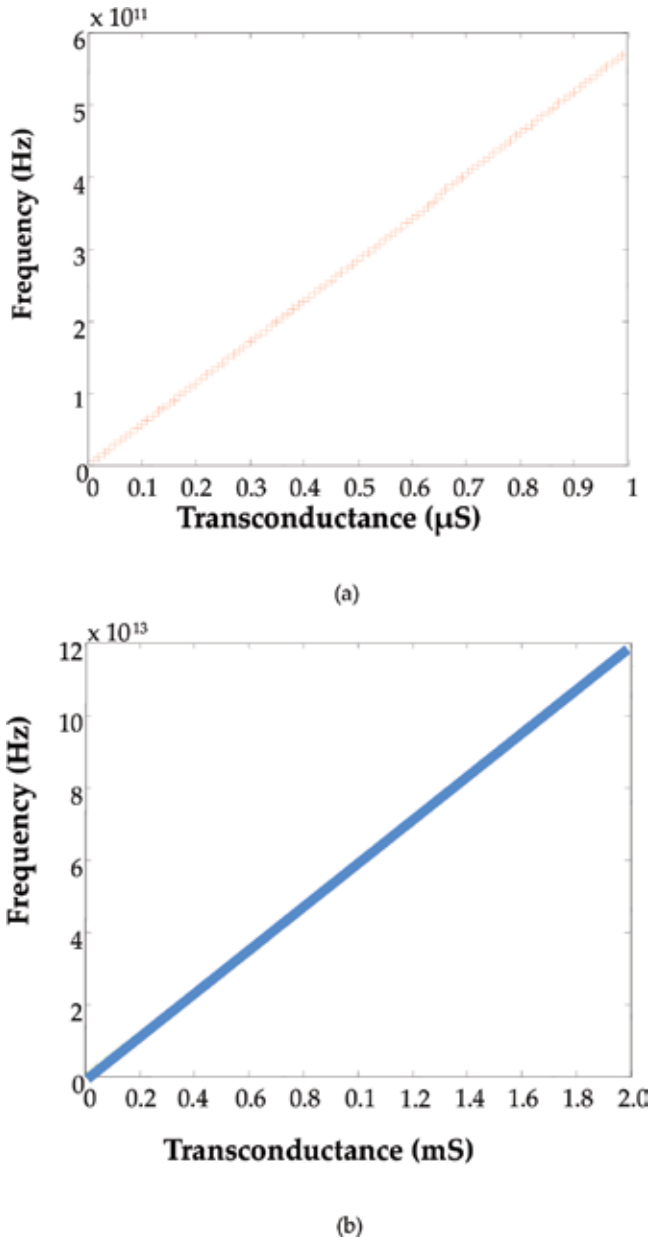

Figure 8. Simulation of frequency, fT, versus transconductance, gm: (a) transconductance in μS and (b) transconductance in mS.

4.3. Frequency response of CNTFET

The current gain of the proposed CNTFET is shown in **Figure 10**. Current gain magnitude is found in 45 dB while the frequency is operated in 10 THz. The value of the CNTFET's

Gm (μS)	F_T (Hz)
19	1.0800×10^{11}
22	1.2505×10^{11}
28	1.5915×10^{11}
32	1.8189×10^{11}
36	2.0463×10^{11}
45	2.5578×10^{11}
50	2.8421×10^{11}
55	3.1263×10^{11}
60	3.4105×10^{11}

Table 1. Frequencies for different current gain of small signal model while transconductance in μS.

Gm (mS)	F_T (Hz)
1.0	5.68×10^{12}
1.1	6.25×10^{12}
1.2	6.82×10^{12}
1.3	7.39×10^{12}
1.5	8.52×10^{12}
1.6	9.00×10^{12}
1.7	9.66×10^{12}
1.8	10.00×10^{12}

Table 2. Frequencies for different current gain of small signal model while transconductance in mS.

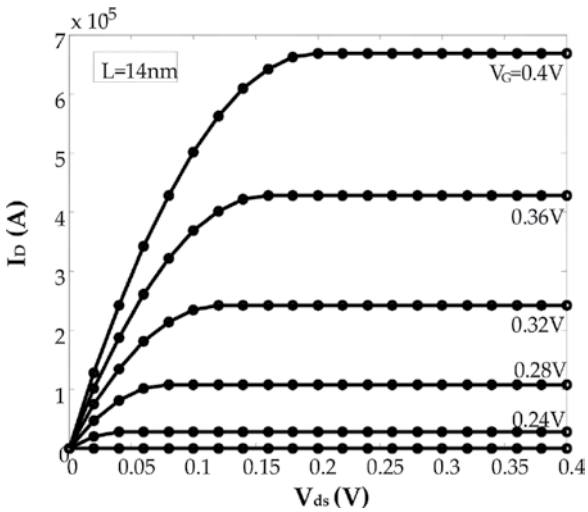

Figure 9. I-V transfer characteristics of CNTFET.

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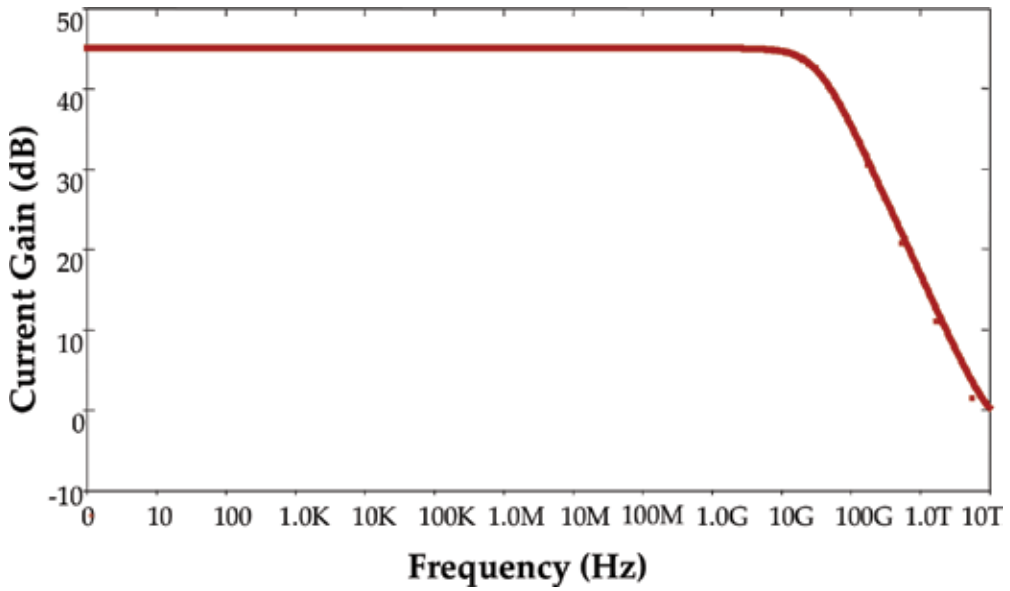

Figure 10. Output current gain of the CNTFET at 10-THz frequency.

Device Parameters	CNTFET [25]	This Research
Current gain (db)	20	45
g_m (mS)	3.8	1.8
C_{gs} (F)	65f	14a
C_{gd} (F)	52f	14a
Cut-off-Freq (Hz)	30G	10T

Table 3. Comparison of current research.

transconductance gm is set as 1.8 mS from the analysis as shown in **Figure 10** at the gate voltage of 0.4 V [24].

To validate the output characteristics of the current development of proposed CNTFET, we compare the work with other researches. **Table 3** shows the comparison of the performance of the proposed model. From this performance comparison, we would like to conclude that the proposed CNTFET model is capable of operating in high frequency.

5. Conclusion

This chapter discussed the development of the CNTFET model using 14-nm technology. We delineated a short examination of the proposed plan of CNTFET little banner show. The arrangement contains a suitable blueprint of the little banner procedure and demonstrated the displays by re-enacting little banner parameters for CNTFET with respect to that of 45 dB.

The inherent capacitance of 14 aF and transconductance of 1.8 mS are used as a piece of this examination. A benchmark is showed up for the immense execution of the exhibit made by differentiating and late research data. Particular characteristics are showed up by a course of action of multiplication. Besides, this system has familiar capacitance with survey, the charge defending capacitance at the repeat of 10 THz.

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Conflict of interest

There is no conflict of interest with this publication.

Author details

Soheli Farhana

Address all correspondence to: soheli.farhana@live.iium.edu.my

International Islamic University Malaysia, Kuala Lumpur, Malaysia

References

[1] Sinha S, Balijepalli A, Cao Y. Compact model of carbon nanotube transistor and interconnect. IEEE Transactions on Electron Devices. 2009 Oct;**56**(10):2232-2242

[2] Li H, Xu C, Srivastava N, Banerjee K. Carbon nanomaterials for next-generation interconnects and passives: Physics, status, and prospects. IEEE Transactions on Electron Devices. 2009 Sep;**56**(9):1799-821

[3] Javey A, Wang Q, Ural A, Li Y, Dai H. Carbon nanotube transistors arrays for multistage complementary logic and ring oscillators. Nano Letters. 2002;**2**:929-932

[4] Guo J, Javey A, Dai H, Lundstrom M. Performance analysis and design optimization of near ballistic carbon nanotube FETs. IEDM Technical Digest. 2004:703-706

[5] Bagherizadeh M, Eshghi M. Two novel low-power and high-speed dynamic carbon nanotube full-adder cells. Nanoscale Research Letters. 2011;**6**:519

[6] Maehashi K, Kishimoto T, Ohno Y, Inoue K, Matsumoto K. Fabrication of high-performance voltage inverters based on carbon nanotube field-effect transistors. In: IEEE Nanotechnology Materials and Devices Conference; 2010

[7] Das S, Bhattacharya S, Das D. Modeling of carbon nanotube based device and interconnect using VERILOG-AMS. In: Proceedings of the International Conference on Advances in Recent Technologies in Communication and Computing. 2011. pp. 51-55

[8] Das S, Bhattacharya S, Das D. Design of digital logic circuits using carbon nanotube field effect transistors. International Journal of Soft Computing and Engineering. 2011 Dec;**1**(6): 173-178

[9] Das S, Bhattacharya S, Das D. Design of transmission gate logic circuits using carbon nanotube field effect transistors. In: Proceedings of the National conference on Advanced Communication Systems and Design Techniques. 2011. pp. 75-78

[10] Das S, Bhattacharya S, Das D. Performance evaluation of CNTFET-based logic gates using Verilog-AMS. In: Proceedings of the National Conference on Electronics, Communication and Signal Processing. 2011. pp. 85-88

[11] Koo Y, Littlejohn G, Collins B, Yun Y, Shanov VN, Schulz M, et al. Synthesis and characterization of Ag–TiO2–CNT nanoparticle composites with high photocatalytic activity under artificial light. Composites Part B: Engineering. 2014;**57**:105-111

[12] Hoque M, Ahmad H, Reza A. Design optimization of high frequency Op Amp using 32 nm CNFET. In: 6th International Conference on Electrical and Computer Engineering ICECE; 2010

[13] Kim S, Wang C, Shim M, Mohammadi S. Comparison of single-walled carbon nanotube transistors fabricated by dielectrophoresis and CVD growth. In: Proceedings of 5th IEEE Conference on Nanotechnology. Nagoya, Japan; 2005

[14] Kim Y. Integrated circuit design based on carbon nanotube field effect transistor. Transactions on Electrical and Electronic Materials. 2011;**12**(5):175-188

[15] Hameem Shanavas I, Brindha M, Nallusamy V. An analogous computation of different techniques for the digital implementation of inverter and NAND logic gates. International Journal of Information Engineering and Electronic Business. 2012;**4**(4):33-38

[16] Zhang X, Luo D, Cui G, Wang Y, Huang B. Construction of logic gate based on multi-channel carbon nanotube field-effect transistors. In: Intelligent Human-Machine Systems and Cybernetics (IHMSC), International Conference; 2011. IEEE; August, 2011. Vol. 2, pp. 94-97

[17] Farhana S, Alam AHMZ. Carbon nanotubes: A review on future generation Nano device. Middle-East Journal of Scientific Research. 2014;**20**(1):74-81

[18] Farhana S. Novel carbon nanotube model for low energy loss field-effect transistor. Cogent Engineering. 2017;**4**(1):1300082

[19] Farhana S, Alam AHMZ. Modeling and simulation of CNTFET small signal model. In: 2014 IEEE 6th International Nanoelectronics Conference (INEC); 28-31 July 2014; Hokkaido, Japan. 2014. http://irep.iium.edu.my/39069/

[20] Farhana S, Alam AHMZ, Khan S. DIBL and subthreshold swing effect on carbon nanotube field effect transistor. In: Proceedings of the World Congress on Engineering. 2015. Vol. 1, pp. 455-458

[21] Gokturk HS. Electrical properties of ideal carbon nanotubes. In: Nanotechnology. 5th IEEE Conference; 2005. IEEE; July, 2005. pp. 677-680

[22] Krompiewski S. Electronic transport through side-contacted graphene nanoribbons: Effects of overlap, aspect ratio and orientation. Nanotechnology. 2011;**22**(44):445201

[23] Sanudin R. Characterisation of ballistic carbon nanotube field-effect transistor [doctoral dissertation]. Malaysia: Universiti Teknologi; 2005

[24] Farhana S, Alam AZ, Khan S. Small band-gap-based CNT for modeling of nano sensor. Procedia Computer Science. 2014;**42**:122-129

[25] Coskun K, Simon D, Qing C, Kurt C, Xinning H, Hoon-Sik K, Dawson D, Payne J, Stuenkel M, Zhang H, Banks T, Feng M, Rotkin SV, Rogers JA. High-frequency performance of submicrometer transistors that use aligned arrays of single-walled carbon nanotubes. Nano Letters. 2009;**9**(5):1937-1943

Chapter 2

Dielectric-Modulated TFETs as Label-Free Biosensors

Rupam Goswami and Brinda Bhowmick

Additional information is available at the end of the chapter

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Abstract

This chapter presents tunnel field effect transistors (TFETs) as dielectric-modulated (DM) label-free biosensors, and discusses various aspects related to them. A brief survey of the dielectric-modulated TFET biosensors is presented. The concept of dielectric modulation in TFETs is discussed with focus on principle and design perspectives. A Technology Computer Aided Design (TCAD) based approach to incorporate embedded nanogaps in TFET geometries along with appropriate physics-based simulation models are mentioned. Non-ideal conditions in dielectric-modulated biosensors are brought to light, keeping in view the practical considerations of the devices. A gate engineered TFET is taken up for analysis of sensitivities under different conditions through TCAD simulations. Finally, a status map of the sensitivities of the most significant works in dielectric-modulated label-free biosensors is depicted, and the status of the proposed TFET is highlighted.

Keywords: TFET, biosensor, dielectric modulation, biomolecules, sensitivity

1. Introduction

The dependence of economics of the semiconductor industry on Moore's Law led to the downscaling of device dimensions in metal oxide semiconductor field effect transistors (MOSFETs) in order to accommodate more transistors in the same chip area. As the device dimensions were scaled down to the nanometer regime, degradation in the performance of MOSFETs in the form of short channel effects (SCEs) was observed. The inversion charge sharing by the source and drain regions in short channel MOSFETs led to problems of drain induced barrier lowering (DIBL), threshold voltage roll-off, mobility degradation and high field saturation [1–3]. These problems hindered the progress of MOSFETs towards low power applications which required reduced supply voltage and targets of low off currents. Since

then, the semiconductor industry has been on the lookout for novel devices which can effectively address the issues of scaling and depict performance which is superior to MOSFETs.

Over the past few decades, industries and researchers have proposed a number of devices as prominent alternatives to MOSFETs for low power applications. Most of these devices possess principles of operation which are different from MOSFETs. The International Technology Roadmap for Semiconductors in its document 'Beyond CMOS' published in 2015 reported the emerging devices based on structure or materials and charge/non-charge entity [4]. This include a number of devices like nanowire FET [5–7], carbon nanotube FET [8–10], graphene FET [11–13], TFET [14–16], spin FET [17–19] and negative gate capacitance FET [20, 21]. Of these devices, TFETs have gained concentrated focus for low power applications due to their fundamental fabrication methodologies being similar to MOSFETs, and their ability to achieve sub-60 mV/dec subthreshold swing and lower off currents than MOSFETs. TFETs operate by interband tunneling mechanism unlike thermionic emission in MOSFETs due to which the high energy tails of the Fermi distribution of carriers while moving from source to drain get curtailed, resulting in low subthreshold swings and off currents. Different architectures of TFETs have been proposed till date to improve their performance and increase the on currents. [22, 23], nanowire TFET [24, 25], heterojunction TFET [26, 27], III-V TFET [28], triple material gate TFET [29, 30], cylindrical TFET [31] and SOI TFET [32] are some of the widely used structures.

TFETs have found their uses in a wide range of low power applications like digital circuits and memory applications [33–35]. However, recently, the emergence of FET-based biosensors has projected TFETs as biosensors based on dielectric modulation in which the dielectric constant along with the charge of the biomolecules in the gate dielectric region affect the drain current [36]. The sensitivity of the biosensor in presence of biomolecules is defined with respect to a reference value. A number of geometries of TFETs has been proposed as dielectric-modulated biosensors, and the analyses of their sensitivities having dependence on device parameters have been reported [37–41].

Section 2 of this chapter presents a brief report on the existing works on FET-based biosensors. In Section 3, the principle of dielectric modulation in TFETs and a reference architecture for TFETs as biosensors are discussed. Section 4 mentions the different physics-based models to be considered while simulating a TFET on a Technology Computer Aided Design (TCAD) tool. The different sensitivities are defined in Section 5. Section 6 mentions the various non-ideal conditions that may possibly exist in case of FET-based biosensors. A circular gate TFET is analyzed as a dielectric-modulated biosensor through TCAD simulation in Section 7. Section 8 concludes the chapter and comments on future scope.

2. A brief survey

The compactness, compatibility in fabrication and label-free detection have made FET-based biosensors one of the promising area of interests. Generally, there are two methods to detect the presence of biomolecules: gating effect and dielectric modulation. The gating effect uses

the gate dielectric material with receptors on its surface to immobilize the biomolecules [42]. Dielectric modulation, on the other hand, employs the effect of change in dielectric constant in a portion of the gate dielectric on the drain current and the associated electrical parameters [37–41]. The gating effect is effective for detecting charged biomolecules, while dielectric modulation can assist in sensing charged and neutral biomolecules.

Im et al. proposed a dielectric-modulated (DM) FET-based biosensor [36] after the ion sensitive FETs proposed in 1970s [43]. Sarkar and Banerjee presented a nanowire TFET in [42] demonstrating the gating effect for positively charged biomolecules. It is convenient to assume that the embedded nanogap is completely filled with biomolecules. However, Kim et al. reported on partially filled nanogaps in practical cases due to steric hindrance, and proposed a parameter, fill factor, defined as the percentage of the nanogap occupied by biomolecules [44]. Narang et al. provided similar simulation analyses for partially filled nanogaps for DM FET and PNPN TFET [11]. Narang et al. further presented a Poisson equation based analytical model to account for the effect of dielectric modulation in TFETs [38]. Partially filled nanogaps decrease the response of the biosensor, as the effective dielectric constant varies with position within the nanogap. Abdi and Kumar proposed the concept of deriving the sensitivity through ambipolar current in TFET [45]. Ahangari presented reports of a dual material gate nanowire junctionless TFET as a biosensor [46]. As the nanogap length increased, the sensitivity improved considerably. Kanungo et al. reported that a short gate dielectric-modulated TFET biosensor showed improved sensitivity than a full gate dielectric-modulated TFET [40].

3. Dielectric modulation in TFETs: concept and geometry

3.1. Principle of operation

A conventional homojunction TFET is a gated reverse-biased p-i-n structure [3]. As opposed to the thermionic emission in MOSFETs, the mechanism of transport in TFETs is band-to-band tunneling. In an n-TFET, when positive gate bias increases, the energy bands get suppressed as a result of which the width between the p + source valence band, and i-channel conduction bands reduces, thus facilitating the tunneling of electrons from the former to the latter as depicted in **Figure 1** [3]. This contributes to the drain current.

The tunnel barrier at the source-channel junction is modeled as a triangular barrier, and using WKB approximation, its tunneling probability is calculated as [47].

$$T(E) = exp\left(-\frac{4\lambda\sqrt{2\,m^*\,E_G^{3/2}}}{3q\hbar\left(\Delta\Phi + E_G\right)}\right) \tag{1}$$

where m* is the effective mass, E_G is the energy band gap at the source-channel tunnel junction, $\Delta\Phi$ is the energy overlap of the bands at tunnel junction, λ is the screening tunneling length, q is the electronic charge, and $\hbar$ is the reduced Planck's constant. The screening length λ is defined as [47].

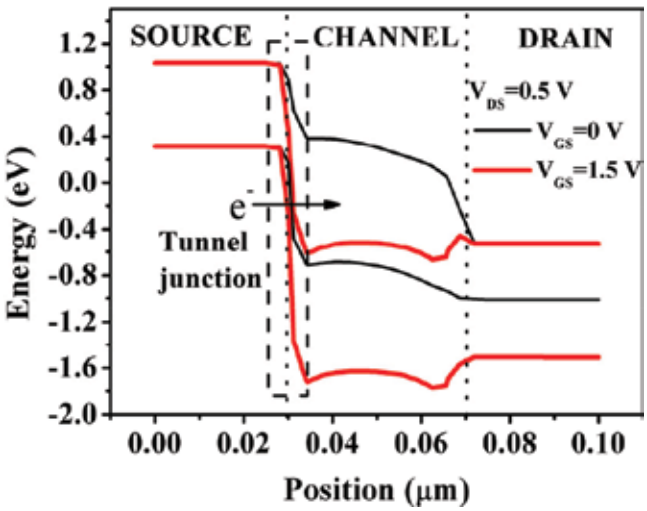

Figure 1. Energy band diagram of a p-i-n TFET showing the on and off states.

$$\lambda = \sqrt{\left(\varepsilon_s / \varepsilon_{ox}\right) t_s t_{ox}} \tag{2}$$

The dielectric modulation in a MOS-based device, and particularly TFETs is the alteration in the dielectric constant in the gate dielectric region of the device. Keeping other parameters constant, the effect of dielectric modulation in TFET is best explained by the parameters, λ and $\Delta\Phi$. A low dielectric constant decreases the gate-to-channel coupling as a result of which the tunnel width is more even at high gate voltages, as compared to the presence of higher gate dielectric constants at the tunnel junction [3, 47, 48]. This results in a low tunneling probability, and hence, low tunneling current. Lesser the gate-to-channel coupling, lesser is the amount of $\Delta\Phi$ at the tunnel junction.

A 2-D Poisson's equation based model of TFET results in a closed form equation of drain current as [49].

$$I_{DS} = W T_{Si,eff} \frac{E_G}{W_{t,min}^2} \cdot \frac{A_K}{B_K} . exp\left(-\frac{B_K E_G}{q W_{t,min}}\right) \tag{3}$$

where, W is the width of the device, $T_{Si,eff}$ is the effective Silicon body thickness, E_G is the band gap of the semiconductor, $W_{t,min}$ is the minimum tunneling width, A_K and B_K are material dependent constants. Equation (3) suggests the dependence of drain current on the minimum tunnel width which, in turn, is dependent on the dielectric constant of the gate insulator region near the tunnel junction. Therefore, as dielectric constant of the nanogap increases, $W_{T,min}$ decreases, and drain current increases.

Another prospect of utilizing dielectric modulation for biosensing is by placing the embedded nanogap towards the channel-drain junction of the TFET, and exploit its ambipolarity [45]. For a conventional n-TFET, when the drain voltage is positive, and gate voltage is negative,

the energy bands at the channel-drain junction get influenced so as to form a tunneling barrier. This results in flow of current by tunneling at this junction. This becomes the reason for anomalies in complementary TFET digital circuits. However, as far as label-free biosensing is concerned, this ambipolar current can be considered as a measure of sensitivity in TFETs.

3.2. Geometry

As evident from Section 3.1, the objective of utilizing dielectric modulation for biosensing requires a modified geometry with the following basic requirements

- The biomolecules must be immobilized in the gate dielectric region. To realize this, a nanogap is required in the gate dielectric. The gate dielectric, therefore, is composed of two regions; apparently, it works like a dual gate dielectric device, where one gate dielectric has a fixed dielectric constant, and the other carries the dielectric constant of the biomolecules.
- The height of the embedded nanogap must be large enough to allow the entry of biomolecules into the cavity or nanogap. A minimum height of 10–11 nm is usually considered for simulation analyses in nanoscale TFETs.
- In order to accommodate more biomolecules, a double gate structure with the above designs may be employed.
- The TFETs must have appropriate source doping. A few biomolecules have dielectric constants of 2 or 3 [39–42], which is closer to the dielectric constant of 1. So, the geometry must be so designed that it is able to respond to immobilization of biomolecules having low dielectric constants as well.
- For TFETs which utilize the ambipolar behavior of the devices, the drain doping concentration is more important.

4. Simulation strategy for a DM TFET as a label-free biosensor

The most convenient way to analyze a biosensor is on a computational platform where the physics-based models applied to the architecture assist in analyzing its performance. There are a number of industrial simulators and most of them come equipped with provisions for defining a geometry and feeding it through iterations of selective models available in their libraries.

The embedded nanogap in a DM TFET is designed by substituting that region in the gate dielectric with a dielectric material (oxide) whose dielectric constant can be altered as per requirement [38]. For charged biomolecules, the charges are considered at the oxide-semiconductor interface. By varying the dielectric constant and the charge, the immobilization of biomolecules may be mimicked appropriately.

The models for TFETs must be chosen with care. Since TFETs usually have high source doping concentration to achieve large band bending at equilibrium, therefore, Fermi-Dirac statistics

is necessary [50]. Bandgap narrowing is important for heavily doped geometries [50]. Nonlocal band-to-band tunneling models are essential to create a suitable simulation environment for the device whose principle of operation is interband tunneling [50]. Field dependent mobility models may be used [50].

5. Sensitivity parameters

The performance of a TFET or any MOS-based device is reflected through its electrical parameters. The most commonly used parameters for defining sensitivity are the drain current and threshold voltage. Subthreshold swing (SS) may also be considered for defining a sensitivity parameter; however, the measurement of SS is dependent on the orders of the logarithmic scale over which the drain current is measured. This value or the measurement may not be consistent as the drain current changes with the variation in the dielectric constant of the immobilized biomolecules. Sensitivities are usually defined with respect to reference values. The reference value in case of a dielectric-modulated biosensor is considered when the nanogap is devoid of biomolecules, and hence, is assumed to be filled with air with a dielectric constant of 1 without any charges at the oxide-semiconductor interface. The drain current based sensitivity is mathematically expressed as [44].

$$Sensitivity,\ S_I = \left.\frac{I_{D,k}}{I_{D,k=1}}\right|_{V_{GS}} \tag{4}$$

where $I_{D,k}$ and $I_{D,k=1}$ are the values of drain currents when the nanogap is filled with biomolecules and the nanogap is unfilled. The values must be measured at the same gate voltage so as to get a justified value of sensitivity.

The threshold voltage has a dependence on the dielectric constant of the gate dielectric and charge at the semiconductor-oxide interface. The shift in threshold voltage with the immobilization of biomolecules with different dielectric constants may be taken up as a sensitivity parameter. It is mathematically expressed as

$$Sensitivity,\ S_{V_T} = V_{T,k=1} - V_{T,k} \tag{5}$$

where $V_{T,k}$ and $V_{T,k=1}$ are the threshold voltages for the cases when the nanogap is filled with biomolecules and when the nanogap is completely unfilled.

There are many threshold voltage extraction methods for MOSFETs, and TFETs. Of them, the Linear Extrapolation (LE) Method is the most widely used [51, 52]. According to this extraction principle, the intercept on the gate voltage axis made by the tangent to the drain current curve corresponding to the maximum value of $g_m = dI_D/dV_{GS}$ is defined as the threshold voltage. Although this extraction method may result in change in threshold voltage with change in range in gate voltage, however, we have considered a fixed range of gate voltage in all the cases of comparison. So, we have used this method of threshold voltage extraction from simulation transfer characteristics.

6. Non-idealities in dielectric-modulated biosensors

While simulating a geometry of a DM TFET as on a TCAD tool to assess its biosensing capacity, it is convenient to assume that the nanocavity is completely filled with the biomolecules. However, in practical cases, the issues of steric hindrance and probe placement do not allow the embedded nanogap to be completely filled [39]. As a result, partially filled nanogaps are formed.

6.1. Steric hindrance

In case of steric hindrance, the biomolecules which get immobilized first prevent the further entry of biomolecules. In fact, there is a hindrance to the biomolecules which are likely to get immobilized in the nanogaps, resulting in partial hybridization. In order to account for this on a TCAD tool for simulation, different patterns of immobilization inside the nanogap are assumed, like increasing, decreasing, concave and convex profiles of placement [39]. As explained in Section 2, this can be designed by defining different heights of gate dielectric material mimicking the biomolecules according to the profile of biomolecules.

6.2. Probe placement

In order to immobilize the biomolecules, probes or receptors are used in the nanogap. The placement of probes in the nanogap for immobilization of biomolecules may not be continuous throughout, and this may result in partially filled nanogaps [39]. For simulation, this may be considered in a similar manner as the steric hindrance except that the profiles shall not be continuous as in steric hindrance.

6.3. Fabrication issues

The nanogap which is formed in a DM biosensor is carved out by forming a native oxide first, and then etching out the native oxide [38]. This method, however, is challenging, and practically, there is possibility that damages result from the process. These anomalies include creation of trap centers at the interface or incomplete etch of the native oxide along with traps in the residual gate dielectric [38]. The phenomenon of tunneling in a TFET is highly dependent on its source-channel tunnel junction, and the alignment of the gate with the junction. During fabrication, the gate edge may be displaced from the junction. This may result in an overlap or an underlap depending on whether the gate shifts towards the source or the channel respectively. In case of a gate-source overlap, the characteristics of the TFET generally improve as the shifted gate can now influence the energy bands in the source-channel junction with better control. However, in case of an underlap, the gate edge moves away from the junction, and the tunnel junction is least affected by it.

7. A circular gate TFET as a DM biosensor

This section presents a geometry of TFET, a Circular Gate TFET (CG) as a dielectric-modulated biosensor, and discusses some of the results. The CG TFET has a non-uniform gate in the

form of a semi-circle. This gate engineering introduces flexibility into the architecture of the device, and aids in optimization of chief electrical parameters, primarily the ambipolar current and ratio of on and off currents [53]. One of the techniques of reducing ambipolar current in a TFET apart from asymmetric source-drain doping is the introduction of gate-drain underlap [3, 45, 53]. In case of Circular Gate TFET, the gate being circular in shape, the gate dielectric thickness is dependent on the radius of the circle. A gate-drain underlap in the architecture shall decrease the thickness of the gate dielectric, which shall, in turn, increase the influence of the gate on the channel. Therefore, reduced ambipolar current can be achieved with appropriate ratio of on and off current simultaneously.

A circular gate TFET as a DM biosensor is depicted in **Figure 2a**. The total length of the Silicon body TFET is 100 nm, where the source and drain are 30 nm each. An embedded nanogap is incorporated into the geometry to immobilize the biomolecules. The embedded nanogap is usually etched out of a dielectric formed by a native oxide. We have considered a native oxide of 1 nm in the nanogap, which is assumed to remain after the gap is etched out.

7.1. Fully filled nanogap

Firstly, we assume that the entire embedded nanogap of the CG TFET in **Figure 2b** is filled with biomolecules, and observe the influence of different factors on its sensitivity. The Fill Factor of an embedded nanogap is defined as the ratio of the area covered by immobilized biomolecules to the total area of the nanogap, and is generally expressed in percentage. For a fully filled nanogap, the Fill Factor is 100%.

7.1.1. Negatively charged biomolecules

The sensitivity of the CG TFET as a biosensor with fully filled nanogap is plotted for negative charge of biomolecules for k = 5, 7, 10 and 12 in **Figure 3a**. With the increase in magnitude of negative charge, the sensitivity decreases. The presence of negatively charged biomolecule-SiO_2 interface prevents depletion of the p-type channel, thus requiring a higher gate voltage than a neutral interface to deplete the p-type substrate, and cause reduction in tunnel width. The voltage balance equation of a metal-oxide-semiconductor structure is represented as [54].

$$V_G = \psi_s + \Phi_{MS} - \frac{q N_{bio}}{C'_{ox}} \tag{6}$$

where, V_G is the gate voltage, Ψ_s is the electrostatic potential at the surface, Φ_{MS} is the difference between the work functions of metal and semiconductor, q is the value of electronic charge, N_{bio} denotes the number of charges per unit area, and C'_{ox} is resultant capacitance per unit area. Furthermore,

$$C'_{ox} = \frac{k}{t_{ox}(x)} \tag{7}$$

where k is the dielectric constant, and $t_{ox}(x)$ is the dielectric thickness as a function of lateral position due to the circular gate.

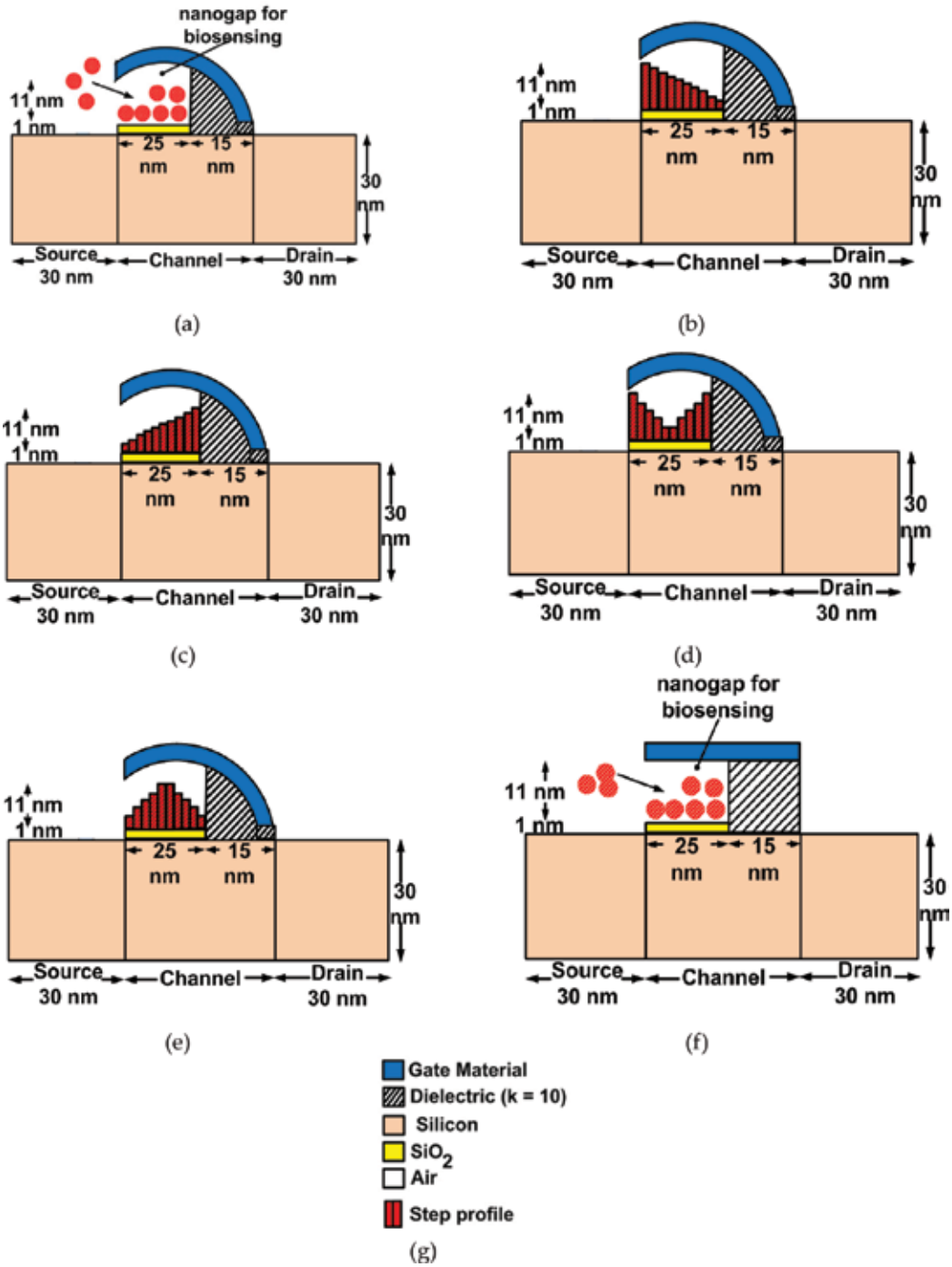

Figure 2. 2-D schematic of dielectric-modulated biosensors: (a) CG TFET, (b) decreasing step profile of biomolecules, (c) increasing step profile of biomolecules, (d) concave step profile of biomolecules, (e) convex step profile of biomolecules, (f) MOSFET, and (g) legend for all the 2D schematics.

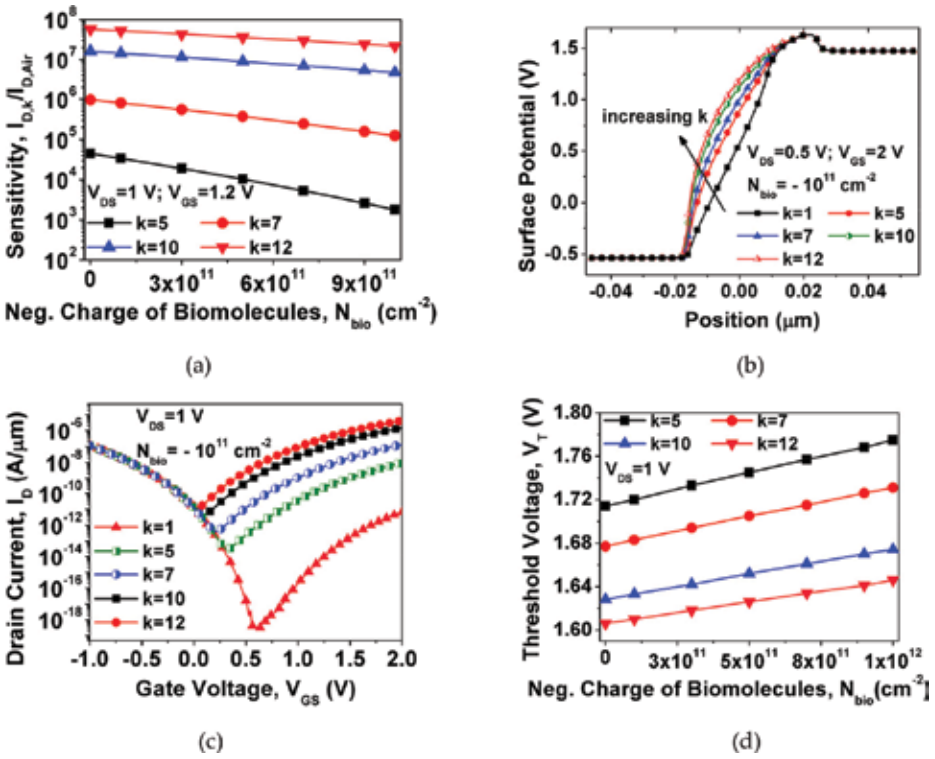

Figure 3. (a) Sensitivity versus negative charge of biomolecules for dielectric constant, k = 5, 7, 10 and 12; (b) surface potential versus position from source to drain at gate voltage 2 V, drain voltage 0.5 V, and $N_{bio} = -10^{11}$ cm^{-2} for dielectric constant, k = 1, 5, 7, 10 and 12; (c) transfer characteristics of CG TFET as biosensor for k = 1 (air), 5, 7, 10 and 12 at fixed negative charge, $N_{bio} = -10^{11}$ cm^{-2}; (d) threshold voltage versus negative charge of biomolecules for dielectric constant, k = 5, 7, 10 and 12.

Considering a fixed gate voltage, as the negative charge of biomolecules increases, Ψ_s must decrease in order to satisfy the potential balance in Eq. (6). As a result, the drain current decreases, thus reducing the sensitivity.

The change in sensitivity of the sensor with increasing magnitude of negative charge is more in case of a low dielectric constant and reduces as the dielectric constant of the nanogap increases. At k = 5, the sensitivity decreases by a factor of 25 when the charge of the immobilized biomolecules changes from neutral to -10^{12} cm^{-2} as compared to k = 12, where it drops by 2.61. In Eq. (6), at fixed negative N_{bio} and V_{GS}, as k in Eq. (7) increases, the potential $-\frac{q N_{bio}}{C'_{ox}}$ decreases, resulting in a corresponding increase in Ψ_s. This increases the drain current, and hence, the sensitivity of the biosensor. This effect is demonstrated in **Figure 3b**.

Figure 3c shows the plots of transfer characteristics of a fully filled nanogap CG TFET biosensor at drain voltage 1 V and charge of biomolecules equal to -10^{11} cm^{-2}. The absence of biomolecules corresponds to k = 1 with no charge at the air-SiO_2 interface as the nanogap remains devoid of biomolecules. Due to the presence of unaltered gate dielectric towards the channel-drain junction of the geometry, therefore, the ambipolar current is same for all dielectric constants of the nanogap. The dielectric constant of the fully filled nanogap closer to the

source-channel tunnel junction has an impact on the drain current. However, as the dielectric constant increases, the minimum value of drain current shifts to the left, thus, verifying the increase in gate capacitance. This corresponds to a decrease in the threshold voltage as shown in **Figure 3d**. The threshold voltage exhibits a high shift with increasing negative charge for low-*k* biomolecules as compared to high-*k* cases. For $k = 5$, the threshold voltage increases by 3.56% as the charge of the immobilized biomolecules change from neutral to -10^{12} cm^{-2} as compared to $k = 12$ where the increase is relatively small, that is, 2.49%.

7.1.2. Positively charged biomolecules

Like Section 7.1.1, similar plots are presented here for positive charge of biomolecules. The variation of sensitivity with increasing positive charges for $k = 5$, 7, 10 and 12 is shown in **Figure 4a**. The positive charge of biomolecules depletes the p-type channel, and causes more tunneling of electrons at the source-channel tunnel junction. Hence, the sensitivity increases. For $k = 5$, the sensitivity increases by a factor of 11 when the charge changes from neutral to 10^{12} cm^{-2}, whereas for $k = 12$, the factor is 2.29. The explanation for the trend of the plot can be made in a similar manner as in Section 7.1.1 with the help of Eqs. (6) and (7).

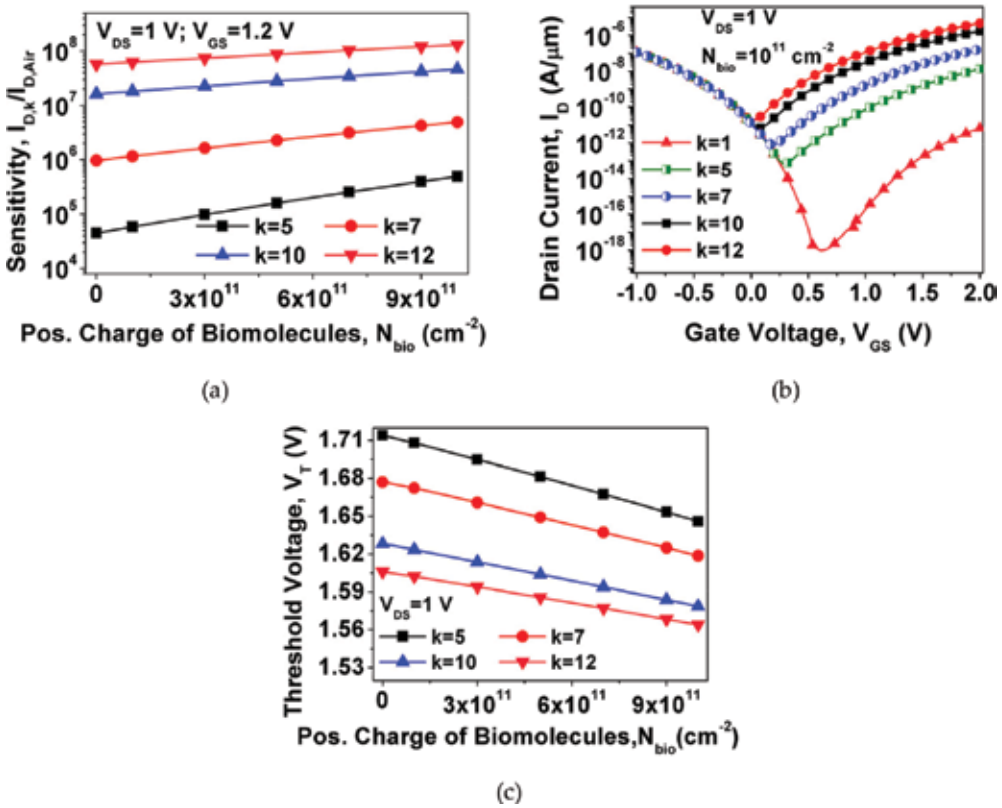

Figure 4. (a) Sensitivity versus positive charge of biomolecules for dielectric constant, $k = 5$, 7, 10 and 12; (b) transfer characteristics of CG TFET as biosensor for $k = 1$ (air), 5, 7, 10 and 12 at fixed negative charge, $N_{bio} = 10^{11}$ cm^{-2}; (c) threshold voltage versus positive charge of biomolecules for dielectric constant, $k = 5$, 7, 10 and 12.

Figure 4b depicts the transfer characteristics of the CG TFET for k = 5, 7, 10, and 12 at $N_{bio} = 10^{11}$ cm^{-2}. The on current in case of positive charged biomolecules is higher than that in case of negatively charged biomolecules as evident from **Table 1**.

In **Figure 4c**, for k = 5, the threshold voltage decreases by 4.03% when the charge changes from neutral to 10^{12} cm^{-2}, whereas for k = 12, the drop is 2.68%.

7.1.3. Sensitivities of DM CG TFET and MOSFET

The comparisons of sensitivities of CG TFET and MOSFET are shown in **Figure 5a** and **b**. At $N_{bio} = \pm 5 \times 10^{11}$ cm^{-2}, the values are extracted for k = 5, 7, 10, and 12. The MOSFET with exactly equal nanogap height and length as that of CG TFET exhibits extremely inferior sensitivity as compared to CG TFET. Earlier works on dielectric-modulated MOSFET have reported similar poor sensitivity of the device as compared to TFET [38, 39].

Sl. No. (horizontal axis of Figure 7)	**Biosensors**	**Reference**
1	Conventional FET	[42]
2	Nanowire TFET	
3	DM FET (L_{GAP} = 200 nm, H_{GAP} = 15 nm, k = 2.1)	[36]
4	DM FET (L_{GAP} = 100 nm, H_{GAP} = 15 nm, k = 2.1)	
5	Full Gate DMTFET (L_{GAP} = 10 nm, L_{GATE} = 42 nm, H_{GAP} = 5 nm, k = 4)	[40]
6	Short Gate DMTFET (L_{GAP} = 10 nm, L_{GATE} = 20 nm, H_{GAP} = 5 nm, k = 4)	
7	DM FET (L_{GAP} = 30 nm, L_{GATE} = 100 nm, H_{GAP} = 9 nm, k = 10)	[39]
8	DM FET (L_{GAP} = 75 nm, L_{GATE} = 250 nm, H_{GAP} = 9 nm, k = 10)	
9	DM PNPN TFET (L_{GAP} = 30 nm, L_{GATE} = 100 nm, H_{GAP} = 9 nm, k = 10)	
10	DM PNPN TFET (L_{GAP} = 75 nm, L_{GATE} = 250 nm, H_{GAP} = 9 nm, k = 10)	
11	DM STS I-MOS (L_{GAP} = 50 nm, L_{GATE} = 120 nm, H_{GAP} = 15 nm, k = 10)	[55]
12	SiGe Source DM PNPN TFET, Ge composition = 0% (L_{GAP} = 15 nm, L_{GATE} = 100 nm, H_{GAP} = 9 nm, k = 2.1)	[41]
13	SiGe Source DM PNPN TFET, Ge composition = 10% (L_{GAP} = 15 nm, L_{GATE} = 100 nm, H_{GAP} = 9 nm, k = 2.1)	
14	SiGe Source DM PNPN TFET, Ge composition = 20% (L_{GAP} = 15 nm, L_{GATE} = 100 nm, H_{GAP} = 9 nm, k = 2.1)	
15	CG TFET (L_{GAP} = 25 nm, L_{GATE} = 40 nm, H_{GAP} = 11 nm, k = 10)	Proposed Work
16	CG TFET (decreasing step) (L_{GAP} = 25 nm, L_{GATE} = 40 nm, H_{GAP} = 11 nm, k = 10)	
17	CG TFET (concave step) (L_{GAP} = 25 nm, L_{GATE} = 40 nm, H_{GAP} = 11 nm, k = 10)	

Table 1. Different reported works on biosensors numbered along the horizontal axis of **Figure 7**.

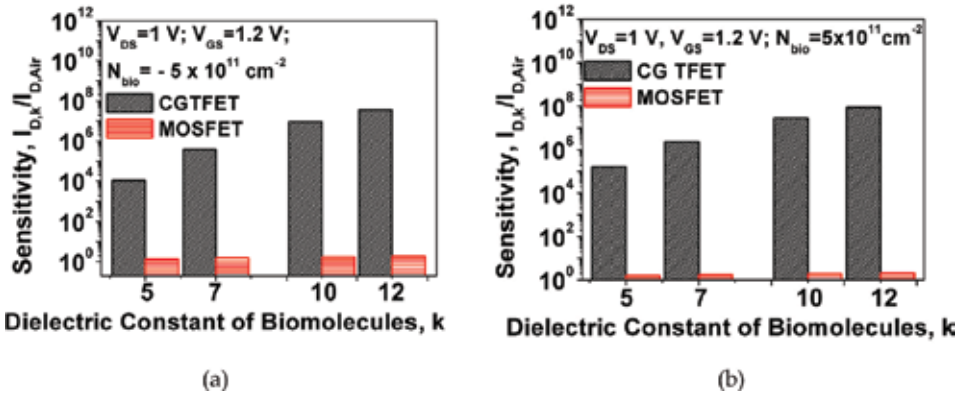

Figure 5. (a) Comparison of sensitivities of dielectric-modulated CG TFET and MOSFET biosensors at gate voltage 1.2 V, drain voltage 1 V and $N_{bio} = -5 \times 10^{11}$ cm^{-2} for dielectric constant, k = 5, 7, 10 and 12; (b) comparison of sensitivities of dielectric-modulated CG TFET and MOSFET biosensors at gate voltage 1.2 V, drain voltage 1 V and $N_{bio} = 5 \times 10^{11}$ cm^{-2} for dielectric constant, k = 5, 7, 10 and 12.

Not only does a shorter channel length affect the electrical characteristics of a MOSFET, but also its principle of thermionic emission by which its operation contributes to such low sensitivity. On the contrary, TFETs which operate by band-to-band tunneling perform well even when scaled. This advantage of TFET is suitable to be exploited for its biosensing capabilities.

7.2. Partially filled Nanogap

The comparison of sensitivity for the four different profiles of partially filled nanogap shown in **Figure 1b–e** is shown in **Figure 6**. Only the decreasing and concave step profiles of biomolecule immobilization respond well to the change in dielectric constant. Contrary to this, the

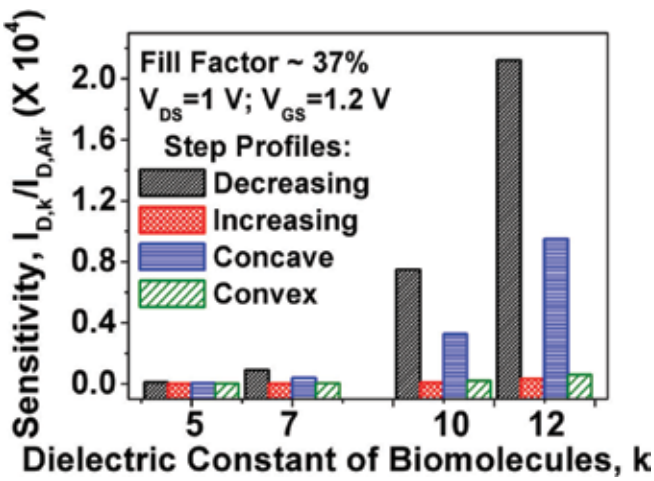

Figure 6. Comparison of sensitivities of step profiles of partially filled nanogap in CG TFET biosensor for dielectric constant, k = 5, 7, 10 and 12.

increasing and convex step profiles demonstrate poor sensitivity. The reason for this is the proximity of the highest step with the source-channel tunnel junction. In case of decreasing and concave step profiles, the higher steps are present near to the tunnel junction as shown in **Figure 1b**, **d** respectively. As the value of k increases, the gate-channel coupling increases in the region of higher steps closer to the tunnel junction. So, the response of the biosensor is better than that of the increasing and convex step profiles where the higher steps are located away from the source-channel tunnel junction.

7.3. Status map of biosensors

There are a number of important simulated and modeled works reported on dielectric-modulated TFET and FET. This section presents a map of the sensitivities of such biosensors proposed till date along with sensitivity of the proposed CG TFET.

Although the status map of **Figure 7** mentions the maximum or best sensitivities of each work, yet the architectural specifications under which the biosensors have been reported vary from one to another, and hence, drawing comparisons among them through **Figure 7** is not justified. However, there are a few conclusions that can be derived from the status map. Dielectric-modulated TFETs are more sensitive to the presence of biomolecules than MOSFETs due to the difference in their current transport mechanisms. In MOSFETs, sensitivities reduce at lesser channel lengths. The CG TFET, with a channel length of 40 nm, shows significant sensitivity; a fully filled nanogap in CG TFET for k = 10 has sensitivity closer to that of DM PNPN TFET for k = 10 possessing a channel length of 250 nm and nanogap length of 75 nm. However, the partially filled nanogaps (decreasing and concave step profiles) have lesser sensitivities than the fully filled case as explained in Section 7.2.

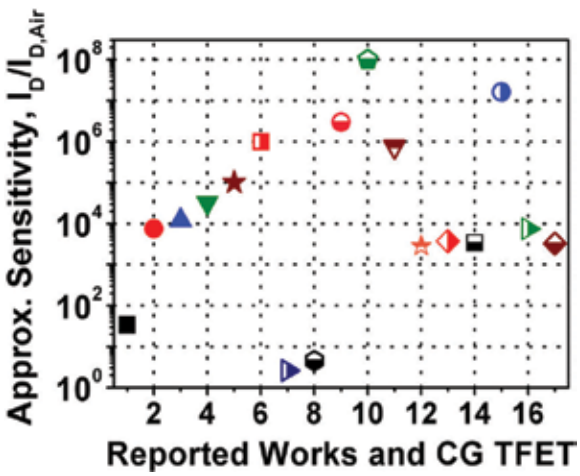

Figure 7. Sensitivities of FET-based biosensors of reported works and those of CG TFET. The sensitivities are extracted from the published works, and due to the possible tolerances in extraction, the vertical axis is named as 'approximate sensitivity'. The various biosensors are referred by using serial numbers from 1 to 17, the details of which are listed in **Table 1**.

8. Conclusion

This chapter has presented an overview on Tunnel Field Effect Transistors (TFETs) as dielectric-modulated biosensors. Tunnel Field Effect Transistors have emerged as one of the most significant devices for low power applications due to their ability to withstand the effects of scaling. With the interests gathering around FET-based biosensors, research on TFETs as biosensors has recently brought new focus. This chapter has discussed the various aspects of dielectric-modulated TFET as biosensor with emphasis on the design and development through simulation analyses. Practical implications of the biosensors are presented. A Circular Gate TFET as a dielectric-modulated biosensor is presented and analyzed at lesser channel length. The CG TFET is observed to offer an impressive sensitivity as compared to other biosensors. The different challenges in implementing a TFET-based dielectric-modulated biosensor are varied, ranging from the problems of steric hindrance, fabrication issues and uncertainty of probe placement. Simulation and modeling may enable one to predict the various effects. Appropriate physics-based models are necessary to validate the results on TCAD tool.

Author details

Rupam Goswami[1]* and Brinda Bhowmick[2]

*Address all correspondence to: rupam.goswamifet@kiit.ac.in

1 Kalinga Institute of Industrial Technology, Bhubaneswar, India

2 National Institute of Technology Silchar, Silchar, India

References

[1] Sarangi S, Bhushan S, Santra A, Dubey S, Jit S, Tiwari PK. A rigorous simulation based study of gate misalignment effects in gate engineered double-gate (DG) MOSFETs. Superlattices and Microstructures. 2013;**60**:263-279. DOI: 10.1016/j.spmi.2013.05.009

[2] Choi WY, Park B-G, Lee JD, Liu T-JK. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Letters. 2007;**28**(8):743-745. DOI: 10.1109/led.2007.901273

[3] Royer CL, Mayer F. Exhaustive experimental study of tunnel field effect transistors (TFETs): From materials to architecture. In: 10th International Conference on Ultimate Integration of Silicon; March 18-20, 2009. Aachen: IEEE; 2009. pp. 53-56. DOI: 10.1109/ulis.2009.4897537

[4] International Technology Roadmap for Semiconductors. http://public.itrs.net/. 2015 Edition. [Accessed: January 06, 2018]

[5] Yang F-L et al. 5nm-gate nanowire fin FET. In: Digest of Technical Papers Symposium. VLSIT; June 15-17, 2004. Honolulu: IEEE; 2004. pp. 196-197. DOI:10.1109/VLSIT.2004.1345476

[6] Elmessary MA, Nagy D, Aldegunde M, Seoane N, Indalecio G, Lindberg J, et al. Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), January 25-27, 2016. Vienna: IEEE; 2016. pp. 52-55. DOI: 10.1109/ulis.2016.7440050

[7] Yoon J-S, Kim K, Rim T, Baek C-K. Performance and variations induced by single interface trap of nanowire FETs at 7-nm node. IEEE Transactions on Electron Devices. 2017;**64**(2): 339-345. DOI: 10.1109/ted.2016.2633970

[8] Wong HSP. Beyond the conventional transistor. IBM Journal of Research and Development. 2002;**46**(2.3):133-168. DOI: 10.1147/rd.462.0133

[9] Guo J, Datta S, Lundstrom M. A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors. IEEE Transactions on Electron Devices. 2004;**51**(2):172-177. DOI: 10.1109/ted.2003.821883

[10] Yousefi R, Shabani M. A model for carbon nanotube FETs in the ballistic limit. Microelectronics Journal. 2011;**42**(11):1299-1304. DOI: 10.1016/j.mejo.2011.08.012

[11] Fiori G, Iannaccone G. Simulation of graphene nanoribbon field-effect transistors. IEEE Electron Device Letters. 2007;**28**(8):760-762. DOI: 10.1109/led.2007.901680

[12] Echtermeyer T, Lemme M, Baus M, Szafranek B, Geim A, Kurz H. Nonvolatile switching in graphene field-effect devices. IEEE Electron Device Letters. 2008;**29**(8):952-954. DOI: 10.1109/led.2008.2001179

[13] Tamersit K, Djeffal F. Double-gate graphene Nanoribbon field-effect transistor for DNA and gas sensing applications: Simulation study and sensitivity analysis. IEEE Sensors Journal. 2016;**16**(11):4180-4191. DOI: 10.1109/jsen.2016.2550492

[14] Nirschl T, Wang P-F, Hansch W, Schmitt-Landsiedel D. The tunnelling field effect transistors (TFET): The temperature dependence, the simulation model, and its application. In: IEEE International Symposium on Circuits and Systems; May 23-26, 2004. Vancouver: IEEE, p. III-713-16. DOI: 10.1109/ISCAS.2004.1328846

[15] Jiang C, Liang R, Xu J. Investigation of negative capacitance gate-all-around tunnel FETs combining numerical simulation and analytical modeling. IEEE Transactions on Nanotechnology. 2016;**16**(1):58-67. DOI: 10.1109/tnano.2016.2627808

[16] Omura Y, Mallik A, Matsuo N. The impact of a fringing field on the device performance of a P-channel tunnel field-effect transistor with a high-κ gate dielectric. In: MOS Devices for Low-Voltage and Low-Energy Applications. Singapore: Wiley; 2016. pp. 399-411. DOI: 10.1002/9781119107361.ch34

[17] Shen M, Saikin S, Cheng M-C. Spin injection in spin FETs using a step-doping profile. IEEE Transactions On Nanotechnology. 2005;**4**(1):40-44. DOI: 10.1109/tnano.2004.840150

[18] Datta S, Das B. Electronic analog of the electro-optic modulator. Applied Physics Letters. 1998;**56**(7):665-667. DOI: 10.1063/1.102730

[19] Sugahara S, Tanaka M. A spin metal-oxide-semiconductor field-effect transistor (spin MOSFET) with a ferromagnetic semiconductor for the channel. Journal of Applied Physics. 2005;**97**(10):10D503. DOI: 10.1063/1.1852280

[20] Salahuddin S. Review of negative capacitance transistors. In: International Symposium on VLSI Technology, Systems and Application (VLSI-TSA); April 25-27, 2016. Hsinchu: IEEE. pp. 1-1. DOI: 10.1109/vlsi-tsa.2016.7480491

[21] Jo J, Shin C. Impact of temperature on negative capacitance field-effect transistor. Electronics Letters. 2015;**51**(1):106-108. DOI: 10.1049/el.2014.3515

[22] Boucart K, Ionescu A. Double gate tunnel FET with ultrathin silicon body and high-k gate dielectric. In: Proceedings of the European Solid-State Device Research Conference, September 19-21, 2006. Montreux: IEEE; 2007. pp. 1725-1733. DOI: 10.1109/essder.2006.307718

[23] Boucart K, Ionescu AM. Length scaling of the double gate tunnel FET with a high-K gate dielectric. Solid-State Electronics. 2007;**51**(11-12):1500-1507. DOI: 10.1016/j.sse.2007.09.014

[24] Lam K-T, Seah D, Chin S-K, Kumar SB, Samudra G, Yeo Y-C, et al. A simulation study of graphene-nanoribbon tunneling FET with heterojunction channel. IEEE Electron Device Letters. 2010;**31**(6):555-557. DOI: 10.1109/led.2010.2045339

[25] Vishnoi R, Kumar MJ. Compact analytical drain current model of gate-all-around nanowire tunneling FET. IEEE Transactions on Electron Devices. 2014;**61**(7):2599-2603. DOI: 10.1109/ted.2014.2322762

[26] Toh E-H, Wang GH, Chan L, Sylvester D, Heng C-H, Samudra GS, et al. Device design and scalability of a double-gate tunneling field-effect transistor with silicon–germanium source. Japanese Journal of Applied Physics. 2008;**47**(4):2593-2597. DOI: 10.1143/jjap.47.2593

[27] Ahish S, Sharma D, Kumar YBN, Vasantha MH. Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping. IEEE Transactions on Electron Devices. 2016;**63**(1):288-295. DOI: 10.1109/ted.2015.2503141

[28] Dewey G, Chu-Kung B, Boardman J, Fastenau JM, Kavalieros J, Kotlyar R, et al. Fabrication, characterization, and physics of III–V heterojunction tunneling field effect transistors (H-TFET) for steep sub-threshold swing. In: International Electron Devices Meeting, December 5-7, 2011. Washington, DC: IEEE; 2012. pp. 33.6.1-33.6.4. DOI: 10.1109/iedm.2011.6131666

[29] Bagga N, Dasgupta S. Surface potential and drain current analytical model of gate all around triple metal TFET. IEEE Transactions on Electron Devices. 2017;**64**(2):606-613. DOI: 10.1109/ted.2016.2642165

[30] Bagga N, Sarkar SK. An analytical model for tunnel barrier modulation in triple metal double gate TFET. IEEE Transactions on Electron Devices. 2015;**62**(7):2136-2142. DOI: 10.1109/ted.2015.2434276

[31] Dash S, Mishra G. A new analytical threshold voltage model of cylindrical gate tunnel FET (CG-TFET). Superlattices and Microstructures. 2015;**86**:211-220. DOI: 10.1016/j.spmi.2015.07.049

[32] Lee MJ, Choi WY. Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs). Solid-State Electronics. 2011;**63**(1):110-114. DOI: 10.1016/j.sse.2011.05.008

[33] Luong G, Strangio S, Tiedemannn A, Lenk S, Trellenkamp S, Bourdelle K, et al. Experimental demonstration of strained Si nanowire GAA n-TFETs and inverter operation with complementary TFET logic at low supply voltages. Solid-State Electronics. 2016;**115**:152-159. DOI: 10.1016/j.sse.2015.08.020

[34] Mookerjea S, Mohata D, Krishnan R, Singh J, Vallett A, Ali A, et al. Experimental demonstration of 100nm channel length In0.53Ga0.47As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications. In: IEEE International Electron Devices Meeting (IEDM), December 7-9, 2009. Baltimore: IEEE; 2010. pp. 1-3. DOI: 10.1109/iedm.2009.5424355

[35] Singh J, Ramakrishnan K, Mookerjea S, Datta S, Vijaykrishnan N, Pradhan D. A novel Si-tunnel FET based SRAM design for ultra low-power 0.3V VDD applications. In: 15th Asia and South Pacific Design Automation Conference (ASP-DAC), January 18-21, 2010. Taipei: IEEE; 2010. pp. 181-186. DOI: 10.1109/aspdac.2010.5419897

[36] Im H, Huang X-J, Gu B, Choi Y-K. A dielectric-modulated field-effect transistor for biosensing. Nature Nanotechnology. 2007;**2**(7):430-434. DOI: 10.1038/nnano.2007.180

[37] Narang R, Saxena M, Gupta RS, Gupta M. Dielectric modulated tunnel field-effect transistor—A biomolecule sensor. IEEE Electron Device Letters. 2012;**33**(2):266-268. DOI: 10.1109/led.2011.2174024

[38] Narang R, Reddy KVS, Saxena M, Gupta RS, Gupta M. A dielectric-modulated tunnel-FET-based biosensor for label-free detection: Analytical modeling study and sensitivity analysis. IEEE Transactions on Electron Devices. 2012;**59**(10):2809-2817. DOI: 10.1109/TED.2012.2208115

[39] Narang R, Saxena M, Gupta RS, Gupta M. Comparative analysis of dielectric-modulated FET. IEEE Transactions on Nanotechnology. 2015;**14**(3):427-435. DOI: 10.1109/TNANO.2015.2396899

[40] Kanungo S, Chattopadhyay S, Gupta PS, Rahaman H. Comparative performance analysis of the dielectrically modulated full-gate and short-gate tunnel FET-based biosensors. IEEE Transactions on Electron Devices. 2015;**62**(3):994-1001. DOI: 10.1109/ted.2015.2390774

[41] Kanungo S, Chattopadhyay S, Gupta PS, Sinha K, Rahaman H. Study and analysis of the effects of SiGe source and pocket-doped channel on sensing performance of dielectrically modulated tunnel FET-based biosensors. IEEE Transactions on Electron Devices. 2016;**63**(6):2589-2596. DOI: 10.1109/ted.2016.2556081

[42] Sarkar D, Banerjee K. Proposal for tunnel-field-effect-transistor as ultra-sensitive and label-free biosensors. Applied Physics Letters. 2012;**100**(14):143108. DOI: 10.1063/1.3698093

[43] Bergveld P. Thirty years of ISFETOLOGY. Sensors and Actuators B: Chemical. 2003;**88**(1):1-20. DOI: 10.1016/s0925-4005(02)00301-5

[44] Kim C-H, Ahn J-H, Lee K-B, Jung C, Park HG, Choi Y-K. A new sensing metric to reduce data fluctuations in a nanogap-embedded field-effect transistor biosensor. IEEE Transactions on Electron Devices. 2012;**59**(10):2825-2831. DOI: 10.1109/ted.2012.2209650

[45] Abdi DB, Kumar MJ. Dielectric modulated overlapping gate-on-drain tunnel-FET as a label-free biosensor. Superlattices and Microstructures. 2015;**86**:198-202. DOI: 10.1016/j.spmi.2015.07.052

[46] Ahangari Z. Performance assessment of dual material gate dielectric modulated nanowire junctionless MOSFET for ultrasensitive detection of biomolecules. RSC Advances. 2016;**6**(92):89185-89191. DOI: 10.1039/c6ra17361f

[47] Knoch J, Appenzeller J. A novel concept for field-effect transistors – The tunneling carbon nanotube FET. In: 63rd Device Research Conference Digest, DRC 05; June 20-22, 2005. Santa Barbara: IEEE; 2005. pp. 153-156. DOI: 10.1109/drc.2005.1553099

[48] Knoch J, Mantl S, Appenzeller J. Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices. Solid-State Electronics. 2007;**51**(4):572-578. DOI: 10.1016/j.sse.2007.02.001

[49] Wang C, Wu C, Wang J, Huang Q, Huang R. Analytical current model of tunneling field-effect transistor considering the impacts of both gate and drain voltages on tunneling. Science China Information Sciences. 2014;**58**(2):1-8. DOI: 10.1007/s11432-014-5196-3

[50] Synopsys. Sentaurus Device User Guide. Mountain View: Synopsys, Inc.; 2011

[51] Ortiz-Conde A, García S Fj, Liou J, Cerdeira A, Estrada M, Yue Y. A review of recent MOSFET threshold voltage extraction methods. Microelectronics Reliability. 2002;**42**(4-5):583-596. DOI: 10.1016/s0026-2714(02)00027-6

[52] Ortiz-Conde A, García-Sánchez FJ, Muci J, Barrios AT, Liou JJ, Ho C-S. Revisiting MOSFET threshold voltage extraction methods. Microelectronics Reliability. 2013;**53**(1):90-104. DOI: 10.1016/j.microrel.2012.09.015

[53] Goswami R, Bhowmick B, Baishya S. Electrical noise in circular gate tunnel FET in presence of interface traps. Superlattices and Microstructures. 2015;**86**:342-354. DOI: 10.1016/j.spmi.2015.07.064

[54] Tsividis Y. Operation and Modelling of the MOS Transistor. 2nd ed. New York: Oxford University Press; 1999

[55] Singh S, Kondekar P, Jaiswal NK. Label-free biosensor using nanogap embedded dielectric modulated schottky tunneling source impact ionization MOS. Microelectronic Engineering. 2016;**149**:129-134. DOI: 10.1016/j.mee.2015.10.005

Chapter 3

Band Gap Modulated Tunnel FET

Brinda Bhowmick and Rupam Goswami

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.76098

Abstract

This chapter presents bandgap-modulated tunnel field effect transistor (TFET) and discusses its simulation and modeling. A geometry of TFET, the heterojunction TFET, is considered, and different electrical parameters are discussed using Technology Computer Aided Design (TCAD) tool. The effect of the heterojunction on the characteristics is observed through the variations in the length and mole fraction of the pocket layer adjacent to the source. An analytical model is further presented for gate-drain underlap TFET using 2-D Poisson equation and Kane's interband tunneling model. The results are validated with the output from the TCAD tool.

Keywords: heterojunction TFET, TCAD, analytical model, subthreshold swing, tunneling

1. Introduction

Tunnel field effect transistor (TFET) is an asymmetrical gated p-i-n device. Unlike thermionic conduction in metal-oxide-semiconductor FETs (MOSFETs), its working principle is based on a band-to-band tunneling (BTBT) mechanism [1, 2]. This amendment results in a reduced subthreshold swing (SS), low off-state leakage currents, and less short-channel effects. Recently, numerous structural and material designs of TFETs have been proposed with an objective to achieve improvement in subthreshold swing (SS) and off current. A few of them are bandgap-engineered TFETs [3], graphene nanoribbon TFETs [4], gate-engineered TFET [5], and strained silicon-germanium TFETs [6]. Double-gate TFET [7], dual-material gate TFET [8], hetero-gate dielectric TFET [9], and heterojunction TFETs [10] have also been investigated for improved electrical parameters of TFET. Generally, TFETs have a very low current as compared to ITRS requirement. In order to get a high ON current, a high-k gate dielectrics are preferred. High-k gate dielectrics causes improved capacitive coupling between the gate and the source-channel tunnel junction, resulting in an increased current in TFET. Moreover, to decline the effective oxide

thickness at the tunnel junction, high-k gate oxide is used so that the gate-tunneling current can be reduced. Actually, due to these reasons, the recent trend is to use high-k materials as a better replacement of the conventional SiO_2 (silicon dioxide). On the other hand, it causes a significant ambipolar current. The gate-drain underlap structure in association with heterojunction can be adopted to diminish ambipolar current [2]. A silicon-germanium (SiGe) layer is used at the tunnel junction so that bandgap and tunnel width can be modulated. Electrical parameters have been investigated for various Ge-mole fractions.

Technology Computer Aided Design (TCAD) simulation is a complex iterative mathematical process, and hence various analytical models have been proposed in order to develop a better understanding of the physics-based principles of TFETs and obtain results not constrained by computational time [11]. A number of analytical models based on Poisson equation have been proposed in the study for different geometries [12–14]. In this chapter, a mole fraction-dependent model has been proposed and validated.

This chapter is organized as follows: first, the heterojunction gate-drain underlap tunnel is discussed, and in the second section, the electrical parameters of the heterojunction gate-drain underlap tunnel FET (UL-HTFET) is investigated with the help of TCAD simulation. The third section discusses the physics-based compact model and the validation of the model with simulated results. In the last section, the effect of temperature on the electrical parameters is investigated.

2. Heterojunction gate-drain underlap tunnel FET

A 2-D structure of the proposed UL-HTFET is shown in **Figure 1**. Here, a *p* + source and *n* + drain with an intrinsic channel and a δ*p* + $Si_{1-x}Ge_x$ layer at the source-channel tunnel junction are present. The δ*p* + layer can be replaced by a δ*n* + layer too.

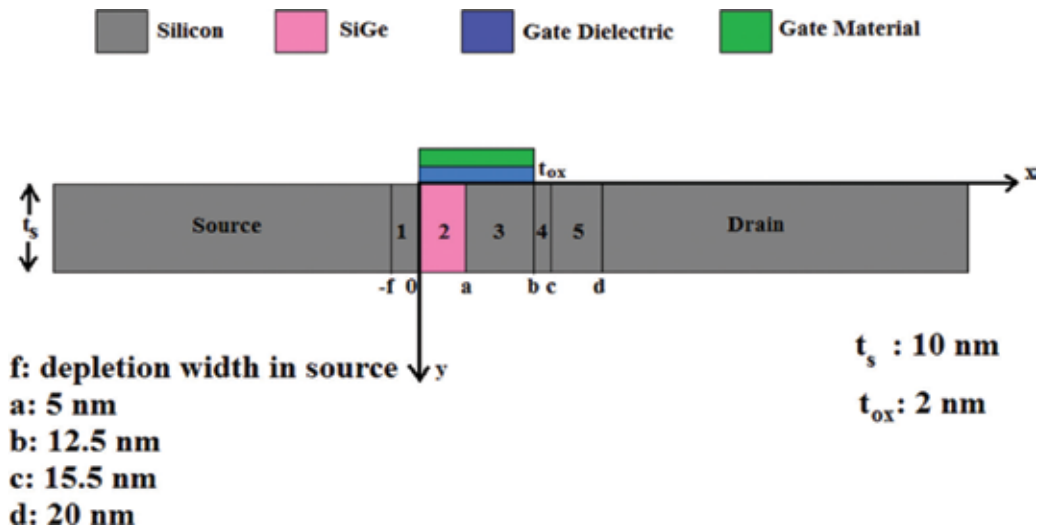

Figure 1. A 2-D geometry of the device (UL-HTFET).

The effect of germanium mole fraction on the UL-HTFET is investigated. Aluminum with work function (4.1 eV) is considered as the gate material. The proposed device spans across a total length of 100 nm with a length of the channel equal to 20 nm. The $\delta p + Si_{1-x}Ge_x$ layer extends from the source-channel junction up to 1 nm into the channel under the gate. The various doping concentrations are used such as source, 10^{21} cm^{-3}; drain, 5×10^{19} cm^{-3}; δp + layer, 10^{18} cm^{-3}; and intrinsic region, 10^{16} cm^{-3}. In n-channel, the operation of TFET positive gate and drain voltages is applied with respect to the source. Here, voltage at the source is considered as the reference voltage.

The tunnel FET works on the principle of band-to-band tunneling. Here, SiGe layer is added at the channel near the source-channel junction to enhance the on-current.

3. Simulated results of UL-HTFET

Figure 2 shows the I_{ds}-V_{gs} characteristics of the Si/Ge heterojunction UL-HTFET at different lengths of L_p. When the HTFET is turned on, it shows very high on-current due to the effective bandgap narrowing at the interface of source-channel junction. The I_{ds}-V_{gs} curves are mainly dependent on n + −doped pocket length (L_p) as shown in **Figure 2**; as L_p gets longer, the effective area for tunneling width is extended for HTFET. However, the low off-state current in UL-HTFET (9.205×10^{-20} A/μm) when L_p is less than 2 nm, and this indicates that the ambipolar-tunneling effect at drain channel is suppressed. When L_p is 2 nm, as observed, the tunneling width becomes extremely thin to concede tunneling current at V_{gs} = −0.5 V. This tunneling current interrupts UL-HTFET device performance at off-state. The low I_{off} can be achieved at L_p = 1 and 2 nm, and I_{on} is greatly higher at L_p = 4 nm in TFET. Therefore, an optimum L_p can be located at 1 nm where high ion is achieved and the leakage is suppressed as shown in I_{ds}-V_{gs} characteristics.

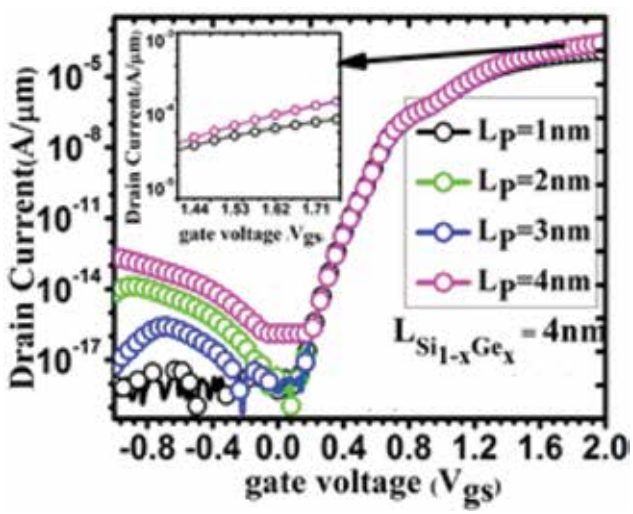

Figure 2. Transfer characteristics for varying L_p lengths at V_{ds} = 0.7 V.

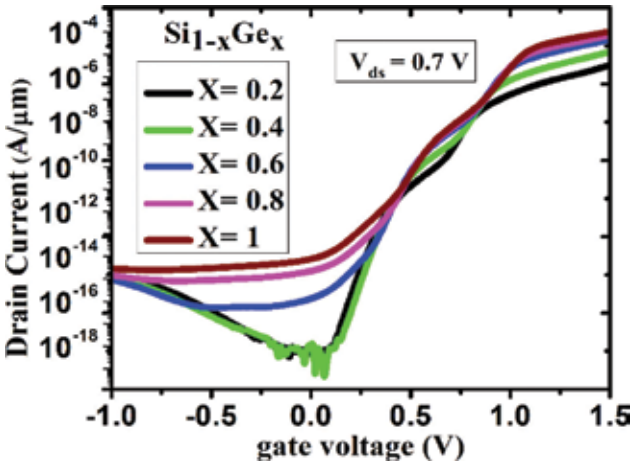

Figure 3. I_d-V_{gs} characteristics of UL-HTFET with varying Ge-mole fractions.

In **Figure 3**, the I_d-V_{gs} characteristics of the UL-HTFET is shown. The mole fraction of SiGe layer is varied. With germanium mole fraction of 0.4, the best I_{on}/I_{off} ratio has been achieved (10^{12}). For Ge-mole fractions below 0.5, the device exhibits a better ratio. As the mole fraction increases beyond 0.5, the properties of the n + layer align more with those of germanium than of silicon. With an increase in mole fraction greater than 0.4, the on-current increases but the increase in off-current is more. This is due to an effective band bending at the source-channel tunnel junction by which the tunnel width can be modulated. For a reduced tunnel width in ON state (V_{gs} = 1 V), more ON current is achieved. However, at OFF state, the current is due to thermionic emission as the tunnel current is insignificant.

The energy band diagram is plotted at different mole fractions at ON state (V_{ds} = 0.7 V, V_{gs} = 1.2 V) shown in **Figure 4**. It is observed that at 0.8-mole fraction of germanium, the ON current is more. With an increase in Ge-mole fraction, the tunnel width reduces and hence enhanced ON current is achieved. In the inset of **Figure 4**, the variation of valence band with mole fraction is shown. The conduction band variation is insignificant with mole fraction.

In **Figure 5**, the electric field is shown at different mole fractions. The peak electric field is observed around 20-nm length along the lateral direction. This is the source-channel tunnel junction. A high electric field at this location is due to the presence of a large tunnel barrier. With the increased mole fraction (at x = 1), a highest peak is observed, and hence tunneling probability will increase and be responsible for the increased current in ON state.

The ON/OFF current ratio and the subthreshold swing are shown in **Figure 6**. The best I_{ON}/I_{OFF} ratio is achieved for Ge-mole fraction of 0.3. In TFETs, an abrupt I_d-V_{gs} plot is obtained where the subthreshold swing varies with gate voltage. Therefore, two types of SS [15] are defined in TFETs: one is the average SS and the other is known as point SS. The average SS is defined mathematically as

$$SSav = (V_T - V_{OFF})/[\log(I_T) - \log(I_{OFF})] \quad (1)$$

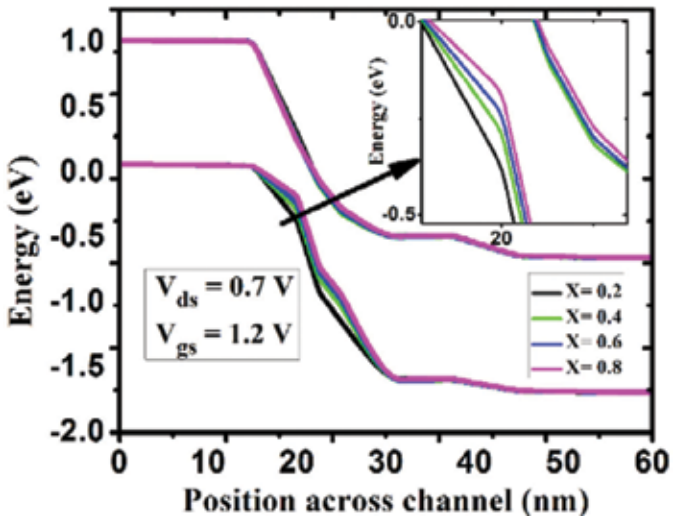

Figure 4. Energy band diagram at ON state.

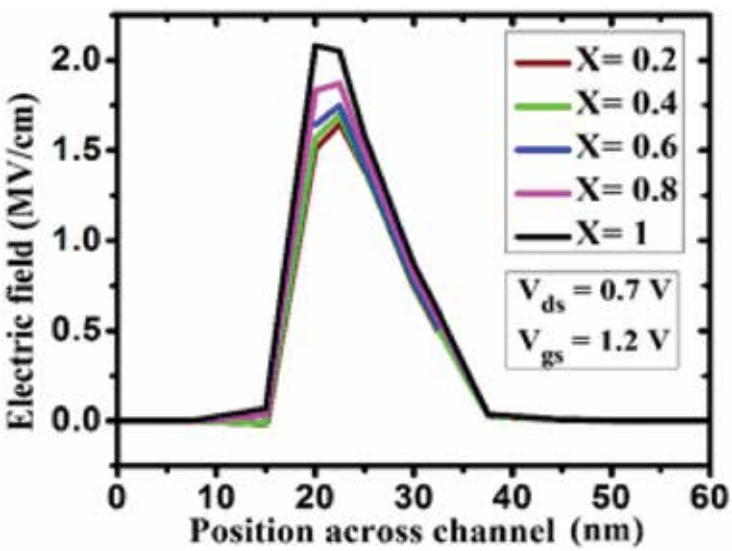

Figure 5. Electric field along the channel length in UL-HTFET.

where V_T is the threshold voltage and V_{OFF} is the value of gate voltage at which the drain current just begins to take off. I_T and I_{OFF} are the drain currents at the respective voltages. Point SS, on the other hand, is the minimum SS at any point on the I_d-V_{gs} plot. The plot of average SS for different Ge-mole fractions is shown in **Figure 6**. A remarkable average SS (37 mV/dec) is achieved at 0.2 Ge-mole fraction.

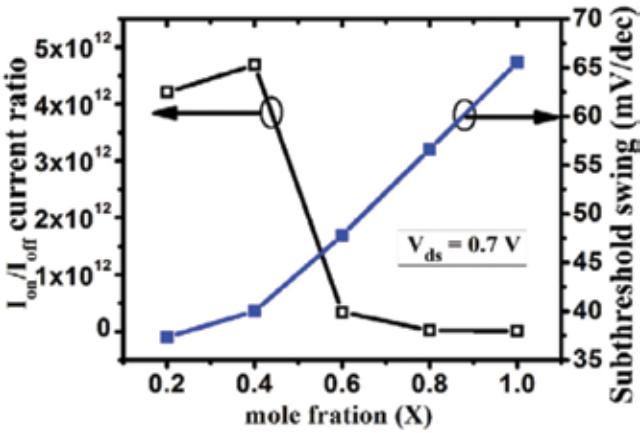

Figure 6. ON and OFF current ratios (I_{ON}/ I_{OFF}) and subthreshold swing (SS) versus Ge-mole fraction.

4. Development of analytical model for UL-HTFET

4.1. 2-D Poisson equation-based model

In regions 1–4 of **Figure 1**, the 2-D Poisson's equation is considered and the 1-D Poisson's equation is solved on region 5 due to the absence of gate overlap. The following assumptions have been considered while modeling [12–16]:

1. No trap charges are considered.
2. There are no immobile charges in gate dielectric.
3. Gate leakage current is zero.
4. Source-channel and channel-drain depletion regions do not have any kind of mobile charges.

In regions I–IV, the 2-D Poisson's equation is given as follows:

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \frac{qN_i}{\varepsilon_i} \tag{2}$$

where the subscript $i = 1, 2, 3, 4$ corresponding to regions 1, 2, 3, or 4.

$\Psi_i(x,y)$, N_i, and ε_i are the two-dimensional potential, doping concentration, and permittivity of the semiconductor material, respectively, in the respective four regions.

The 2-D potential is approximated as parabolic along the depth of the device. So, the assumption for the 2-D potential is considered as

$$\Psi_i(x,y) = C_{0i}(x) + C_{1i}(x)y + C_{2i}(x)y^2 \tag{3}$$

where $C_{0i}(x)$, $C_{1i}(x)$, and $C_{2i}(x)$ are coefficients that are functions of mole fraction.

In each of the four regions, three vertical boundary conditions must be satisfied to confirm the continuity of potential and electric field at the gate insulator–semiconductor interface ($y = 0$) and at the lowermost part of the device ($y = t_s$)

$$\Psi_{\mathrm{i}}(\mathrm{x},0) = \Psi_{\mathrm{si}}(\mathrm{x})$$

$$\frac{\partial \Psi_{\mathrm{i}}(\mathrm{x},0)}{\partial y} = \frac{\varepsilon_{\mathrm{i}}}{\varepsilon_{\mathrm{ox}}\mathrm{t}_{\mathrm{ox}}}\{\Psi_{\mathrm{si}}(\mathrm{x}) - \mathrm{v}_{\mathrm{i}}\}$$

$$\frac{\partial \Psi_i(x,t_s)}{\partial y} = 0 \tag{4}$$

where $\Psi_{si}(x)$ is the surface potential, ε_{ox} is the permittivity of gate dielectric, t_{ox} is the gate dielectric thickness, and $v_i = V_{GS} - V_{fbi}$. The gate voltages with respect to source and the flatband voltage are represented by V_{GS}, and V_{fbi}, respectively. The bandgap E_{Gi} is a function of Ge-mole fraction in $Si_{1-x}Ge_x$ expressed as a linear interpolation of the bandgaps of Si ($\sim$ 1.10 eV) and Ge ($\sim$ 0.66 eV):

$$E_{Gi} = 1.10 - 0.34\mathrm{x} \tag{5}$$

Using the boundary conditions of Eq. (4), we obtain the coefficients of Eq. (3) as follows:

$$\mathrm{C}_{0\mathrm{i}} = \Psi_{\mathrm{si}}(\mathrm{x})$$

$$\mathrm{C}_{1\mathrm{i}} = \frac{\varepsilon_{\mathrm{i}}}{\varepsilon_{\mathrm{ox}}\mathrm{t}_{\mathrm{ox}}}\{\Psi_{\mathrm{si}}(\mathrm{x}) - \mathrm{v}_{\mathrm{i}}\}$$

$$C_{2i} = \frac{\varepsilon_i}{2\varepsilon_{ox}t_{ox}t_s}\{v_i - \Psi_{si}(x)\} \tag{6}$$

Using the coefficients of Eq. (6) in the polynomial in Eq. (3), the 2-D Poisson's equation can be expressed as

$$\Psi_{si}{}^{//} - k_i^2\Psi_{si} = k_i^2\xi_i \tag{7}$$

with

$$k_i = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_i t_{ox} t_s}}$$

and $\xi_i = \frac{qN_i}{\varepsilon_i k_i^2} - v_i$.

Eq. (7) has a solution of the form:

$$\Psi_{si}(x) = A_i e^{+k_i x} + B_i e^{-k_i x} - \xi_i \tag{8}$$

The surface potentials for regions I–IV of the device are represented by Eq. (8). For region V, we apply 1-D Poisson's equation:

$$\frac{\partial^2 \Psi_5(x)}{\partial x^2} = \frac{qN_5}{\varepsilon_5} \tag{9}$$

to get

$$\Psi_5(x) = \Psi_{s5}(x) = \frac{qN_5}{\varepsilon_5}x^2 + C_1 x + C_2 \tag{10}$$

The coefficients $A_1, B_1, A_2, B_2, A_3, B_3, A_4, B_4, C_1,$ and C_2 must satisfy the boundary conditions for the continuity of surface potential and electric field in the five regions:

$$\Psi_{s1}(-\mathrm{f}) = -\left(\frac{\mathrm{kT}}{\mathrm{q}}\right)\ln\left(\frac{\mathrm{N_s}}{\mathrm{n_{i1}}}\right)$$

$$\Psi_{s1}(0) = \Psi_{s2}(0)$$

$$\frac{\partial \Psi_{s1}(0)}{\partial x} = \frac{\partial \Psi_{s2}(0)}{\partial x}$$

$$\Psi_{s2}(\mathrm{a}) = \Psi_{s3}(\mathrm{a})$$

$$\frac{\partial \Psi_{s2}(\mathrm{a})}{\partial x} = \frac{\partial \Psi_{s3}(\mathrm{a})}{\partial x}$$

$$\Psi_{s3}(\mathrm{b}) = \Psi_{s4}(\mathrm{b})$$

$$\frac{\partial \Psi_{s3}(\mathrm{b})}{\partial x} = \frac{\partial \Psi_{s4}(\mathrm{b})}{\partial x}$$

$$\Psi_{s4}(\mathrm{c}) = \Psi_{s5}(\mathrm{c})$$

$$\frac{\partial \Psi_{s4}(\mathrm{c})}{\partial x} = \frac{\partial \Psi_{s5}(\mathrm{c})}{\partial x}$$

$$\Psi_{s5}(d) = V_{DS} + \left(\frac{kT}{q}\right)\ln\left(\frac{N_d}{n_{i2}}\right) \tag{11}$$

where V_{DS} is the drain voltage with respect to source, and n_{i1} and n_{i2} are the intrinsic concentrations of the $Si_{1-x}Ge_x$ layer and silicon, respectively. Here, *a*, *b*, *c*, *d*, and *-f* are the various positions along the channel at which the boundary conditions are applied. Their

values are mentioned in the inset of **Figure 1**. The width of the depletion region in the source is expressed as

$$f = \sqrt{\frac{2\varepsilon_1|\xi_1 - \Psi_{ss}|}{q|N_1|}} \tag{12}$$

where

$$\Psi_{ss} = -\frac{kT}{q}\ln\left(\frac{N_s}{n_{i2}}\right)$$

Using Eqs. (8) and (10), the lateral electric field for the five regions is given as

$$\mathrm{E_{xi}} = -\mathrm{k_i}\left(\mathrm{P_i e^{k_i x}} - \mathrm{Q_i e^{-k_i x}}\right)$$

for i = 1, 2, 3, 4 corresponding to regions I, II, III, or IV.

and

$$\mathrm{E_{x5}} = -\left(\frac{\mathrm{qN_5 x}}{\varepsilon_5} + \mathrm{C_1}\right) \tag{13}$$

The vertical electric fields for the different regions are expressed using Eqs. (3) and Eq. (10) as

$$E_{yi} = -(a_{1i} + 2a_{2i}y) \tag{14}$$

for i = 1, 2, 3, 4 corresponding to regions I, II, III, or IV.

and

$$\mathrm{E_{y5}} = 0 \tag{15}$$

The drain current is calculated by integrating the band-to-band generation rate G_{BTBT} over the volume of the device

$$I_d = q\int G_{BTBT}dV \tag{16}$$

where

$$G_{BTBT} = A\frac{|E|^2}{\sqrt{E_{Gi}}}\exp\left(-B\frac{E_{Gi}^{1.5}}{|E|}\right) \tag{17}$$

where $E = \sqrt{E_x^2 + E_y^2}$

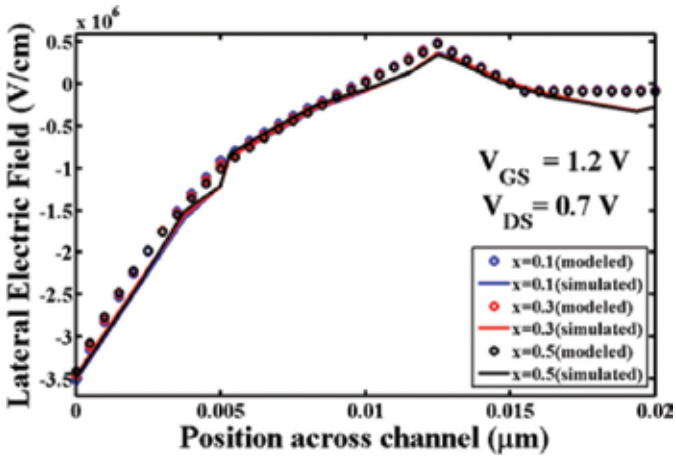

Figure 7. Variation of lateral electric field at the surface in the channel for different Ge-mole fractions.

4.2. Validation of the analytical model

The developed analytical models are validated with simulation data from TCAD. **Figure 7** shows the plot of lateral electric field at the surface of the UL-HTFET in the channel region for different Ge-mole fractions of the silicon-germanium layer, at $V_{GS} = 1.2\ V$ and $V_{DS} = 0.7\ V$. It has been seen that the modeled values match with the simulated values of lateral electric field except that a small mismatch in the field is observed at the position in the channel where the gate-channel overlap terminates.

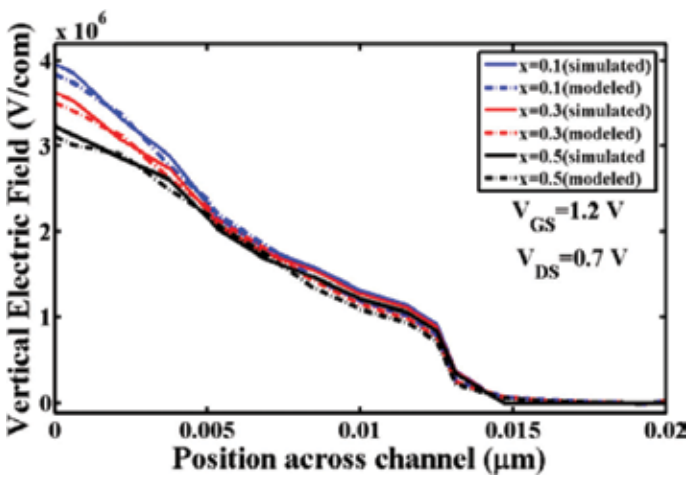

Figure 8. Variation of vertical electric field at the surface in the channel for different Ge-mole fractions.

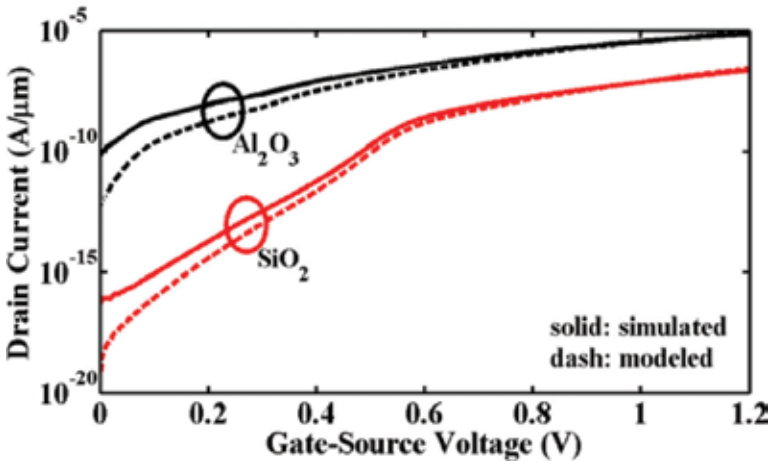

Figure 9. I_D-V_{gs} characteristics at Ge-mole fraction equal to 0.5, gate voltage equal to 1.2 V, and drain voltage equal to 0.7 V.

A plot of vertical electric field at the surface of the device versus horizontal position in the channel region is shown in **Figure 8** for different values of Ge-mole fractions at a fixed drain voltage of 0.7 V and a gate voltage of 1.2 V. For all the cases, it has been observed that the modeled results closely approach the simulated results. The simulated vertical electric field is slightly different as compared to the modeled ones near the junction of silicon-germanium-silicon in the channel region; however, at other positions in the channel, there is a close match between the modeled and the simulated values of vertical electric field.

The variation of drain current with gate voltage has been computed and portrayed in **Figure 9**. There is a close match between the model and the simulated data.

5. Dependence of threshold voltage on temperature

An algorithm for the extraction of threshold voltage in heterojunction TFET is presented in **Figure 10** [17]. The algorithm uses the analytical model of Section 4 to plot multiple curves of surface potential versus position for different gate voltages and fixed drain voltage. The advantage of this algorithm is that the procedure is completely computational, and the threshold voltage can be determined without deriving the transfer characteristics. Moreover, the method can be extended to fit different threshold voltage extraction methods by changing the fitting parameter [17].

The model takes into account the dependence of temperature. The method involves geometrical constructions on a plot of surface potential versus position and using mathematical parameters to define a variable *range_point*.

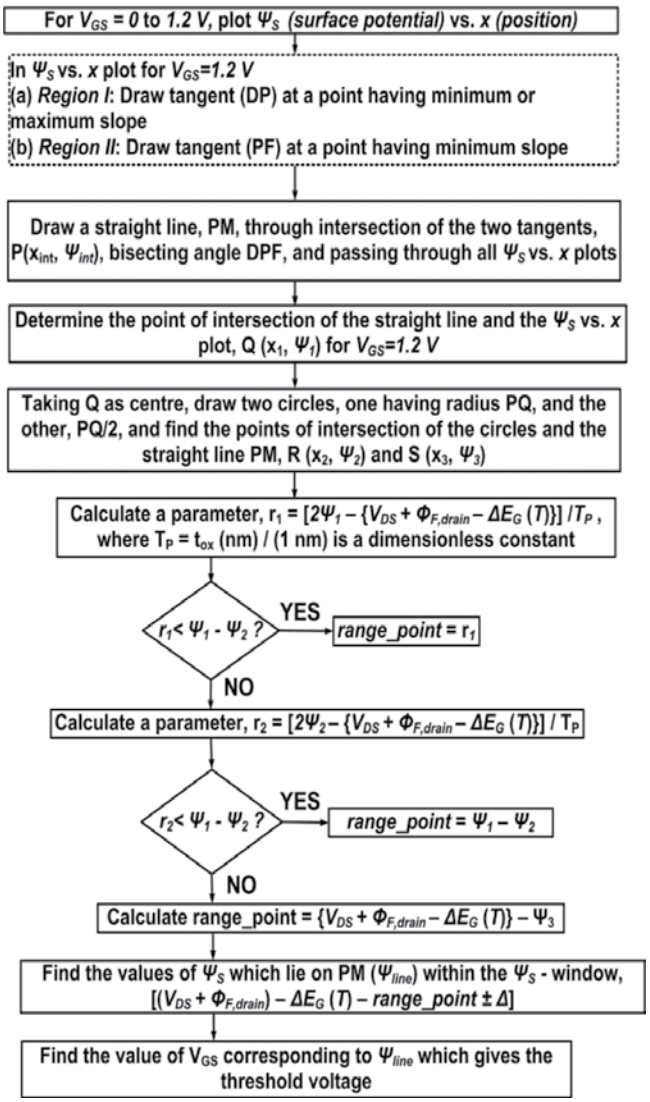

Figure 10. Algorithm for the extraction of threshold voltage in heterojunction and homojunction TFETs [17].

A plot of threshold voltage versus temperature is shown in **Figure 11**. The plot shows that for high-*k* gate dielectric TFET, the threshold voltage rises with an increase in temperature, whereas for low-*k* dielectric, the threshold voltage remains almost constant. The simulated values of threshold voltage have been derived using linear extrapolation method of determining threshold voltage. The method involves the construction of a tangent at the point on the

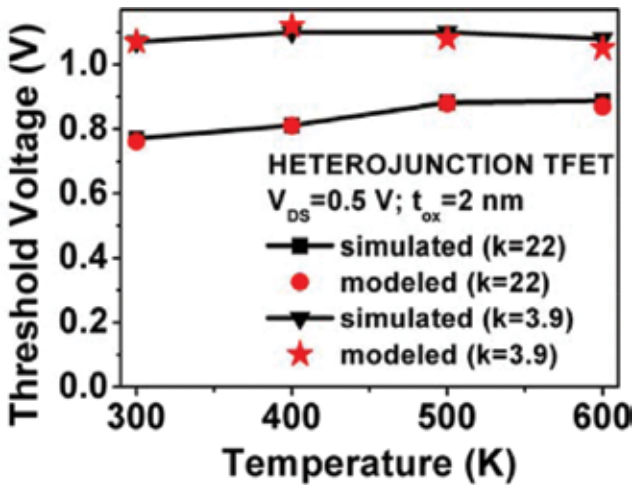

Figure 11. A plot of threshold voltage versus temperature for dielectric constants, 3.9 and 22.

transfer characteristics where the transconductance is maximum. The value at which the tangent intersects the gate voltage axis is taken to be the threshold voltage.

6. Conclusion

This chapter has presented a comprehensive evaluation of a bandgap-modulated UL-HTFET. The simulation analyses have examined the different electrical parameters and their dependence on the pocket length, mole fraction of the SiGe layer, and gate voltage. An impressive on-off current ratio of $>10^{12}$ and a subthreshold swing less than 60 mV/dec are observed. An analytical model based on 2-D Poisson equation has been developed for the gate-drain underlap heterojunction TFET. The modeled values of surface potential, electric field, and drain current satisfy the results of the simulation. Furthermore, a temperature-dependent algorithm has been discussed to extract threshold voltage in heterojunction TFETs, and a validation has been presented for the plot of threshold voltage at different temperatures.

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Author details

Brinda Bhowmick[1]* and Rupam Goswami[2]

*Address all correspondence to: brindabhowmick@gmail.com

1 Department of Electronics and Communication Engineering, National Institute of Technology Silchar, Silchar, Assam, India

2 Kalinga Institute of Industrial Technology, Bhubaneswar, Odisha, India

References

[1] Choi WY, Park B-G, Lee JD, Liu T-JK. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. IEEE Electron Device Letters. 2007;**28**(8): 743-745. DOI: 10.1109/led.2007.901273

[2] Royer CL, Mayer F. Exhaustive experimental study of tunnel field effect transistors (TFETs): From materials to architecture. In: 10th International Conference on Ultimate Integration of Silicon 2009; 18–20 March 2009. Aachen: IEEE; 2009. pp. 53-56. DOI: 10.1109/ulis.2009.4897537

[3] Ahish S, Sharma D, Kumar YBN, Vasantha MH. Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping. IEEE Transactions on Electron Devices. 2016;**63**(1):288-295. DOI: 10.1109/ted.2015.2503141

[4] Tamersit K, Djeffal F. Double-gate graphene nanoribbon field-effect transistor for DNA and gas sensing applications: Simulation study and sensitivity analysis. IEEE Sensors Journal. 2016;**16**(11):4180-4191. DOI: 10.1109/jsen.2016.2550492

[5] Goswami R, Bhowmick B. An analytical model of drain current in a Nanoscale circular gate TFET. IEEE Transactions on Electron Devices. 2017;**64**(1):45-51. DOI: 10.1109/TED.2016.2631532

[6] Zhao Q-T, Richter S, Schulte-Braucks C, Knoll L, Blaeser S, Luong GV, et al. Strained Si and SiGe nanowire tunnel FETs for logic and analog applications. IEEE Journal of the Electron Devices Society. 2015;**3**(3):103-114. DOI: 10.1109/jeds.2015.2400371

[7] Boucart K, Ionescu A. Double gate tunnel FET with ultrathin silicon body and high-k gate dielectric. In: Proceedings of the European Solid-State Device Research Conference. 2006; 19–21 Sept. Vol. 2006. Montreux, Switzerland: IEEE; 2007. pp. 1725-1733. DOI: 10.1109/essder.2006.307718

[8] Saurabh S, Kumar MJ. Novel attributes of a dual material gate Nanoscale tunnel field-effect transistor. IEEE Transactions on Electron Devices. 2011;**58**(2):404-410. DOI: 10.1109/ted.2010.2093142

[9] Choi WY, Lee W. Hetero-gate-dielectric tunneling field-effect transistors. IEEE Transactions on Electron Devices. 2010;**57**(9):2317-2319. DOI: 10.1109/ted.2010.2052167

[10] Dewey G, Chu-Kung B, Boardman J, Fastenau JM, Kavalieros J, Kotlyar R, et al. Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing. International Electron Devices Meeting. 2011; 5–7 Dec. 2011. Washington, DC, USA: IEEE; 2012. p. 33.6.1-33.6.4. DOI: 10.1109/iedm.2011.6131666

[11] Synopsys. Sentaurus device user guide. Mountain view. In: CA. 2011

[12] Bagga N, Sarkar SK. An analytical model for tunnel barrier modulation in triple metal double gate TFET. IEEE Transactions on Electron Devices. 2015;**62**(7):2136-2142. DOI: 10.1109/ted.2015.2434276

[13] Dash S, Mishra G. A new analytical threshold voltage model of cylindrical gate tunnel FET (CG-TFET). Superlattices and Microstructures. 2015;**86**:211-220. DOI: 10.1016/j.spmi.2015.07.049

[14] Lee MJ, Choi WY. Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs). Solid-State Electronics. 2011;**63**(1):110-114. DOI: 10.1016/j.sse.2011.05.008

[15] Vishnoi R, Kumar MJ. Compact analytical drain current model of gate-all-around nanowire tunneling FET. IEEE Transactions on Electron Devices. 2014;**61**(7):2599-2603. DOI: 10.1109/ted.2014.2322762

[16] Goswami R, Bhowmick B, Baishya S. Physics-based surface potential, electric field and drain current model of a δp^{+} $Si_{1-x}Ge_{x}$ gate–drain underlap nanoscale n-TFET. International Journal of Electronics. 2016;**103**(9):1566-1579. DOI: 10.1080/00207217.2016.1138514

[17] Goswami R, Bhowmick B. A temperature-dependent surface potential-based algorithm for extraction of threshold voltage in homojunction TFETs. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields. 2017 Jul. DOI: 10.1002/jnm.2304

Chapter 4

Room-Temperature Terahertz Detection and Imaging by Using Strained-Silicon MODFETs

Juan Antonio Delgado-Notario, Vito Clericò, Kristel Fobelets, Jesús Enrique Velázquez-Pérez and Yahya Moubarak Meziani

Additional information is available at the end of the chapter

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Abstract

This chapter reports on an experimental and theoretical study of Schottky-gated strained-Si modulation-doped field-effect transistors (MODFETs) with different sub-micron gate lengths (100, 250, and 500 nm). Room-temperature detection of terahertz (THz) radiation by the strained-Si MODFETs was performed at two frequencies (0.15 and 0.3 THz). A technology computer-aided design (TCAD) analysis based on a two-dimensional hydrodynamic model (HDM) was used to investigate the transistor response to THz radiation excitation. TCAD simulation was validated through comparison with DC and low-frequency AC measurements. It was found that the photoresponse of the transistors can be improved by applying a constant drain-to-source bias. This enhancement was observed both theoretically and experimentally. The HDM model satisfactorily describes the experimental dependence of the photoresponse on the excitation frequency, the gate bias, and the drain-to-source current bias. The coupling of the incoming THz radiation to the MODFETs was studied at 0.15 and 0.3 THz. Finally, to demonstrate the suitability of strained-Si MODFET for terahertz applications, an image sensor within a pixel-by-pixel terahertz imaging system for the inspection of hidden objects was used.

Keywords: strained silicon, MODFETs, THz, plasma waves, TCAD, imaging, detectors

1. Introduction

The demand to substantially improve electron mobility in Si-based field effect transistors (FETs) led to the development of $Si/Si_{1-x}Ge_x$ MODFETs (modulation-doped field-effect transistor).

A MODFET is based on a single or a double heterojunction of two semiconductors with different bandgaps. In an n-channel MODFET, electrons diffuse from a highly doped layer toward a lowly doped layer of a high-mobility material where they are confined by means of the conduction-band discontinuity between the two materials. These electrons form a two-dimensional electron gas (2DEG) conductive channel at the heterointerface. Single-device strained $Si/Si_{0.6}Ge_{0.4}$ MODFETs with 100-nm T-gates with up to 74-GHz current gain cutoff frequency and 107-GHz maximum oscillation frequency were demonstrated [1].

The terahertz (THz) region (~0.1–10 THz; ~0.03–3 mm; ~3–300 cm^{-1}) lies in the gap between the microwaves and infrared regions of the electromagnetic (EM) spectrum. THz radiations have extraordinary properties; it is a non-ionizing radiation and it is capable of penetrating through many non-conductive materials [2]. THz radiations have shown a great potential in a huge range of THz applications including astronomy [3, 4], spectroscopy (rotational, vibrational, and translational modes in the THz range are specific to a particular substance allowing to obtain a THz fingerprint) [5–7], thickness measurement of multilayer objects [8], communications with a bandwidth significantly higher than those based on microwaves [9], nondestructive inspection based on both imaging of concealed objects and spectroscopy [10], metrology [11], quality control [12], and so on. THz rays (T-rays) permit imaging with a diffraction-limited resolution similar to that of the human eye [13], and, since common optically opaque packaging materials are transparent to T-rays, the inspection of concealed objects is possible.

During the last decade, new promising 2D materials have recently attracted interest to develop room-temperature solid-state THz sensors [14]. However, so far, only devices based on III–V materials [15] and silicon [16] have proved experimentally their potential to build low-cost, compact, scalable, and reliable systems; accordingly, the extension of the frequency range of these devices generates a great interest in THz detection.

Solid-state devices are rising as one of the most promising ways to obtain THz detection and emission at room temperature. Dyakonov and Shur proposed in [17–19] the use of field-effect transistors (FETs) as detectors, multipliers, and mixers in the THz range using the oscillations of the plasma waves in the channel. Nonlinear properties of the two-dimensional plasma permit the detection of the THz radiation. Plasma wave-based detectors can directly convert the incoming EM radiation into measurable voltage or current. They demonstrated that a FET under excitation by THz radiation generates a DC drain-to-source voltage when the drain is open and, therefore, operating in the photovoltaic-mode detection. The value of this voltage can be modulated by the gate-to-source bias voltage, as the gate bias controls the plasma density and therefore the carrier concentration in the FET channel. The increasing availability of continuous-wave compact sources based on solid-state oscillators in the millimeter-wave range raises the interest on the development of direct detectors [20].

This chapter presents a study of room-temperature terahertz detection using strained-silicon modulation field-effect transistors with three different gate lengths. Detection of THz radiation [21, 22] and imaging using Si/SiGe transistors have been previously demonstrated [23, 24]. A main distinct interest of the high-mobility n-type FETs based on the Si/SiGe system is that, unlike the ones based on III–V plasmon detectors, it will be easy to integrate MODFET THz detectors with mainstream Si technology circuits, since both are fabricated on conventional

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Si wafers. Therefore, strained-Si MODFETs can lead to single-chip high-performance THz (basic analog building blocks were already demonstrated using Si/SiGe FETs [25]) and guide to future compact, low-cost, high-speed, and high-precision THz detectors.

2. Device description and TCAD simulations

2.1. Strained-silicon MODFET

The devices under study are based on the Si/SiGe system, and the layout of the transistors is shown in **Figure 1(a)**. The epistructure of the MODFETs used in this work is as follows: a thick relaxed linearly graded SiGe virtual substrate is grown over a p-doped conventional Si wafer. The final top Ge molar concentration in the virtual substrate was 0.3. The structure has an undoped 12-nm tensile strained Si channel, sandwiched between two n-doped $Si_{0.70}Ge_{0.30}$ relaxed supply layers (reddish layers) to generate a high density of electrons in the strained-Si quantum well [26, 27]. The highlighted bluish layer marks out the strained-Si quantum well. Pt/Au was evaporated to fabricate the Schottky gate that was not symmetrically placed between the source and the drain. A more detailed description of the transistor fabrication can be found in [26].

The material system Si/SiGe allows the creation of a thin layer of strained silicon under tetragonal (biaxial tensile) strain due to the different values of the Si and the SiGe lattice constants. Tetragonal strain has the effect of lifting the sixfold degeneracy of the conduction band in

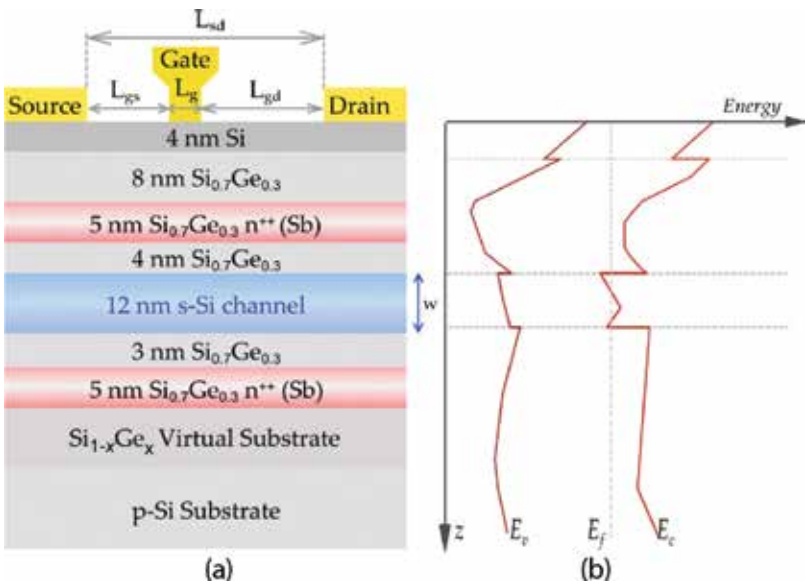

Figure 1. (a) Epistructure of the Si/SiGe MODFETs showing the vertical layout of the transistors. (b) Conduction and valence band profiles and the Fermi level under the gate in equilibrium [26].

silicon into a twofold and fourfold degenerate sets lowering the energy of the two valleys with their long axis perpendicular to the Si/SiGe interface. Consequently, the strained-Si gap is reduced as well as the electron conductivity mass as compared to bulk as a lower value, leading to an enhancement of the electron mobility by a factor of 2 [28, 29]. Since intervalley carrier scattering may only occur between degenerate minima, electrons in a layer of (tensile)-strained silicon would undergo a lower number of intervalley scattering events per unit time than in bulk silicon. The combination of the effect pointed earlier makes tensile strained silicon devices excellent candidates to build the high-mobility FET channel that is necessary to detect THz radiation. The energy band diagram at zero voltage is presented in **Figure 1(b)** [26]. The value of the conduction band offset of the heterojunction $Si/Si_{0.70}Ge_{0.30}$ is about 180 meV, ensuring an excellent electron confinement in the strained-Si quantum well layer that is necessary for room-temperature high-mobility operation of the detector. **Table 1** summarizes the geometrical parameters and the value of the threshold voltage of the strained-Si MODFETs under study.

The channel's length (L_{DS}) and width (W_G) were kept constant for all devices (L_{DS} = 2 μm, W_G = 30 μm). However, the gate lengths of the transistors were varied. Transistors with 100-, 250-, and 500-nm gate lengths were characterized. The gates were asymmetrically placed between the source (S) and the drain (D) contacts in all transistors; the distance between the right edge of the source and the left edge of the gate (L_{GS}) was equal to 1 μm for all the transistors (**Table 1**). An asymmetrical position of the gate is of interest to enhance THz detection by the transistor [30]. Measuring devices with different values of the gate length allows the study of the influence of the gate length on the performance of the transistors as THz

	L_{DS} (μm)	L_{GS} (μm)	L_G (nm)	W_G (μm)	V_{th} (V)
Device 1 (D1)	2	1	100	30	−0.75
Device 2 (D2)	2	1	250	30	−0.67
Device 3 (D3)	2	1	500	30	−0.62

Table 1. Geometrical and electrical parameters of the strained-Si MODFETs under study.

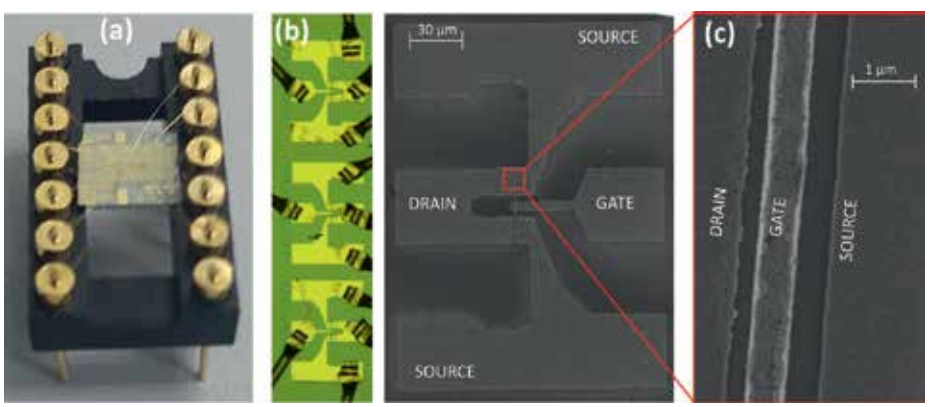

Figure 2. Strained-Si MODFETs under study mounted and bounded on a DIP14 (a) and their optical microscope image (b). (c) SEM image of device 3 (500-nm T-gate transistor).

detectors and on the coupling of the incoming THz radiation. Strained-Si MODFETs were mounted and wire-bonded on the same dual in-line package (DIP14) shown in **Figure 2(a)**. An optical microscope image of the three different devices under study is given in **Figure 2(b)**. A SEM image of D3 with L_G = 500 nm is shown in **Figure 2(c)**.

2.2. TCAD modeling

Dyakonov and Shur obtained an analytical solution of the unidimensional Euler equation that demonstrated the ability of the plasma waves in FET channels [17–19] to generate and detect THz radiation. A single equation cannot account for important parameters (such as doping profiles, high electric fields that locally modify the carrier mobility, device geometry, etc.) that condition the performance of the FET as a THz detector.

A better description of the charge transport in a transistor may be achieved through the numerical solution of the drift-diffusion model (DDM) that consists of the Poisson equation (Eq. (1)) and the continuity equations for electrons (Eq. (2)) and holes (Eq. (3)) [31]:

$$\nabla^2 \varphi = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^-\right) \tag{1}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\left(\vec{\nabla} \cdot \vec{J_n}\right) - U_n \tag{2}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\left(\vec{\nabla} \cdot \vec{J_p}\right) - U_p \tag{3}$$

where ϕ is the electric potential, q is the absolute value of the electron charge, n/p is the electron/hole concentration, N_D^+ (N_A^-) is the ionized donor (acceptor) concentration, ε is the local material permittivity, and U_n (U_p) represents the net electron (hole) recombination rate. $\vec{J}_n$ ($\vec{J}_p$) is the current density of electrons (holes) in the drift-diffusion model given by the following equations:

$$\vec{J_n} = q\,\mu_n(u_n)\left[n\vec{E} + \vec{\nabla}(u_n n)\right] \tag{4}$$

$$\vec{J_p} = q\,\mu_p(u_p)\left[n\vec{E} + \vec{\nabla}(u_p p)\right] \tag{5}$$

where $\vec{E}$ is the electric field, μ_n (μ_p) is the electron (hole) mobility, and u_n (u_p) is the electron (hole) thermal voltage. In deep-submicron FETs, the drain and gate biases give rise to large electric fields that rapidly change over small length scales giving leading to nonlocal phenomena that dominate the transistor performance [26, 27]. As carriers are intensely heated by the electric field in the channel of deep-submicrometer FETs, energy balance equations accounting for electron and hole heating and energy relaxation in the device must be self-consistently added to the transport model. The DDM only considers moment relaxation [32], and therefore it is unable to describe a hot carrier transport. As channel mobility is closely dependent on the

carrier temperature, an extended model needs to be used to study the electric properties of deep-submicron FET transistors used in plasma wave THz detection. This extended model is known as the hydrodynamic model (HDM).

The HDM [32, 33] includes a carrier energy balance by coupling to the set of DDM equations and the electron and hole energy flow densities that are given as follows:

$$\vec{\nabla} \cdot \overrightarrow{S_n} = \frac{1}{q}\overrightarrow{J_n} \cdot \vec{E} - \frac{3}{2}\left(n\frac{u_n - u_0}{\tau_n} + \frac{\partial(u_n n)}{\partial t}\right) \tag{6}$$

$$\vec{\nabla} \cdot \overrightarrow{S_p} = \frac{1}{q}\overrightarrow{J_p} \cdot \vec{E} - \frac{3}{2}\left(p\frac{u_p - u_0}{\tau_p} + \frac{\partial(u_p p)}{\partial t}\right) \tag{7}$$

where $\overrightarrow{S_n}$ ($\overrightarrow{S_p}$) is the electron (hole) energy relaxation time, u_n (u_p) is the electron (hole) thermal voltage, and the electric field that is self-consistently obtained from the Poisson equation.

Strained-Si MODFET is essentially a majority carrier device; then the hole energy balance equation (Eq. (7)) was disregarded in the model. In this work, a two-dimensional HDM (Eqs. (1)–(6)) was used. It was implemented with Synopsys TCAD [34]. Carrier relaxation times were obtained from uniform-field Monte Carlo simulations [35, 36]. In TCAD simulations, impurity de-ionization, Fermi-Dirac statistics, and mobility degradation due to both longitudinal and transverse electric field were considered. All TCAD simulations were carried out at room temperature.

The geometry and dimensions used in the simulations are the ones shown in **Figure 1(a)**. The doping level of the supply layers was 10^{19} cm^{-3} for the upper supply layer and 1.8×10^{18} cm^{-3} for the lower one. The thicknesses of the virtual substrate and the p-Si wafer were chosen to be 600 and 500 nm, respectively, to economize computer memory. A uniform residual n-type-doping density of 10^{15} cm^{-3} was assumed in the non-intentionally doped regions of the transistor. Under both source and drain contacts, highly doped regions were considered to ensure ensure low values of contact resistance for the ohmic contacts of the device. The values of the conduction and valence bands offsets between the strained-Si and the relaxed $Si_{1-x}Ge_x$ as a function of the Ge molar fraction (x = 0.30) were extracted from [37]. Low electric field mobility in the channel was modeled using Roldan's model for biaxially strained Si on relaxed SiGe [38], and the maximum value electron mobility in the channel was 1600 cm^2/(Vs).

3. THz setup

Static (DC) and THz measurements were carried out at room temperature. On-wafer, DC measurements of drain-to-source current versus drain-to-source and gate-to-source bias voltages were done using a Cascade 11000B probe station and an Agilent B1500A semiconductor parameter analyzer. **Figure 3** shows a photograph with a schematic of the experimental setup used for the terahertz characterization of the strained-Si MODFETs. A solid-state harmonic generator THz source based on a dielectric resonator oscillator (DRO) at 12 GHz and electronic

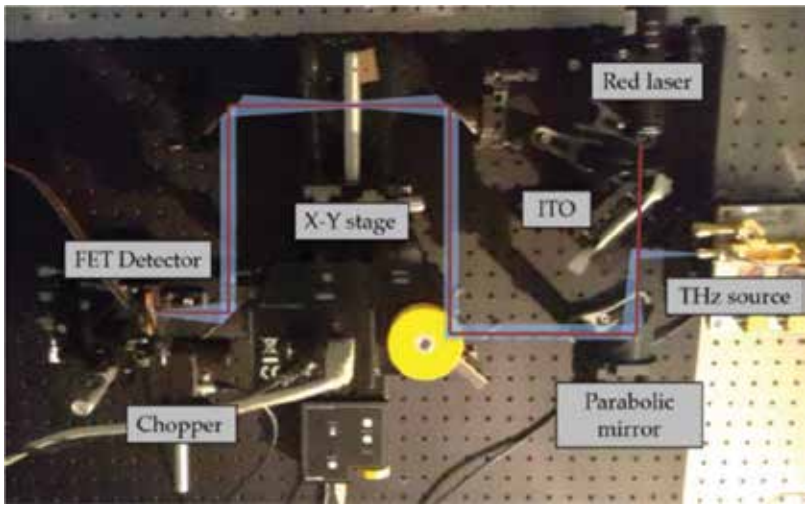

Figure 3. Photograph of the experimental setup and schematic description of the THz (blue) and red laser (red line) beams.

multiplication to reach 0.15 THz with a power of 3 mW and 0.3 THz with a power of 6 mW was used to excite the transistors. The output power was measured close to the source using a highly sensitive calibrated pyroelectric detector. The incoming THz radiation was modulated by a mechanical chopper between 0.233 and 5 kHz, collimated and focused by an indium tin oxide (ITO) mirror and off-axis parabolic and plane mirrors. A red LED (or laser) was used for the alignment of the THz beams.

The photo-induced drain-to-source voltage, ΔU, was measured using a lock-in technique. Finally, a X-Y stage was used to generate pixel-by-pixel THz images.

4. Results and discussion

4.1. DC characterization

Transfer characteristics of Device 3 are shown in **Figure 4(a)** for two values, 20 and 200 mV, of the drain-to-source voltage (V_{DS}). The three transistors are depletion-mode devices, so a negative bias voltage must be applied to the gate (i.e., a negative gate-to-source voltage) to cut off the c hannel [25, 39]. Transfer characteristics in a log scale show that a total switch-off of the device was not possible, and a constant level of drain current (I_{DS}) persists for a gate bias of −1 V (8 μA for V_{ds} = 20 mV and 80 μA for V_{ds} = 200 mV). As the drain voltage is moderately raised from 20 to 200 mV, the above-described behavior is enhanced, and the sub-threshold current at V_{GS} = -1 V increases when V_{DS} increases. As pointed out earlier, this behavior reveals a moderate control of the channel by the gate electrode due to the double supply layer; in return, this double deck ensures a suitable concentration of the electron plasma in the channel that is of paramount importance to achieve a good performance of the transistor in THz detection.

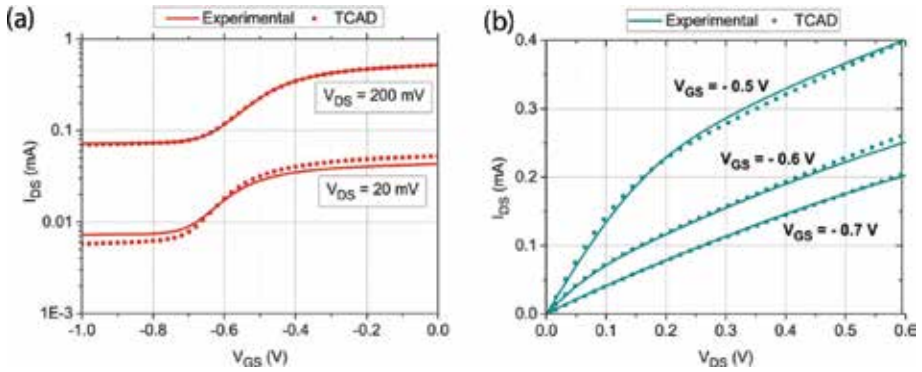

Figure 4. (a) Experimental and simulated transfer characteristics for device 3 for two values of the drain voltage plotted in a log scale and (b) output characteristics for three different values of V_{GS}.

The TCAD simulation model of the transistor was validated through comparison with DC and AC measurements. The agreement between TCAD and experimental results across the whole ranges of gate-to-source and drain-to-source biases studied is excellent as shown in **Figure 4**.

Agreement between measurement and simulation magnitudes involving first derivatives of the drain current was also analyzed. In the first place, the efficiency of the transconductance was analyzed. This magnitude defined as the ratio of transconductance (g_m) to drain-to-source DC current (I_{DS}), is a key parameter used to compare the performance of different technologies of transistors. The efficiency of the transconductance is used here, on the one hand, because it clearly shows the operation region of the device and, on the other hand, because the efficiency of the transconductance is linearly dependent on a current derivative and discrepancies between simulation and experimental results are readily revealed. **Figure 5(a)** gives the experimental and calculated efficiency of the transconductance versus the gate voltage (V_{GS}) of the device D3. The maximum value of the efficiency of the transconductance measured

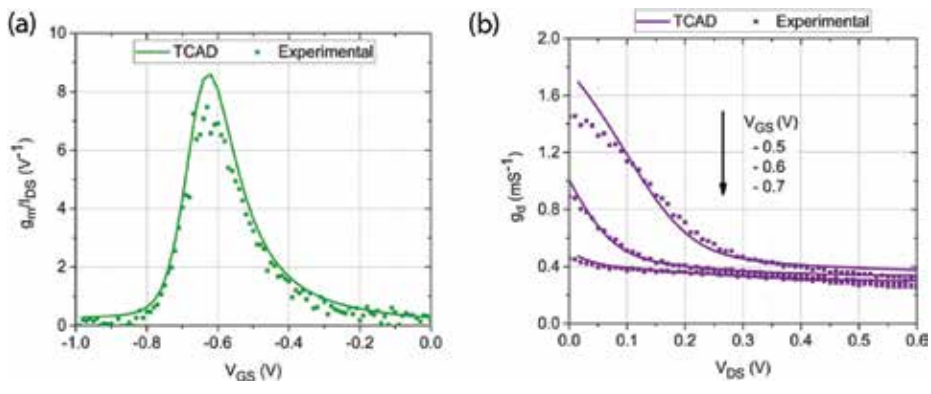

Figure 5. (a) Efficiency of the transconductance versus the gate voltage obtained from measurements and numerical TCAD simulations and (b) drain conductance versus drain voltage for three different values of gate bias obtained from measurements and numerical TCAD simulations.

and obtained from TCAD simulations (<10 V^{-1}) is significantly lower than the theoretical limit (38 V^{-1}), along with the above-discussed behavior of the transconductance, suggesting that further improvements of the transistor performance may be achieved by an optimization of the layout of the structure.

In the second place, the drain conductance that gives the first derivative of the drain current with respect to the drain current was also determined. **Figure 5(b)** shows drain conductance as a function of drain voltage for three different gate voltages (−0.5, −0.6, and −0.7 V). Experimental and TCAD drain conductance curves show an excellent agreement between measurements and TCAD simulations.

4.2. THz detection: TCAD versus experimental

A TCAD study of the THz photovoltaic response of the transistor was implemented, as in measurements, grounding the source, biasing the gate, and floating the drain contact while a THz small sinusoidal signal (0.15 or 0.3 THz) was superimposed to the gate voltage as described in [17–19]. As the DC drain voltage setup in the photovoltaic mode must be supported by a net charge in the drain region, in TCAD simulations, a charge boundary condition was implemented at the floating drain contact with a distributed boundary condition over all nodes of the mesh of the drain electrode. The boundary condition is as follows:

$$\oint \vec{D} \cdot \overrightarrow{dS} = Q \tag{8}$$

where $\vec{D}$ is the electric displacement field, Q is the total net charge, and the integral is evaluated over the entire surface of the drain electrode. Eq. (8) forces the potential on the drain (i.e., the photoresponse of the detector) to be adjusted to produce the correct total charge on the electrode. HDM equations (Eqs. (1)–(6)) were solved in the time domain to obtain the transistor photoresponse. The amplitude of the sinusoidal signal superimposed in the gate contact was fixed to an arbitrary value of 5 mV. Since this value is arbitrary, the magnitude of the THz response obtained in simulations will be presented henceforward as arbitrary magnitude in figures.

In TCAD simulations, it was found that the drain voltage (ΔU) induced by the THz sinusoidal signal exhibits both the same shape (sinusoidal) and the frequency than the AC signal superimposed to the gate bias; this ensures that no frequency conversion takes place in the simulated devices. In addition, it was found that its amplitude is considerably smaller than one of the gate's signal in agreement with the fact that in the THz range the transistor is unable to amplify signals and it is merely working as a THz detector. The mean value of the induced drain voltage by the radiation was negative as predicted by theoretical models [17–19]. The photoresponse obtained in TCAD simulations was extracted by subtracting the value of drain-to-source voltage when the THz signal was applied ($\Delta U_{THz\text{-}on}$) from the drain-to-source voltage when no signal was applied ($\Delta U_{THz\text{-}off}$):

$$\Delta U = \Delta U_{THz-off} - \Delta U_{THz-on} \tag{9}$$

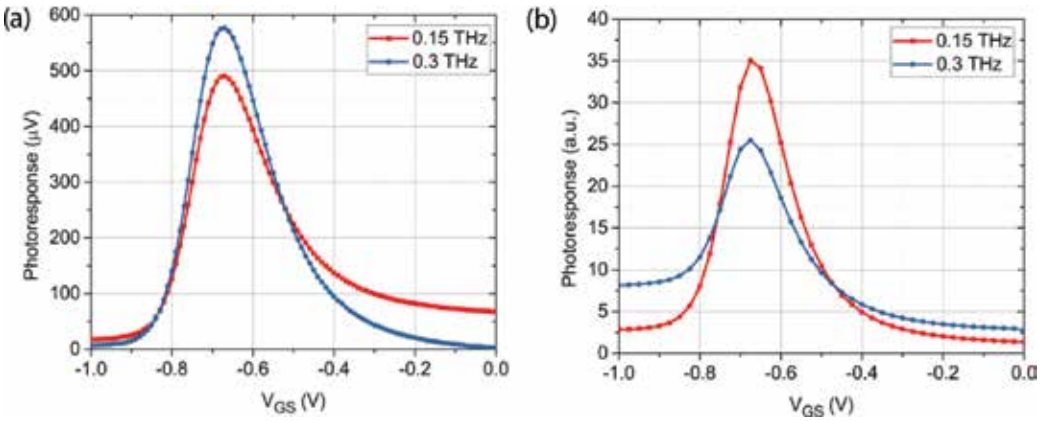

Figure 6. Measured (a) and TCAD simulation (b) photoresponse versus gate voltage under excitation of 0.3 (blue dots) and 0.15 THz (red squares) of D2.

Figure 6 gives the room-temperature photovoltaic response of device D2 with L_G = 250 nm obtained experimentally and from TCAD simulations at 0.3 (blue squares) and 0.15 THz (red dots).

The higher value in the photoresponse was found when the gate electrode was voltage-biased at a voltage close to the threshold voltage of the transistor [40]. This behavior has been observed earlier in FETs [16, 20] and it was attributed to a non-resonant (broadband) response of the detector. It is related to over-damping of the plasma waves in the channel where the AC current generated by the incoming radiation at the source cannot reach the drain side of the channel. A theoretical study of the photoresponse in this regime is presented in [21, 22]. The quality factor [19] is given by: $Q = \omega\tau$, where τ is the relaxation time given by $m^*\mu/e$ (m^*: the electron effective mass, μ: the electron mobility, and e: the absolute value of the electron charge). In the present case, the devices show a higher channel mobility (~1600 $cm^2/V{\cdot}s$) as compared to the conventional Si-MOSFET (~200 $cm^2/V.s$); the value of the quality factor was estimated to be 0.14 at f = 0.15 THz and ~0.29 at f = 0.3 THz; any of these values fulfills the resonance condition. The experimental photoresponse (**Figure 6(a)**) is more intense under excitation at 0.3 THz than at 0.15 THz. The photoresponse obtained in TCAD simulations exhibits the opposite behavior: the photoresponse at 0.15 THz is more intense than at 0.3 THz. This must be partly attributed to the fact that in measurements, the source's output power at 0.3 THz is twice than at 0.15 THz. Moreover, the coupling of the THz radiation to the devices could vary at 0.15 and 0.3 THz. These possibilities will be explored and further discussed subsequently. As in TCAD simulations, the amplitude of the sinusoidal gate signal was fixed to 5 mV for both frequencies, and no coupling and/or effects related to the differences in the incoming THz power at both frequencies can be found.

Besides the photovoltaic mode, the efficiency of the detector can be improved, creating additional asymmetries between the drain and the source [30, 41, 42]. One method to generate these asymmetries is to apply a DC current between the drain and the source ($I_{DS} > 0$). **Figure 7** shows the photoresponse obtained experimentally and from TCAD simulations when a drain-to-source current bias, I_{DS} = 50 μA, is imposed to the transistor D1 at 0.15 and at 0.3 THz.

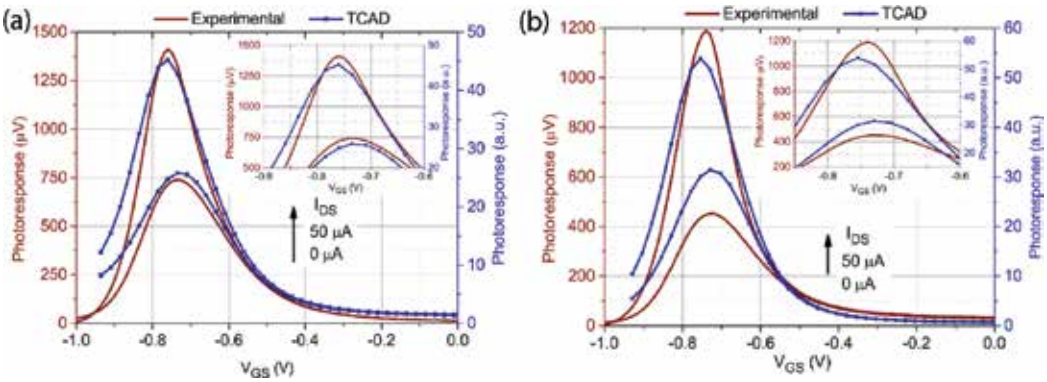

Figure 7. Photoresponse versus gate voltage measured experimentally (red color) and obtained from TCAD simulations (blue color) for different values of I_{DS} at 0.3 (a) and 0.15 THz (b) for D1. The insets show a zoom of the region of maximum photoresponse.

The main effect of imposing a DC source-to-drain current bias is that THz detection is significantly enhanced, and the photoresponse grows when the bias current is increased. The bias current introduces an additional asymmetry between the source and the drain, creating a depletion of the electron density on the drain side of the channel, and consequently, the maximum value of the photoresponse is increased [24, 41, 42]. Moreover, a noticeable additional effect (the insets in **Figure 7**) is that the maximum in the photoresponse is shifted toward more negative values of the gate voltage. **Figures 6** and **7** show that the MODFET photoresponse exhibits the same dependence with respect to the gate bias voltage both in measurements and in simulations. An excellent agreement between TCAD and experimental results is found in the photovoltaic mode ($I_{DS} = 0$) and even when a bias current (I_{DS}) is applied to the transistor. Therefore, the measured photoresponse of the strained-Si MODFET must be mainly attributed to the plasmonic response of the channel carriers rather than to the antenna role played by bonding wires or metal pads as simulations reproduce correctly the experimental photoresponse.

In addition, to the abovementioned channel asymmetry created by the current bias, a built-in asymmetry can be introduced geometrically by imposing an asymmetric design of the contact pads of the transistor. **Figure 8** shows the obtained photoresponse from TCAD simulations as a function of the asymmetry factor. The latter is defined as the ratio L_{GS}/L_{GD}, where L_{GS} is the distance between the right edge of the source and the left edge of the gate and L_{GD} is the distance between the right edge of the gate and the left edge of the drain (**Figure 1(a)**). $L_{GS}/L_{GD} = 1$ means that the transistor is symmetric. The gate length was kept constant at 500 nm for all the transistors.

A higher photoresponse signal was obtained for an asymmetry factor of 0.2 where the gate finger is very close to the source contact. However, in the opposite case, when the finger is close to the drain pad, no enhancement of the photoresponse was obtained. In the non-resonant regime, the oscillation of the plasma occurs close to the source pad where the electrons are injected into the channel and hence the gate finger close to the source pad could control efficiently the damped oscillation of the plasma waves. We conclude that for a better performance, asymmetry should be introduced as close as possible to the source pad.

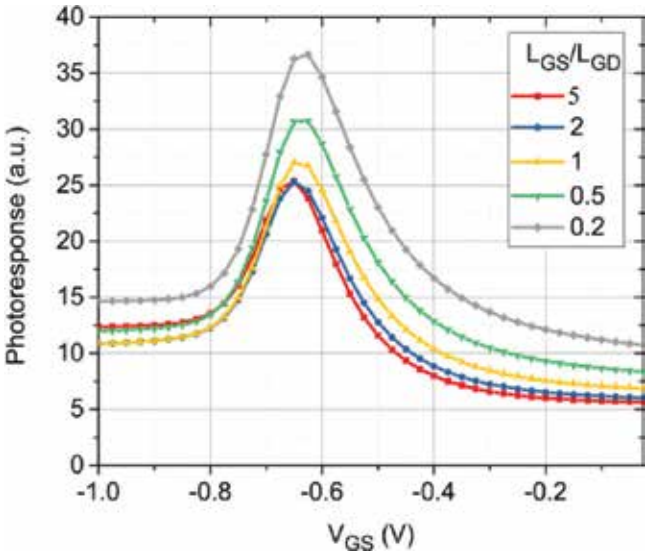

Figure 8. Photoresponse obtained from TCAD simulations versus V_{GS} for different horizontal positions of the gate contact.

4.3. Polarization sensitivity of photoresponse

It can be observed in **Figures 6(a)** and **7** that the obtained photoresponse is more intense under excitation at 0.3 than at 0.15 THz. This must be partly attributed to the higher power at 0.3 THz (~6 mW) than at 0.15 THz (~3 mW) and to the coupling of the THz radiation to the device that varies with frequency. Moreover, the bonding wires and the metallic pads could play an antenna role to couple the incoming terahertz radiation (linearly polarized) to the 2D electron channel [43–45]. To understand how radiation is coupled, devices were rotated in the plane perpendicular to the terahertz beam, and the photoresponse signal was measured for

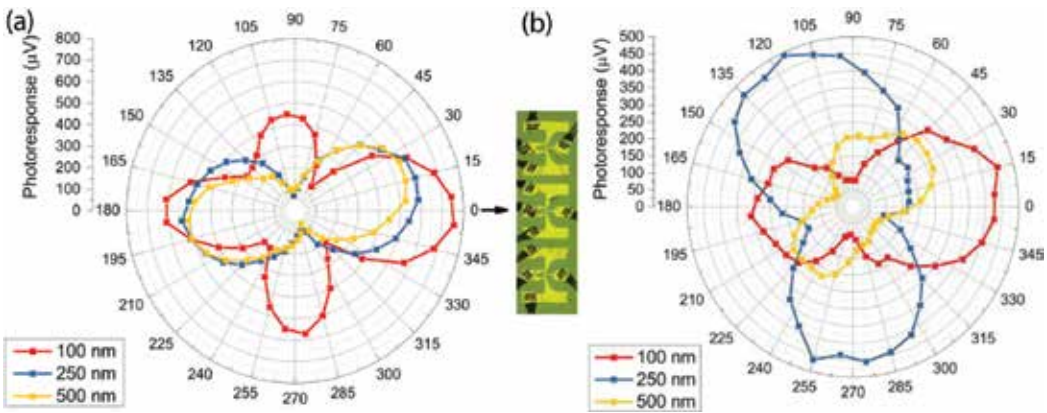

Figure 9. Photoresponse versus rotation angle for all devices under excitation of 0.3 (a) and 0.15 THz (b). The inset figure shows the devices at the zero-angle position.

each angular position of the devices. **Figure 9** shows the photoresponse signal as a function of the polarization of the incoming THz radiation for 0.3 (a) and 0.15 THz (b).

For all the devices at 0.3 THz, a maximum of the photoresponse signal was found when the incoming radiation was parallel to the gate finger pads (see the inset of **Figure 9(a)** at 0°), showing a maximum photoresponse for all the devices at the same angular position. At 0.15 THz the maximum photoresponse was obtained at different angular positions for each device. It is clearly shown that at a lower frequency (0.15 THz), bounding wires play an important role to couple the terahertz radiation to the channel of the device. Moreover, at a higher frequency (0.3 THz), the coupling is performed by the contact pads and/or the gate fingers. These results are in agreement with previously published ones [46].

4.4. Responsivity, NEP, and imaging

Responsivity (R_V) and noise equivalent power (NEP) are the two key parameters (figures of merit) that determine the performance of THz detectors. Responsivity is calculated according to the expression:

$$R_V = \frac{\Delta U S_t}{P_t S_a} \frac{\pi}{\sqrt{2}} \tag{10}$$

where ΔU is the photoresponse signal measured with the lock-in amplifier, S_t is the radiation beam spot area, S_a is the active area of the transistor, and P_t is the total incident power surrounding the detector. The radiation beam power and spot area were measured using a calibrated pyroelectric detector at the MODFET position (see **Figure 3**); the P_t values were P_t = 0.5 mW at 0.15 THz and P_t = 1 mW at 0.3 THz. The spot area is given by πr^2 where r is the radius of the beam spot (≈1.5 mm at 0.3 THz and 3.3 mm at 0.15 THz). The area of each single transistor, including the contact pads, is less than 0.05 mm^2 (**Figure 2**), that is, it is much smaller than the diffraction limit area $S_\lambda = \lambda^2/4$. Accordingly, to calculate *Rv* in Eq. (6), *Sa* was replaced by S_λ to avoid overestimation of the *Rv* as well as NEP. The factor $\pi/\sqrt{2}$ originates from the Fourier transform of the square wave-modulated THz signal detected as RMS value with a lock-in.

The NEP is given by N_{th}/R_V, where N_{th} is the thermal noise of the transistor in V/Hz$^{0.5}$ and R_V is the responsivity in V/W. Since R_V and the NEP were studied at zero drain current bias, the thermal noise $N_{th} = (4kTR_{ds})^{0.5}$ is the only relevant source of noise of the transistor. Here, R_{ds} is the drain-to-source resistance that can be extracted from the transfer characteristics measured at a low drain bias (20 mV) corresponding to the linear regime (i.e., **Figure 5(a)**).

Figure 10 presents the responsivity and NEP curves for D1 with L_G = 100 nm at 0.15 and 0.3 THz. **Table 2** summarizes the obtained NEP and Rv for the Si-MODFETs at 0.15 and at 0.3 THz. Device 1, with the shorter gate, exhibits the best performance at 0.3 THz with R_V = 46.4 V/W and NEP ~0.12nW/Hz$^{0.5}$ and Device 2 exhibits the best performance at 0.15 THz with R_V = 74.5 V/W and NEP ~0.06 nW/Hz$^{0.5}$. This must be attributed to the large photoresponse signal provided by the Si/SiGe MODFET and to a better coupling of the incoming terahertz radiation. The values obtained for the NEP and the responsivity are comparable to

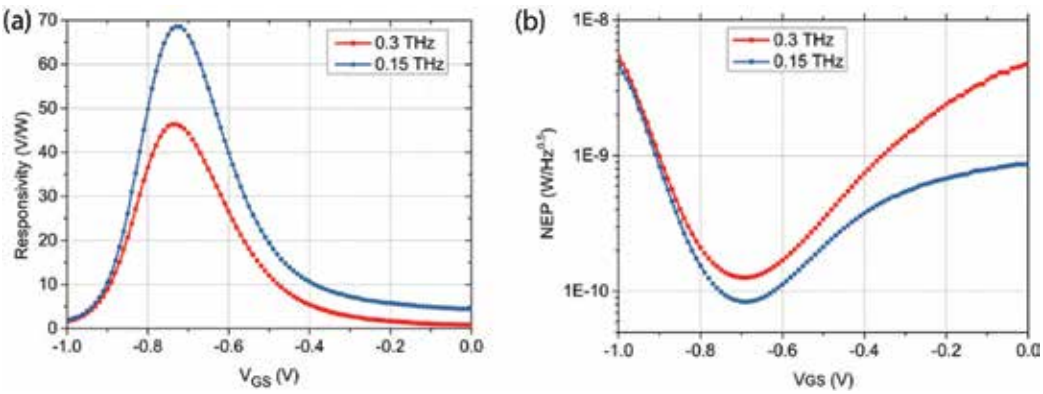

Figure 10. Responsivity (a) and NEP (b) measured under excitation of 0.15 (blue dots) and 0.3 THz (red squares) of the strained-Si MODFET with 100-nm gate length.

	0.15 THz		**0.3 THz**	
	R_V (V/W)	**NEP (nW/√Hz)**	**R_V (V/W)**	**NEP (nW/√Hz)**
Device 1	68.6	0.08	46.4	0.12
Device 2	74.5	0.06	36.2	0.13
Device 3	41.1	0.12	33.3	0.14

Table 2. Calculated NEPs and R_V for the different devices under studio.

the ones of commercial terahertz detectors at room temperature like Golay cells, pyroelectric detectors, and Schottky diodes [47]. However, the Si/SiGe MODFET presents the advantage of working at higher modulation frequencies as compared to other detectors.

To test the ability of the strained-Si MODFETs as detectors in THz imaging, a single transistor (D1) was used as the sensor in the terahertz imaging system shown in **Figure 3**. **Figure 11** shows the visible image of a standard copper RT/duroid® laminate where the logo of the Nanotechnology Group at Salamanca University has been etched (a) and its terahertz image at 0.3 THz (b) when it was wrapped around with a paper. THz radiation passes through in the regions were the metal layer was etched off and it is reflected in the regions covered with copper. A pixel-by-pixel image was taken using D1 as the detector; the gate of the transistor

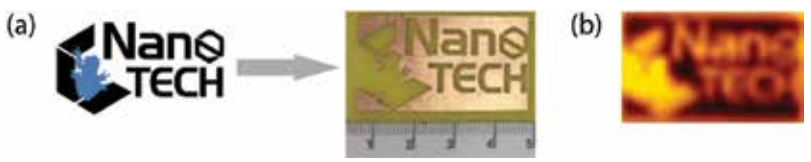

Figure 11. Visible (a) and 0.3 THz (b) images obtained at room temperature using the strained-Si MODFET with a shorter gate as sensor.

was biased around its threshold voltage to obtain a maximum intensity of the signal. The clear terahertz image obtained of the hidden object confirms the suitability of strained-Si MODFETs to be used as detectors to obtain high-quality THz images. Better resolution could be obtained at higher frequencies owing to its lower wavelength (λ <1 mm).

5. Conclusions

The potential of submicron gate length strained-Si MODFETs as detectors of terahertz radiation was demonstrated. A broadband (non-resonant) THz detection was observed under excitation of the transistors by a continuous-wave source at 0.15 and 0.3 THz. TCAD results obtained using a HDM model were in good agreement with the experimental ones in terms of both the excitation frequency and the gate-to-source bias. When imposing a source-to-drain current of 50 μA, both TCAD simulations and experiments show an increase of the photoresponse as compared to the photovoltaic mode. A theoretical study was performed to analyze the effect of gate's geometrical asymmetries on the THz detection. Coupling between THz radiation and strain-Si MODFETs channel was analyzed at 0.3 and 0.15 THz. It shows that the coupling is mainly performed by bonding wires at 0.15 THz. Finally, the strained-Si MODFET was used as a single pixel detector to obtain images of a concealed object at 0.3 THz.

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Author details

Juan Antonio Delgado-Notario[1]*, Vito Clericò[1], Kristel Fobelets[2],
Jesús Enrique Velázquez-Pérez[1] and Yahya Moubarak Meziani[1]

*Address all correspondence to: juanandn@usal.es

1 USAL NanoLab, University of Salamanca, Salamanca, Spain

2 Department of Electrical and Electronic Engineering, Imperial College, South Kensington Campus, London, UK

References

[1] Aniel F, Enciso-Aguilar M, Giguerre L, Crozat P, Adde R, Mack T, Seiler U, Hackbarth T, Herzog HJ, König U, Raynor B. High performance 100 nm T-gate strained Si/Si0.6Ge0.4 n-MODFET. Solid-State Electronics. 2003;**47**:283-289. DOI: 10.1016/S0038-1101(02)00208-3

[2] Rainsford T, Mickan SP and Abbott D. In T-Ray Sensing Applications: Review of Global Developments, Conference on Smart Structures, Devices, and Systems II; 13-15 December 2004; Sydney, Australia, 2005. pp. 826-838. DOI: 10.1117/12.607746

[3] Wiedner MC, Wieching G, Bielau F, Rettenbacher K, Volgenau NH, Emprechtinger M, Graf UU, Honingh CE, Jacobs K, Vowinkel B, Menten KM, Nyman LÅ, Güsten R, Philipp S, Rabanus D, Stutzki J, Wyrowski F. First observations with CONDOR, a 1.5 THz heterodyne receiver. Astronomy and Astrophysics. 2006;**454**:L33. DOI: 10.1051/0004-6361:20065341

[4] Siegel PH. Thz instruments for space. IEEE Transactions on Antennas and Propagation. 2007;**55**:2957-2965. DOI: 10.1109/TAP.2007.908557

[5] Clericò V, Delgado-Notario JA, Campos N, Gómez D, Diez E, Velazquez JE, Meziani YM. Terahertz spectroscopy of a multilayers flake of graphene. Journal of Physics: Conference Series. 2015;**647**:012040. DOI: 10.1088/1742-6596/647/1/012040

[6] Crowe TW, Globus T, Woolard DL, Hesler JL. Terahertz sources and detectors and their application to biological sensing. Philosophical Transactions of the Royal Society of London Series a-Mathematical Physical and Engineering Sciences. 2004;**362**:365-374. DOI: 10.1098/rsta.2003.1327

[7] Chen W, Peng Y, Jiang X, Zhao J, Zhao H, Zhu Y. Isomers identification of 2-hydroxyglutarate acid disodium salt (2hg) by terahertz time-domain spectroscopy. Scientific Reports. 2017;**7**:12166. DOI: 10.1038/s41598-017-11527-z

[8] Krimi S, Klier J, Jonuscheit J, Freymann G, Urbansky R, Beigang R. Highly accurate thickness measurement of multi-layered automotive paints using terahertz technology. Applied Physics Letters. 2016;**109**:021105. DOI: 10.1063/1.4955407

[9] Blin S, Teppe F, Tohme L, Hisatake S, Arakawa K, Nouvel P, Coquillat D, Penarier A, Torres J, Varani L, Knap W, Nagatsuma T. Plasma-wave detectors for terahertz wireless communication. IEEE Electron Device Letters. 2012;**33**:1354-1356. DOI: 10.1109/LED.2012.2210022

[10] Federici JF, Schulkin B, Huang F, Gary D, Barat R, Oliveira F, Zimdars D. THz imaging and sensing for security applications - explosives, weapons and drugs. Semiconductor Science and Technology. 2005;**20**:S266-S280. DOI: 10.1088/0268-1242/20/7/018

[11] Kleine-Ostmann T. In Thz metrology, 38th international conference on infrared, millimeter, and terahertz waves (IRMMW-THz); 01-06 September 2013; Mainz, Germany. DOI: 10.1109/IRMMW-THz.2013.6665913

[12] Ahi K, Shahbazmohamadi S, Asadizanjani N. Quality control and authentication of packaged integrated circuits using enhanced-spatial-resolution terahertz time-domain spectroscopy and imaging. Optics and Lasers in Engineering. 2017. DOI: 10.1016/j.optlaseng.2017.07.007

[13] Chan WL, Deibel J, Mittleman DM. Imaging with terahertz radiation. Reports on Progress in Physics. 2007;**70**:1325-1379. DOI: 10.1088/0034-4885/70/8/R02

[14] Wang M, Yang EH. THz applications of 2D materials: Graphene and beyond. Nano-Structures & Nano-Objects. 2017. DOI: 10.1016/j.nanoso.2017.08.011

[15] Hou HW, Liu Z, Teng JH, Placios T, Chua SJ. High temperature terahertz detectors realized by a GaN high electron mobility transistor. Scientific Reports. 2017;**7**:46664. DOI: 10.1038/srep46664

[16] Meziani YM et al. Non- resonant response to terahertz radiation by submicron cmos transistors. IEICE Transactions on Electronics. 2006;**E89C**:993-998. DOI: 10.1093/ietele/e89-c.7.993

[17] Dyakonov M, Shur M. Shallow-water analogy for a ballistic field-effect transistor - new mechanism of plasma-wave generation by dc current. Physical Review Letters. 1993;**71**:2465-2468. DOI: 10.1103/PhysRevLett.71.2465

[18] Dyakonov M, Shur M. 2-dimensional electronic flute. Applied Physics Letters. 1995;**67**:1137-1139. DOI: 10.1063/1.114986

[19] Dyakonov M, Shur M. Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid. IEEE Transactions on Electron Devices. 1996;**43**:380-387. DOI: 10.1109/16.485650

[20] Knap W, Deng Y, Rumyantsev S, Shur M. Resonant detection of subterahertz and terahertz radiation by plasma waves in submicron field-effect transistors. Applied Physics Letters. 2002;**81**:4637-4639. DOI: 10.1063/1.1473685

[21] Delgado-Notario JA, Meziani YM, Velazquez-Perez JE, Fobelets K. Optimization of thz response of strained-si modfets. Physica Status Solidi C: Current Topics in Solid State Physics. 2015;**12, 12**(12):1401-1404. DOI: 10.1002/pssc.201510136

[22] Delgado-Notario JA, Javadi E, Calvo-Gallego J, Diez E, Velazquez JE, Meziani YM, Fobelets K. Sub-micron gate length field effect transistors as broad band detectors of terahertz radiation. Fundamental and Applied Problems of Terahertz Devices and Technologies. 2017;**58**:87-95. DOI: 10.1142/S0129156416400206

[23] Meziani YM, Garcia-Garcia E, Velazquez-Perez JE, Coquillat D, Dyakonova N, Knap W, Grigelionis I, Fobelets K. Terahertz imaging using strained-si modfets as sensors. Solid State Electronics. 2013;**83**:113-117. DOI: 10.1016/j.sse.2013.01.030

[24] Delgado-Notario JA, Meziani YM, Velazquez-Perez JE, Fobelets K. Sub-THz imaging using non-resonant HEMT detectors. Sensors. 2018;**18**:543. DOI: 10.3390/s18020543

[25] Fobelets K, Jeamsaksiri W, Papavasilliou C, Vilches T, Gaspari V, Velazquez-Perez JE, Michelakis K, Hackbarth T, Konig U. Comparison of sub-micron Si:SiGe heterojunction nFETs to Si nMOSFET in present-day technologies. Solid State Electronics. 2004;**48**:1401-1406. DOI: 10.1016/j.sse.2004.01.017

[26] Rumyantsev SL, Fobelets K, Veksler D, Hackbarth T, Shur M. Strained-si modulation doped field effect transistors as detectors of terahertz and sub-terahertz radiation. Semiconductor Science and Technology. 2008;**23**:105001. DOI: 10.1088/0268-1242/23/10/105001

[27] Gaspari V, Fobelets K, Velazquez-Perez JE, Hackbarth T. Dc performance of deep submicrometer schottky-gated n-channel Si:Sige hFETs at low temperature. IEEE Transactions on Electron Devices. 2005;**52**:2067-2074. DOI: 10.1109/TED.2005.855059

[28] Braunstein R, Moore AR, Herman F. Intrinsic optical absorption in germanium-silicon alloys. Physical Review. 1958;**109**:695-710. DOI: 10.1103/PhysRev.109.695

[29] Oberhüber R, Zandler G, Vogl P. Subband structure and mobility of two-dimensional holes in strained Si/SiGe MOSFETs. Physical Review B. 1998;**58**:9941-9947. DOI: 10.1103/PhysRevB.58.9941

[30] Kurita Y, Ducournau G, Coquillat D, Satou A, Kobayashi K, Tombet SB, Meziani YM, Popov VV, Knap W, Suemitsu T, et al. Ultrahigh sensitive sub-terahertz detection by inp-based asymmetric dual-grating-gate high-electron-mobility transistors and their broadband characteristics. Applied Physics Letters. 2014;**104**:251114. DOI: 10.1063/1.4885499

[31] Hänsch W. The Drift Diffusion Equation and its Applications in MOSFET Modeling. Wien: Springer-Verlag; 1991. DOI: 10.1007/978-3-7091-9095-1

[32] Grasser T, Tang TW, Kosina H, Selberherr S. A review of hydrodynamic and energy-transport models for semiconductor device simulation. Proceedings of the IEEE. 2003;**91**:251-274. DOI: 10.1109/JPROC.2002.808150

[33] Meinerzhagen B, Engl WL. The influence of the thermal-equilibrium approximation on the accuracy of classical two-dimensional numerical modeling of silicon submicrometer mos-transistors. IEEE Transactions on Electron Devices. 1988;**35**:689-697. DOI: 10.1109/16.2514

[34] Taurus Medici: Taurus Taurus User Guide, Version X-2005. 10, Synopsys, Inc., Mountain View, California; 2005

[35] Martinez MJM, Pardo D, Velazquez JE. 2d bipolar Monte Carlo calculation of current fluctuations at the onset of quasisaturation of a Si BJT. Physica B: Condensed Matter. 1999;**272**:263-266. DOI: 10.1016/S0921-4526(99)00282-3

[36] Martin MJ, Pardo D, Velazquez JE. Microscopic analysis of the influence of ge profiles on the current-noise operation mode of n-si/p-si1-xgex heterostructures. Semiconductor Science and Technology. 2000;**15**:277-285. DOI: 10.1088/0268-1242/15/3/310

[37] Schaffler F. High-mobility si and ge structures. Semiconductor Science and Technology. 1997;**12**:1515-1549. DOI: 10.1088/0268-1242/12/12/001

[38] Roldan JB, Gamiz F, Cartujo-Cassinello R, Cartujo P, Carceller JE, Roldan A. Strained-si on si1-xgex mosfet mobility model. IEEE Transactions on Electron Devices. 2003;**50**:1408-1411. DOI: 10.1109/TED.2003.81347

[39] Gaspari V, Fobelets K, Velazquez-Perez JE, Ferguson R, Michelakis K, Despotopoulos S, Papavassilliou C. Effect of temperature on the transfer characteristic of a 0.5 mu m-gate Si:Sige depletion-mode n-modfet. Applied Surface Science. 2004;**224**:390-393. DOI: doi.org/10.1016/j.apsusc.2003.08.066

[40] Meziani YM, Garcia E, Calvo J, Diez E, Velázquez E, Fobelets K, Knap W. Detection of Terahertz Radiation from Submicron Plasma Waves Transistors. In: Unil Perera AG, editor. Book Bolometers. Rijeka, Croatia: Intech; 2012. pp. 137-150, ISBN 978-953-51-0235-9

[41] Lu JQ, Shur M. Terahertz detection by high-electron-mobility transistor: Enhancement by drain bias. Applied Physics Letters. 2001;**78**:2587-2588. DOI: 10.1063/1.1367289

[42] Popov VV, Fateev DV, Otsuji T, Meziani YM, Coquillat D, Knap W. Plasmonic terahertz detection by a double-grating-gate field-effect transistor structure with an asymmetric unit cell. Applied Physics Letters. 2011;**99**:243504. DOI: 10.1063/1.3670321

[43] Drexler C, Dyakonova N, Olbrich P, Karch J, Schafberger M, Karpierz K, Mityagin Y, Lifshits MB, Teppe F, Klimenko O, Meziani YM, Knap W, Ganichev SD. Helicity sensitive terahertz radiation detection by field effect transistors. Journal of Applied Physics. 2012;**111**:124504. DOI: 10.1063/1.4729043

[44] Sakowicz M, Lusakowski J, Karpierz K, Grynberg M, Gwarek W, Boubanga S, Coquillat D, Knap W, Shchepetov A, Bollaert S. A high mobility field-effect transistor as an antenna for sub-THz radiation. AIP Conf. Proc. 2010;**1199**:503. DOI: 10.1063/1.3295528

[45] Veksler DB, Muravjov AV, Kachorovskii VY, Elkhatib TA, Salama KN, Zhang XC, Shur MS. Imaging of field-effect transistors by focused terahertz radiation. Solid-State Electronics. 2009;**53**:571. DOI: 10.1016/j.sse.2009.04.004

[46] Sakowicz M, Lusakowski J, Karpierz K, Grynberg M, Gwarek W, Boubanga S, Coquillat D, Knap W, Shchepetov A, Bollaert S. A high mobility field-effect transistor as an antenna for sub-THz radiation. AIP Conf. Proc. 2010;**1199**:503-504. DOI: 10.1063/1.3295528

[47] Rogalsky A, Sizov F. Terahertz detectors and focal plane arrays. Opto-Electronics Review. 2011;**19**(3):346-404. DOI: 10.2478/s11772-011-0033-3

Chapter 5

Clamping Force Distribution within Press Pack IGBTs

Erping Deng, Zhibin Zhao, Jinyuan Li and Yongzhang Huang

Additional information is available at the end of the chapter

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Abstract

Press pack insulated gated bipolar transistors (PP IGBTs) have been gradually used in the high-voltage and high-power-density applications, such as the power system and electric locomotive, with its advantages of double-sided cooling, higher power density, and easy to connect in series compared with traditional wire-bonded power IGBT modules. However, the clamping force is quite important for PP IGBTs because too much clamping fore will cause mechanical damage to the silicon chips and too little clamping force will increase the junction temperature of the silicon chips due to the increased thermal contact resistance. And eventually it leads to thermal damage. Furthermore, the clamping force distribution within PP IGBTs is affected by many factors, and they can be divided into the internal and external factors. The finite element analysis model of the PP IGBTs is established based on the theory of elastic mechanics to obtain the influence of the affect factors, including the external clamping modes, spring design, thermal stress, the machining accuracy, and so on. The contribution of those affect factors to the clamping force distribution is ranked, and this can be a guideline not only for users but also for the manufacturers.

Keywords: flexible HVDC, press pack IGBTs, clamping force distribution, reliability, affect factors

1. Introduction

1.1. Opportunities for PP IGBTs

Nowadays, the challenges such as globally increasing demand of electrical energy, the stringency of conventional energy resources (such as oil, gas, and coal), and so on are arising in the field of electrical energy supply [1]. The high-voltage direct current (HVDC) transmission

system, especially the flexible HVDC transmission system with voltage source converters (VSC), is an innovative solution because of its advantages of the ability to supply the power to the passive power grid (i.e., islet), the independent control of the active and reactive power, and the flexible operation modes [2]. The most important parts of the flexible HVDC transmission system are the converter valve and HVDC breaker, which are based on Insulated Gate Bipolar Transistors (IGBTs), briefly shown in **Figure 1**.

The flexible HVDC transmission system has been successfully applied in the developed countries for many years, and it is prosperous in China in the recent years. More and more projects with higher voltage and higher capacity ratings are developing to meet the requirements and the reliability as the most important issue. This high-voltage and high-reliability application has greatly promoted the development of IGBTs. There are two packaging styles for high-power IGBT devices: typical wire-bonded IGBT modules and press pack IGBTs (PP IGBTs). The high-power IGBT module of 3300 V/1500 A had been widely used in the flexible HVDC transmission system. While with the growing demand of capacity, the IGBT module cannot meet the increasing voltage and capacity requirements, and PP IGBTs are gradually applied with its advantages of higher-power density, easy to connect in series, and short-circuit failure mode [3].

The first PP IGBTs used in the converter valve of the flexible HVDC transmission system in China is 4500 V/1500 A. After this, PP IGBTs of 3300 V/2000 A, 3300 V/3000 A, 4500 V/2000 A, and 4500 V/3000 A are required in the future flexible project because of the higher capacity demand, for example, the 4500 V/3000 A is needed in the 500 kV/3000 MW or 800 kV/3000 MW flexible project.

1.2. Challenges for PP IGBTs

The press pack packaging style for high-voltage and high-power density IGBT can be divided into StakPak (**Figure 2**) and press pack (**Figure 3**). The original motivation in most cases was the poor power-cycling capability of early versions of wire-bonded modules and their explosion behavior [5]. The StakPak packaging style is patent protected by ABB, and the research on the StakPak is very limited. The press pack is widely used by Poseico, Fuji, Westcode, and Toshiba because of the experience with the packaging of high-power devices, such as gate turn-off thyristors, diodes, IGCT, and so on [6], and many researches are based on this packaging style. Therefore, the PP IGBTs discussed in this chapter are the press pack style as shown in **Figure 3**.

Figure 1. Two most important components in the flexible HVDC transmission system: (a) converter valve station and (b) schematic diagram for HVDC breaker [4].

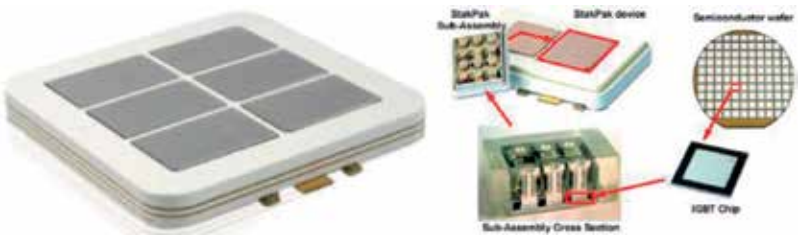

Figure 2. StakPak packaging style from ABB.

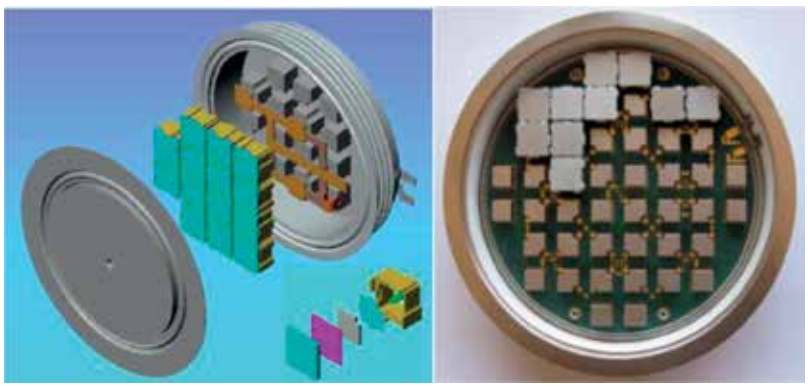

Figure 3. Press pack packaging style from Westcode [7].

Figure 3 shows that the PP IGBTs have a multilayered structure. The electrical and thermal paths for the silicon chips are supplied by the collector and emitter copper electrodes. Furthermore, the needed clamping force also should be applied on the two electrodes to make all components to contact well. The recommended clamping force for applications in a datasheet is a range, and a clamping pressure of 1.2 kN/cm^2 is ideal according to mounting instructions from manufacturers [8, 9]. Two molybdenum plates surrounding the silicon chips are to uniform the clamping force distribution and reduce the thermal expansion/contraction between the molybdenum plates and silicon chips when the press pack IGBT undergoes high-temperature variations. A silicon chip subassembly is consisted of a silver shim plate, together with a silicon chip and two molybdenum plates. Many silicon chip subassemblies connected in parallel to form a press pack IGBT and the current rating is determined by the paralleled number.

With the increasing demand of higher voltage and current ratings, more and more silicon chip subassemblies are needed to connect in parallel. Therefore, there are many challenges in the packaging technology, especially the long life time reliability when applied in the flexible HVDC transmission system as follows:

- current distribution among silicon chips [10];
- clamping force distribution among silicon chips [11–13];
- junction temperature distribution among silicon chips [14];

- the internal insulation problem [15];
- long-time reliability [16].

1.3. Clamping force distribution

For PP IGBTs, the clamping force is a special and very important parameter that many other parameters are correlated with this value, including the electrical and thermal behavior, reliability, and so on. For example, the current and junction temperature distributions are affected by the clamping force distribution a lot [17] through the electrical and thermal contact resistance [18, 19]. Too much clamping force will mechanically damage the silicon chip and too little clamping force will increase the junction temperature caused by the increased thermal contact resistance. Eventually, this leads to the silicon chip thermal damage as shown in **Figure 4** [20]. Therefore, the clamping force distribution within PP IGBTs is quite important that it not only affects both the electrical and thermal behavior but also the long-time reliability of PP IGBTs.

There are many factors that may influence the clamping force distribution within PP IGBTs not only during the design process but also in the applications. And the affect factors can be divided into external and internal factors. All the factors that may affect the clamping force distribution within PP IGBTs are shown subsequently and analyzed through the finite element method. For high-power IGBT modules or PP IGBTs, some Fast Recovery Diode (FRD) chips are always connected in anti-paralleled with the IGBT chips to provide the current path while the IGBT chips are turned off. Actually, the matching of the silicon chips, which means the internal layout of IGBT chips and FRD chips within PP IGBTs, will also influence on the clamping force distribution. However, the electrical and thermal behaviors, for example, the collector current and junction temperature distributions, of the PP IGBTs depend on the internal layout or matching of the silicon chips to a large extent. Therefore, the matching of the silicon chips should pay more attention to the electrical and thermal behaviors rather than the clamping force distribution.

A. External affect factors

- external clamping modes
- design of disc spring

B. Internal affect factors

- slim plates
- thermal stress
- machining accuracy
- internal layout
- design of electrodes

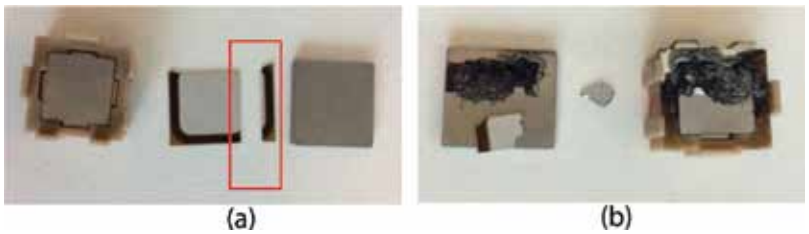

Figure 4. Failed silicon chips caused by nonuniform clamping force [20]: (a) too much pressure and (b) too little pressure.

2. Basic theory

2.1. Governing equations

Mechanics is a very useful discipline established to explain many phenomena existing in nature, for example, material mechanics, structure mechanics, elastic mechanics, elastic–plastic mechanics, and so on. Material mechanics is mainly used to explain the deformation of a single simple object. Elastic mechanics can be used to research the micro-deformation phenomenon, and elastic–plastic mechanics is mainly used to explain the macro-deformation, for example, nonlinearity, material yield problem, and so on.

PP IGBTs consist of many components that undergo micro-deformation as stated before, thus the elastic mechanics is suitable for its mechanical analysis. The mechanical analysis of a specific material can be explained through the physical properties of materials, deformation, and the balance of forces. Just like in the electrical engineering area, Maxwell's equations can be used to explain all electromagnetic phenomena. Coupled with specific boundary conditions, three equations, including the constitutive equations of materials, geometric equations, and equilibrium equations of force as shown in Eqs. (1)–(3), are used to solve all the elastic mechanics problems:

$$-\nabla \cdot \sigma = F \tag{1}$$

$$\sigma = E \cdot \varepsilon \tag{2}$$

$$\varepsilon = \nabla \cdot u \tag{3}$$

where σ is stress, F is external force, E is elasticity modulus, ε is strain, and u is displacement.

2.2. Finite element model

Eqs. (1)–(3) can be used to explain all the elastic mechanics phenomena, and the equations without specific boundary conditions have unbounded solution. But for engineering problems, there must be a specific solution. Thus, we need to appoint the boundary condition for engineering problems to get the unique solution. In this chapter, the finite element model of PP IGBTs is proposed to predict the clamping force distribution under different conditions and

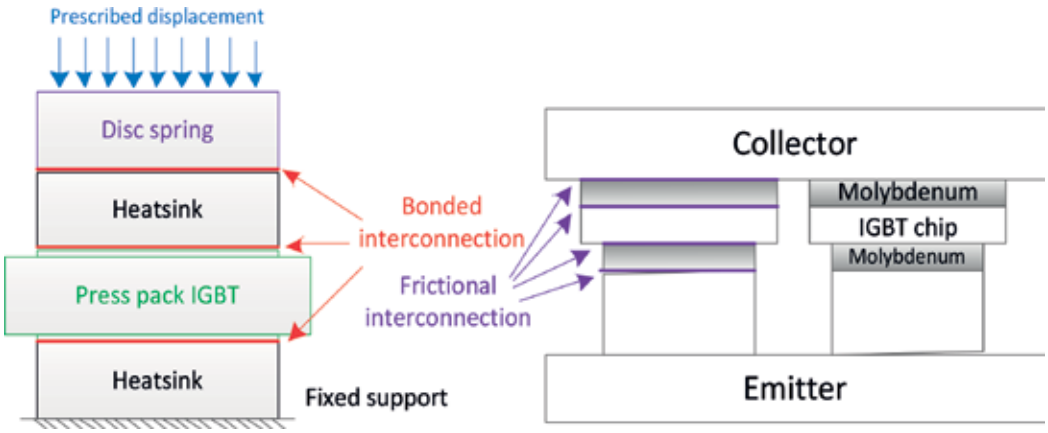

Figure 5. Boundary conditions of the mechanical model.

the boundary conditions are set as follows. In the application of PP IGBTs, a force spreader or a clamp stack is used to transmit the clamping force to the heatsink and then transfer from the heatsink to the surface of the PP IGBTs. A disc spring, usually changing several mm under the clamped phase, is needed to compensate the physical movements, usually several μm, during the process of clamping and thermal expansion. To approximate the working conditions, a prescribed displacement, which is equivalent to the rated clamping force, is applied to the disc spring on the surface of the heatsink of the PP IGBT collector side. A fixed support is placed on the surface of the heatsink of the PP IGBT emitter side. The simplified diagram of the boundary conditions for the mechanical model is shown in **Figure 5**. The mechanical model should also consider the frictional interconnections among the different layers. The interconnections between heatsinks and PP IGBT are set as the bonded interconnection, and the interconnections between multilayers within PP IGBT are set as a frictional contact. A friction coefficient of 0.5 is assumed for the contact layers within the PP IGBT [21, 22], because the friction coefficient has little influence on the pressure distribution [23]. All finite element models used in this chapter to analyze the clamping force distribution within PP IGBTs, with the exception of the specified models, are set as in **Figure 5**.

3. External affect factors

Among the factors that may affect the clamping force distribution within PP IGBTs, we defined the factors from the applications or should pay attention in the applications or the factors outside of the PP IGBTs as the external affect factors. In the application of PP IGBTs, there exist two external factors that may affect the clamping force distribution a lot: external clamping modes and the design of disc spring.

3.1. External clamping modes

The press pack packaging style for IGBTs is learned from thyristors, IGCT, and so on, thus the clamping fixture to supply the needed clamping force in application is also the same. A force

spreader is used to transmit the clamping force to the heatsink and then transfer from the heatsink to the surface of the PP IGBTs as shown in **Figure 6**. The disc spring is also needed to compensate the displacement during the clamping phase, and this parameter will be analyzed in the next part.

The force spreader is quite important in the clamping fixture for the press pack packaging style devices to transmit the uniform clamping force on the devices. Different from those devices with the whole wafer, like thyristors, IGCT, and so on, PP IGBTs contain multi-chips which are connected in parallel to improve the current rating. The uniform of the clamping force on the surface of PP IGBTs will greatly influence the clamping force within PP IGBTs and lower the reliability. Thus, the design of the force spreader is quite important to ensure its basic functions and improve the reliability of the whole system.

According to the basic principle of elastic mechanics, there are two boundary conditions to solve the elasticity problems: force load and displacement load. Force load is the most used boundary condition in the finite element simulations. Most of the studies that focus on the clamping force distribution within PP IGBTs used the force load principle. However, the PP IGBTs clamped by the clamping fixture are restricted by the prescribed displacement. Which boundary condition is suitable for the mechanical analysis of PP IGBTs is unclear. Those two boundary conditions directly applied on the surface of the PP IGBT are compared based on the finite element model mentioned earlier. Nine silicon chips are used as shown in **Figure 7**, and the clamping force of each silicon chip is shown in **Table 1**.

From the results, we can see that chip 5 located in the center of the PP IGBT has a relatively lower clamping force than other chips with the force load boundary condition, and the error is about −30.32%. As the study [19] shows, the thermal contact resistance existed in the contact interface within PP IGBTs depends on the clamping force to a large extent. Thus, the uniform clamping force distribution will influence the characteristic and reliability of PP IGBTs. However, the clamping force distribution within PP IGBT is relative even with the displacement of load condition that the maximum error is about 1.39%. In the real applications, the PP IGBTs are restricted by the prescribed displacement through clamping fixture. However, it is impossible to ensure a uniform displacement on the surface like the displacement load boundary

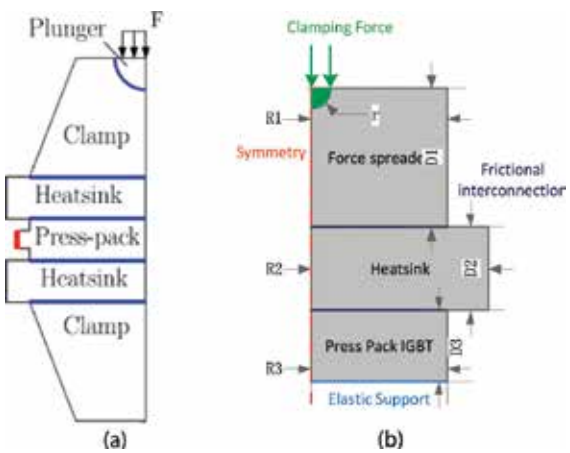

Figure 6. Simplified schematic diagrams for the clamping system: (a) structure diagram and (b) simulation diagram.

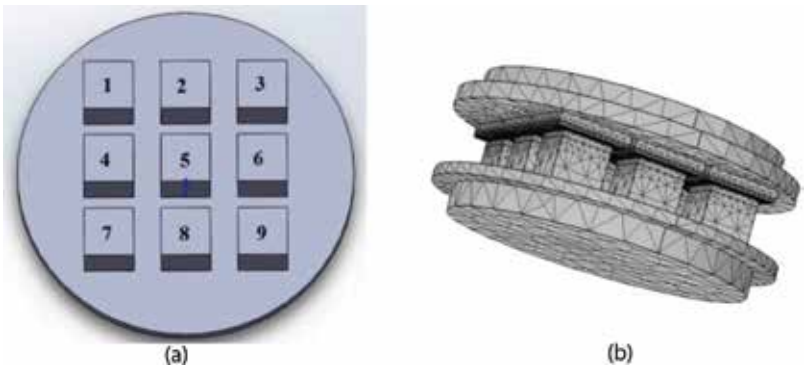

Figure 7. Finite element model: (a) chip number and (b) schematic diagram for simulation.

No	Rated (N)	Force (N)	Error (%)	Displacement (N)	Error (%)
1	1000	1074.6	7.46	986.06	−1.39
2	1000	1001.0	0.10	1010.1	1.01
3	1000	1073.5	7.35	987.06	−1.29
4	1000	1001.0	0.10	1009.7	0.97
5	1000	696.84	−30.32	1011.3	1.13
6	1000	1000.9	0.09	1010.4	1.04
7	1000	1076.1	7.61	987.39	−1.26
8	1000	1002.3	0.23	1011.9	1.19
9	1000	1073.8	7.38	986.09	−1.39

Table 1. Clamping force distribution under different boundary conditions.

condition. Furthermore, the clamping force will increase due to the thermal stress when the PP IGBT is heated up, and the force load condition is not suitable anymore in this situation.

The reason why the clamping force distribution within PP IGBT with force load conditions is worse than the displacement is because the displacement on the surface of PP IGBT is uneven. Therefore, the force spreader is designed to transmit the clamping force to the PP IGBT and ensure that the displacement on the surface is uniform. The clamping force distribution within PP IGBTs is related with the height of the force spreader as shown in **Figure 8** with the results of chip 5.

The radius of the studied PP IGBT is 28 mm, and as seen in **Figure 8**, the error of chip 5 trends to be stable when the height of the force spreader will be higher than 30 mm. That is to say, the displacement on the surface of the PP IGBT is relatively uniform and will not change with a higher force spreader. This is very important in the application. The height of the force spreader should be larger than the radius of the PP IGBT to ensure the clamping force distribution. And the error of chip 5 is still higher than the displacement load condition. However, the displacement load condition on the surface of PP IGBT or heatsink is too ideal.

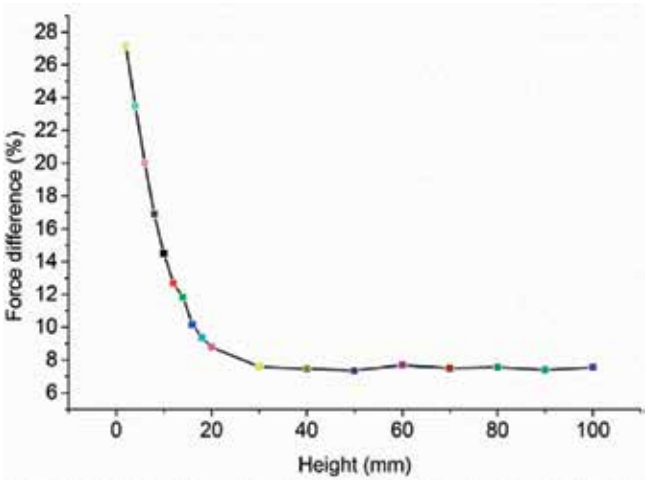

Figure 8. Relationship between the height of force spreader and error of chip 5.

Based on these results, it is shown that the design of the force spreader is quite important that the height of force spreader should be larger than the radius of the PP IGBT. Meanwhile, the clamping mode is very important in the finite element simulation. The best way is to apply the displacement load on the force spreader.

3.2. Design of disc spring

The disc spring is another quite important parameter in the application of PP IGBTs because it can not only compensate the displacement during clamping process but also absorb the thermal stress generated by the high temperature. Firstly, the importance of the disc spring is explained by the single IGBT chip submodule as shown in **Figure 9** under different conditions. One is the clamping phase that the submodule is just clamped by the fixture and another is the heating phase that the submodule is heated up with a desired clamping force.

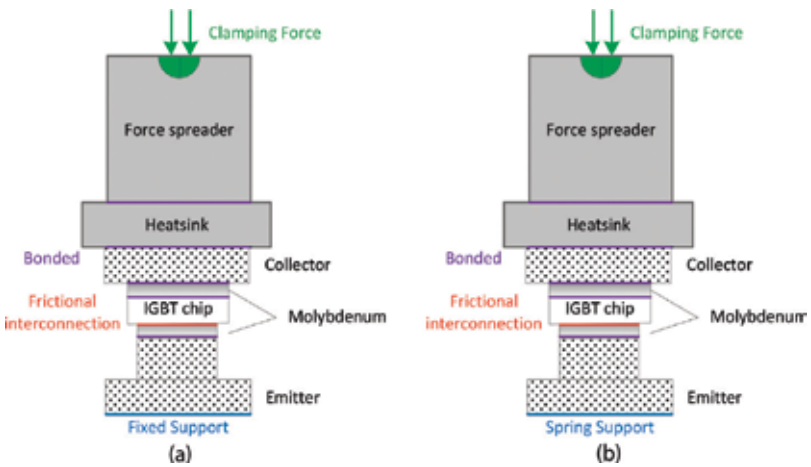

Figure 9. Simulation schematic diagram of single IGBT submodule: (a) without spring and (b) with spring.

As mentioned earlier, the rated clamping force of the single IGBT submodule is obtained through the displacement on a proper designed force spreader. The calculated clamping force of the submodule is used to compare with different conditions, and it is the real clamping force existing in the submodule after the submodule is clamped by the desired displacement.

Furthermore, the selection or the design of the disc spring is also quite important in the applications. The most important parameter for disc spring is the equivalent elastic coefficient. The higher this value, the disc spring is harder to deform which means higher force is needed to obtain the same deformation. And the lower this value, the disc spring can compensate more displacement with the same clamping force. Therefore, the selection of the equivalent elastic coefficient is a tradeoff problem. The rated clamping force of the submodule is designed to 1 kN and the displacement is 1 mm. Therefore, the rated equivalent elastic coefficient is 1e6 N/m. The submodule under the heating phase with different coefficients, range from 1e6 to 1e7, is also analyzed and the results are shown in **Table 2**.

where "without" means no disc spring is applied in the simulation and the value with a unit of N/m is the equivalent elastic coefficient of the disc spring applied in the simulation. The results show that there is no difference in the calculated clamping force of the single submodule whether a disc spring is applied or not during the clamping phase. And the calculated value is almost equal to the rated clamping force of 1 kN. That is to say, the disc spring has no influence on the clamping phase after the submodule is clamped. The disc spring is used to slow down the change rate of the clamping force during the clamping process but it will not affect the final value after the submodule is clamped. Just like the inductance in the circuit, it is used to restrict the change rate of current.

However, the clamping force will increase sharply due to the thermal stress generated by the high temperature when the silicon chip is heated up. And the value is almost 14 times of the rated clamping force. This high clamping force may mechanically damage the silicon chip. The reason is that the submodule is constricted by the clamping fixture. Thus, a disc spring is needed to compensate the displacement or deformation due to the thermal stress, and the calculated clamping force can be controlled to some extent. The increment of the clamping force is also influenced by the equivalent elastic coefficient. The calculated clamping force will be higher with a higher value of equivalent elastic coefficient. And the increment rate of 2.14, 10.65, and 21.06% is also proportional to the value of equivalent elastic coefficient. The reason is that the allowed displacement of the disc spring is 1, 0.2, and 0.1 mm with the same clamped conditions. Actually, the increment of the clamping force cannot be eliminated if the submodule is clamped even if adequate disc spring is applied. And this will not only increase the cost but also will be very difficult to obtain the desired clamping force. Therefore, the design of the disc spring should consider the requirements from application and it is a tradeoff problem.

	Clamping phase (N)		**Heating phase (N)**			
	Without	**1e6 (N/m)**	**Without**	**1e6 (N/m)**	**5e6 (N/m)**	**1e7 (N/m)**
Calculated	997.57	997.59	13,948	1021.4	1106.5	1210.6

Table 2. Calculated clamping force of the submodule comparison.

4. Internal affect factors

Those factors that mainly existed in PP IGBTs or during the design process are defined as the internal affect factors. The internal factors that may affect the clamping force distribution should be analyzed and optimized because it is quite important for the structure design of PP IGBTs. There are five parameters that may affect the clamping force distribution within PP IGBTs a lot: slim plates, thermal stress, machining accuracy, internal layout, and the design of electrodes. Among those affect factors, thermal stress is not a structure parameter that can be changed during the structure design. But this factor is quite important because it will influence the layout or the matching of silicon chips.

4.1. Slim plates

Until now, there are two main packaging styles for PP IGBTs: press pack and StakPak. The StakPak packaging style contains a spring to distribute the clamping force which is patent protected by ABB and the research is very limited. The press pack is widely used by Poseico, Fuji, Westcode, and Toshiba [20, 24]. All the researches are based on the press pack, and there are also some variations between different manufacturers. As shown in **Figure 3** and stated before, a slim plate of silver is proposed to mechanically support the single chip submodule and compensate few deformations because of its good softness.

The contribution of slim plate to the clamping force distribution within PP IGBTs is revealed with three different conditions. As it is known, it is difficult to ensure the same high of all submodules due to the machining accuracy of each component within PP IGBTs or some errors during the assembling process. Condition I is that all the submodules in PP IGBTs have the same height and condition II is that one of those submodules is 0.5 μm lower than others. Condition III is that one of those submodules is 0.5 μm higher than others. The finite element model for this simulation is also shown in **Figure 7** with nine silicon chips, and the height of chip 5 is selected to change. The clamping force distribution within the PP IGBT with different conditions is shown in **Table 3**.

No	Rated (N)	I		II		III	
		Without	With	Without	With	Without	With
1	1000	1016.9	1005.1	1043.79	1044.8	987.27	986.74
2	1000	1005.5	995.96	1043.4	1045.6	965.52	966.94
3	1000	1013.3	1000.9	1041.79	1046.3	986.31	987.55
4	1000	1004.5	976.62	1043.81	1046.1	965.52	965.9
5	1000	924.14	915.56	659.93	630.19	1200	1194.6
6	1000	1002.9	990.6	1041.46	1046.5	965.8	966.3
7	1000	1015.1	999.31	1042.57	1045.8	985.74	987.61
8	1000	1002.5	983.6	1041.03	1047.1	965.83	966.51
9	1000	1015.1	1001	1042.18	1047.7	987.52	987.39

Table 3. Clamping force distribution with different conditions.

The results show no big difference between the single submodules with applied slim plate or without. That is to say, the influence of the slim plate on the clamping force distribution can be ignored. The reason is that the deformation of the silver slim plate is very limited even it has a relative small Young's modulus.

4.2. Thermal stress

A clamping force is needed to ensure the basic functions, and all the components within PP IGBTs contact well. The silicon chips will produce much heat and increase the temperature under working condition of the PP IGBT. Thus, this high temperature induces thermal stress because all the components are constricted by the clamping fixture, and there is no space to move when they are heated up. The thermal stress during the heating phase will change the clamping force distribution within PP IGBTs to a large extent [20]. The finite element model of the conceptual PP IGBT studied consists of 44 silicon chips (30 IGBT chips and 14 FRD chips), and the chip number is marked as shown in **Figure 10**.

A finite element multi-physics model co-coupled with an electrical field, thermal field, and mechanical field is proposed to predict the clamping force distribution within the PP IGBT. The status of the clamping phase is that the PP IGBT is only clamped by the clamping fixture with a prescribed displacement. And the heating phase is the state where the clamped PP IGBT is heated up caused by the collector current to approximate its working condition. More details for this part can be found in the study [20]. The simulation results are shown in **Figure 11**.

The contact pressure distribution within the studied PP IGBT is relatively uniform under the clamping phase. However, this situation changes a lot when the PP IGBT is heated up. The pressure distribution is extremely uneven and is mainly concentrated in the center. That is to say, the clamping force distribution will also be uneven, and the change trend will be the same

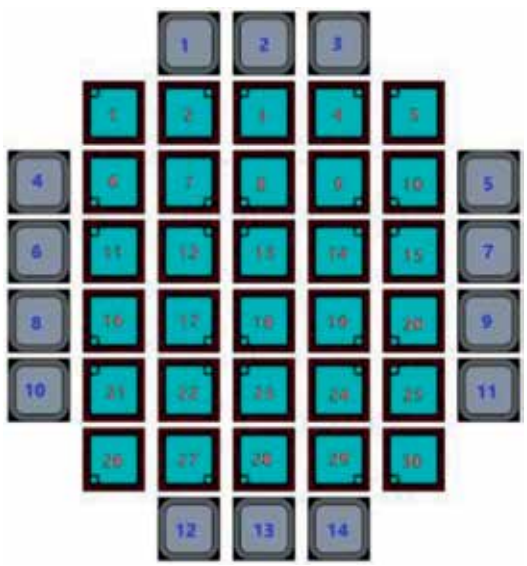

Figure 10. Internal layout and chip numbers of the conceptual PP IGBT.

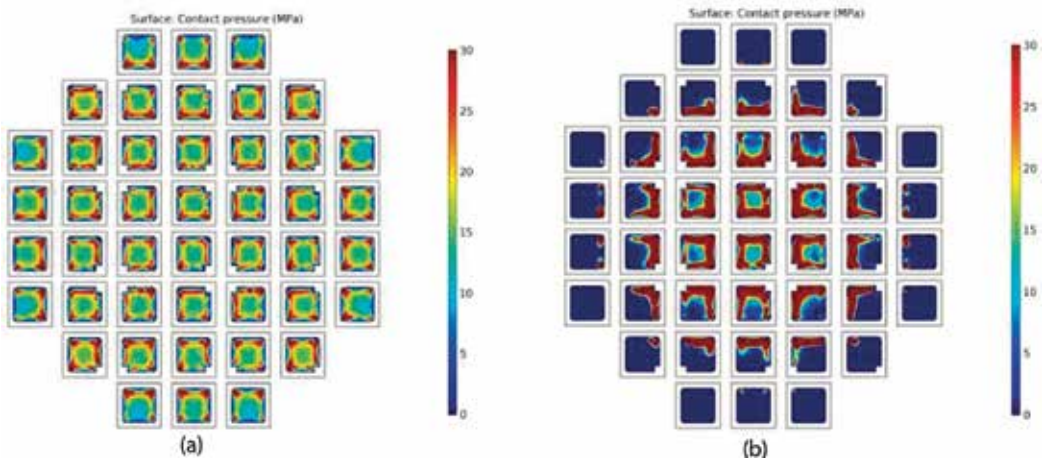

Figure 11. Contact pressure distributions within PP IGBT: (a) clamping phase and (b) heating phase.

with the contact pressure. The average clamping force of one FRD chip (#2) and three IGBT chips (#3, #8, and #13) located in the axis is extracted (marked with a red block in **Figure 10**) and compared in **Table 4**.

The reason is that the collector electrode presents a warpage when the PP IGBT is heated up, and this leads to an extremely uneven clamping force distribution. However, there also exists a little difference among the silicon chips in the clamping force distribution even in the clamping phase because of the warpage of the collector electrode. Another reason is that the pedestal is too hard to absorb the thermal stress generated by the high temperature of silicon chips. Therefore, a harder collector electrode and a softer pedestal can improve the clamping force distribution within PP IGBT.

4.3. Machining accuracy

As stated before, the PP IGBT has a multilayer structure and all components are stacked. It is impossible to control each component having the same size because of the machining accuracy. Therefore, the difference or error in the size among components is inevitable. Furthermore, the size error existing in each component will also be summed up during the assembling process as the components are stacked. Adding up all factors means that the height of each submodule will not be the same. These existing differences of the height of the submodules will affect the clamping force distribution. The finite element model including 11 IGBT chips and five FRD chips is shown in **Figure 12**. More details can be found in the study [13].

The FRD chip 5 with different height tolerances, ranges from 0 to −3 μm, is selected to predict the clamping force distribution within the studied PP IGBT. The von Mises stress on the surface of the silicon chips (IGBT 4, IGBT 8, FRD2, and FRD5) with different heights is extracted and shown in **Figure 13**. Furthermore, the average clamping force of FRD chip 5 is extracted under different height tolerances as shown in **Figure 14**.

The results show that the clamping force of FRD chip 5 decreases sharply while the height tolerances is increasing. The clamping force decreases to less than 100 N, which is much less than

Chip no.	Rated (N)	F (N)		Deviation (%)	
		Case 1	Case 2	Case 1	Case 2
#2	1660	1596.3	84.841	−3.84	−94.89
#3	1558	1549.2	2301.3	−0.56	47.71
#8	1558	1569.1	2949.6	0.71	89.32
#13	1558	1577.8	3072.5	1.27	97.21

Table 4. Average clamping force comparison.

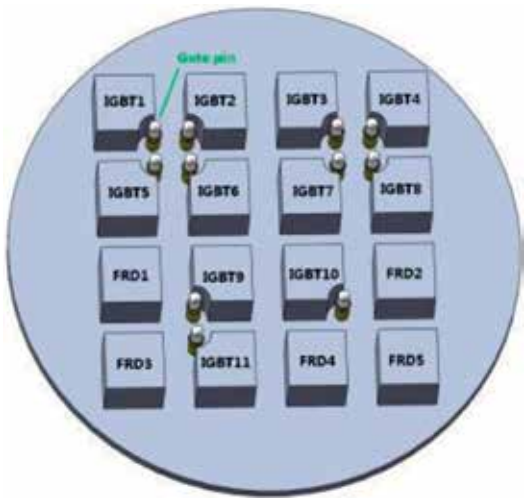

Figure 12. Finite element model and chip number.

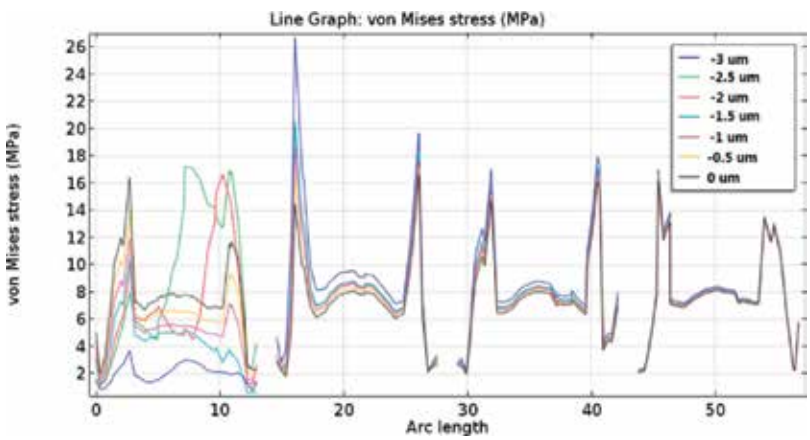

Figure 13. von Mises distribution of the selected silicon chips.

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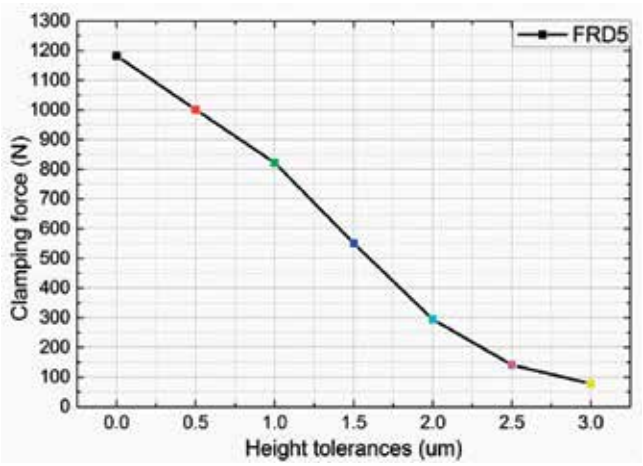

Figure 14. Clamping force of FRD chip 5 under difference height tolerances.

the rated clamping force, when the height tolerance is 3 μm. It is assumed that this chip will lose contact if the height tolerance is more than 3 μm. Meanwhile, the von Mises of the chip nearby the FRD chip 5 will increase sharply, especially the von Mises in the border between the active area and the terminal area. This area is very easy to crack if too much clamping force is applied as stated in [20]. Therefore, the machining accuracy should be controlled to a certain extent to ensure the clamping force distribution. The maximum height tolerance of each submodule should be controlled within 3 μm based on this simulation result.

4.4. Internal layout

From the simulation results of the study [13, 20], there still exists some difference among the submodules in the clamping force distribution within PP IGBTs because of the warpage of the collector electrode even everything is well controlled. The influence of the electrode on the clamping force in this packaging style is inevitable. However, the internal layout can be changed to reduce the influence of the electrode and improve the distribution a little bit. Three layouts are designed and analyzed through the finite element model as shown in **Figure 15**.

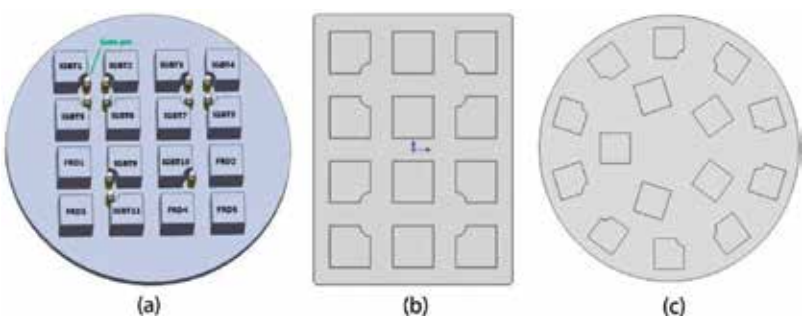

Figure 15. Three different layouts: (a) circular electrodes with the square internal layout, (b) square electrodes with the square internal layout, and (c) circular electrodes with the circular internal layout.

Proposal I is the circular electrodes with the square internal layout; proposal II is the square electrodes with the square internal layout, and proposal III is the circular electrodes with the circular internal layout. The different internal layouts lead to some distinction in the warpage of the electrodes and then affect the clamping force distribution. The average clamping force of each silicon chip is extracted and listed in **Table 5**.

From the clamping force distribution of three different internal layouts, it is shown that it is relatively uniform and the error is acceptable. Considering the difference between the IGBT chips and FRD chips, proposal II is better than I and III with a relatively lower error between the IGBT chips and FRD chips of 4.3% (2.65% to (−1.65%)). The error of those two proposals is 14.98 and 15.75%, respectively. Considering the difference among IGBT chips or FRD chips, proposal III is better because all the IGBT chips or FRD chips are located in the same circular and have the same deformation. However, the error among IGBT chips or FRD chips of proposal II is also relatively low with a value of 0.9 and 0.39%, respectively. In conclusion, proposal II is better than those two proposals because the electrode undergoes little deformation when the PP IGBT is clamped.

4.5. Design of electrodes

Many factors that affect the clamping force distribution within PP IGBTs have been analyzed before because it is known that most of those factors lead to warping the electrode. Therefore, the design of the collector electrode is also quite important for the clamping force distribution

No	Rated (N)	Average clamping force (N)			Error (%)		
		I	II	III	I	II	III
IGBT1	1129	1172.5	1119.2	1068.9	3.85	−0.87	−5.32
IGBT2	1129	1179.3	1111.9	1069.5	4.46	−1.51	−5.27
IGBT3	1129	1176.5	1111.2	1069.6	4.21	−1.58	−5.26
IGBT4	1129	1168.1	1119.8	1069.5	3.46	−0.81	−5.27
IGBT5	1129	1168.1	1120.0	1069.6	3.46	−0.80	−5.26
IGBT6	1129	1026.2	1110.8	1068.5	−9.11	−1.61	−5.36
IGBT7	1129	1024.6	1110.4	1069.5	−9.25	−1.65	−5.27
IGBT8	1129	1162.5	1120.5	1070.0	2.97	−0.75	−5.23
IGBT9	1129	1010.3	—	1069.3	−10.5	—	−5.29
IGBT10	1129	1004.9	—	1070.0	−11.0	—	−5.23
IGBT11	1129	1136.6	—	—	0.67	—	—
FRD1	1161	1207.2	1191.8	1281.1	3.98	2.65	10.39
FRD2	1161	1198.9	1186.1	1281.6	3.26	2.16	10.36
FRD3	1161	1189.9	1187.2	1281.3	2.49	2.26	10.35
FRD4	1161	1192.3	1190.8	1281.2	2.70	2.57	10.28
FRD5	1161	1182.1	—	1280.3	1.82	—	10.34

Table 5. Average clamping force comparison for different internal layouts.

of PP IGBTs. A step has to be designed in the electrode to form a flange to make the PP IGBT a confined space to protect the silicon chips out of environment disruption. Two important parameters in this part are shown in **Figure 16** and are explained.

Where *A* is the diameter of the electrode and *B* is the equivalent diameter of the pedestals. The parameter *A* is the most important parameter because it is used to conduct the current, heat flux, and the clamping force. And furthermore, the equivalent diameter *B* is also very important that the clamping force is transmitted through the pedestals. Whether the value of *A* is matched with *B* or not will affect the clamping force to a large extent. The finite element model used in this section consists of 40 IGBT chips and 20 FRD chips, and this model is axial symmetry. Only half of this model is simulated to save time, and then the results can be expanded to the whole model. Firstly, the electrode diameter of 125 and 141 mm is simulated and the pressure on the surface of the silicon chips is shown in **Figure 17**.

Where the value of 125 mm is smaller than the equivalent diameter of pedestals and 141 mm is larger than that value. The simulation results show that the pressure will concentrate in the center of the PP IGBT when the diameter of the electrode is smaller than the equivalent diameter of pedestals. And the pressure will concentrate in the boundary of the PP IGBT when the diameter of the electrode is too large. The reason is that the electrode undergoes a different direction warpage under those two conditions. Then, different electrode diameters as 125, 127, 131, 135, 139, and 141 mm are simulated based on this finite element model and the average clamping force of each silicon chip is extracted. The clamping force error of each silicon chip is shown in **Table 6** with half model.

As it is seen in the results, the majority of the IGBT chips have plus deviation/error when the electrode diameter is smaller than 135 mm and they have minus error when the diameter is

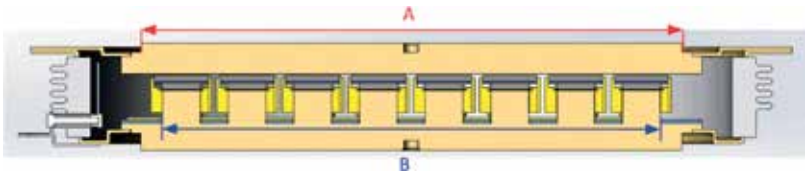

Figure 16. Explanation for important parameters.

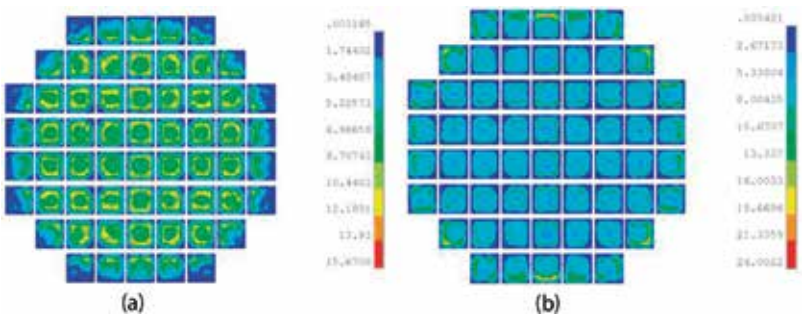

Figure 17. Pressure distribution on the surface of the silicon chips: (a) diameter of 125 mm and (b) diameter of 141 mm.

No.	∅125		∅127		∅131		∅135		∅139		∅141	
	IGBT	FRD	IGBT	FRD	IGBT	FRD	IGBT	FRD	IGBT	FRD	IGBT	FRD
1	−29.35	−61.44	−23.56	−54.53	−13.34	−39.45	−4.96	−22.76	3.02	−5.98	6.90	2.48
2	18.23	−25.75	5.32	−17.95	10.10	−4.35	4.72	7.32	−0.76	18.08	−3.77	23.50
3	1.95	−60.66	18.26	−53.91	0.30	−38.15	3.15	−21.07	−3.60	−3.90	−7.18	4.52
4	7.81	−6.15	5.60	−2.10	9.43	.53	3.78	3.35	−1.03	21.04	−3.98	24.58
5	3.52	3.25	8.91	18.72	11.60	1.56	4.26	3.51	−3.47	−3.64	−6.72	−7.57
6	2.41	2.64	18.32	18.72	11.10	0.87	3.65	3.61	−3.73	−3.27	−7.17	−6.39
7	−20.50	20.15	−15.20	16.31	−5.59	.14	2.01	2.32	9.24	−3.83	12.96	−6.66
8	0.83	−61.04	7.46	−54.13	9.45	−38.38	2.08	−20.88	−5.34	−3.91	−9.37	4.53
9	2.74	−25.16	18.85	−17.34	0.83	−3.87	3.77	7.03	−3.84	17.74	−7.15	24.17
10	0.17	−61.03	6.52	−54.72	.57	−39.33	2.50	−22.88	−3.74	−5.71	−7.00	2.25
11	−20.57		−15.12		−5.31		2.30		9.16		12.99	
12	2.39		18.40		9.92		2.74		−5.08		−8.88	
13	22.78		18.83		0.91		3.47		−4.29		−6.82	
14	20.28		16.52		9.37		2.59		−3.68		−7.20	
15	7.19		14.59		9.10		3.30		−1.22		−4.86	
16	22.83		18.95		11.58		4.51		−3.27		−6.88	
17	21.72		17.74		10.71		3.36		−4.00		−7.42	
18	7.49		15.27		9.80		5.07		−0.34		−4.02	
19	2.73		8.53		10.05		2.78		−3.67		−6.89	
20	−29.45		−23.26		−13.14		−4.63		3.02		7.08	

Table 6. Average clamping force errors among silicon chips with half model (unit: %).

larger than 135 mm. And the clamping force distribution among IGBT chips is uniform. For FRD chips, there exists some difference among those chips but this is acceptable. Therefore, the electrode diameter of 135 mm is the best among those diameters, and this value is close to the equivalent diameter of pedestals. That is to say, the best way to improve the clamping force distribution within PP IGBTs is to match the electrode diameter with the equivalent diameter of pedestals during the electrode design process.

5. Conclusions

The clamping force distribution within PP IGBTs is quite important because it affects not only the electrical and thermal characteristic but also the reliability. Many factors may affect the clamping force that has been classified and analyzed through the finite element method in this chapter,

and the simulation results are well presented and explained. Based on the simulation results, we know that we should pay more attention to the thermal stress, machining accuracy, internal layout, and electrode design during the structure design process, especially the thermal stress. The disc spring is very important for the PP IGBT application, and this factor also should be considered during the mechanical simulation. The slim plate can be omitted in the mechanical simulation that it is too thin and its contribution to the clamping force distribution is very limited.

The clear classification and analysis of all the factors that affect the clamping force distribution can give a guideline not only for the semiconductor manufacturers to optimize the structure design but also for users to take full advantages of the PP IGBTs.

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Author details

Erping Deng[1,2]*, Zhibin Zhao[1], Jinyuan Li[2] and Yongzhang Huang[1]

*Address all correspondence to: dengerpinghit@163.com

1 North China Electric Power University, Beijing, China

2 Global Energy Interconnection Research Institute, Beijing, China

References

[1] Dorn J, Huang H, Retzmann D. Novel voltage- sourced converters for HVDC and FACTS applications. Keynote In: International Council on Large Electric Systems (CIGRE'2007). Osaka, Japan; 2007

[2] Gao Q, Lin Y, Huang L. An overview of Zhoushan VSC-MTDC transmission project. Power System & Clean Energy. 2015;**31**(2):33-38

[3] Wakeman F, Hemmings D, Findlay W, Lockwood G. Pressure Contact IGBT, Testing for Reliability. Westcode Semiconductors Ltd.; March 2012

[4] Häfner J, Jacobson B. Proactive hybrid HVDC breakers—A key innovation for reliable HVDC grids. The Electric Power System of the Future Integrating Super Grids and Micro-grids International Symposium; Bologna, Italy: IEEE, 2011. pp. 264-273

[5] Zeller H. High power components from the state-of-the-art to future trends. In: Proceedings of the Conference on Power Conversion (PCIM' 98); Nurmberg, Germany; May 1998. pp. 1-10

[6] Busca C, Teodorescu R, Blaabjerg F. An overview of the reliability prediction related aspects of high power IGBTs in wind power applications. Microelectronics Reliability. 2011;**51**(9-11):1903-1907

[7] Golland A, Wakeman F. Application of press-pack IGBTs in traction refurbishment. APEC; Austin, Texas, USA; 2005

[8] Recommendations regarding mechanical clamping of Press Pack High Power Semiconductors, ABB

[9] Application Note for Device Mounting Instructions. Westcode Semiconductors Ltd.; March 2012

[10] Müsing A, Ortiz G, Kolar JW. Optimization of the current distribution in press-pack high power IGBT modules. In: Proceedings of the IEEE Power Electronics Conference (IPEC'10); June 2010. pp. 1139-1146

[11] Hasmasan A, Busca C, Teodorescu R. Modelling the clamping force distribution among chips in press-pack IGBTs using the finite element method. In: Proceedings of the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG'12); June 2012. pp. 788-793

[12] Hasmasan A, Busca C, Teodorescu R. Electro-thermo-mechanical analysis of high-power press-pack insulated gate bipolar transistors under various mechanical clamping conditions. IEEE Journal of Industry Applications. 2014;**3**(3):192-197

[13] Deng EP, Zhao ZB, Zhang P. Clamping force distribution within press pack IGBTs. Transactions of China Electrotechnical Society. 2017;**32**(6):201-208

[14] Busca C, Teodorescu R, Blaabjerg F. Dynamic thermal modelling and analysis of press-pack IGBTs both at component-level and chip-level. In: Proceedings of the Conference of IEEE Industrial Electronics Society (IECON'13); November 2013. pp. 677-682

[15] Sweet M, Sankara Narayanan EM, Steinhoff S. Influence of cassete design upon breakdown performance of a 4.5kV press-pack IGBT module. In: Proceedings of the International Conference on Power Electronics, Machines and Drives (PEMD'16); Glasgow, UK; April 2016. pp. 1-6

[16] Tinschert L, Årdal AR, Poller T. Possible failure modes in press-pack IGBTs. Microelectronics Reliability. 2015;**55**(6):903-911

[17] Poller T, Arco SD, Hernes M. Influence of the clamping pressure on the electrical, thermal and mechanical behaviour of press-pack IGBTs. Microelectronics Reliability. 2013;**53**(9-11):1755-1759

[18] Magnar H. Determination of the thermal and electrical contact resistance in press-pack IGBTs. Prenatal Diagnosis. 2013;**32**(13):1233-1241

[19] Deng EP, Zhao ZB, Zhang P. Optimization of the thermal contact resistance within press pack IGBTs. Microelectronics Reliability. 2017;**69**:17-28

[20] Deng E, Zhao Z, Lin Z, et al. Influence of temperature on the pressure distribution within press pack IGBTs. IEEE Transactions on Power Electronics. 2017;**PP**(99):1-1

[21] Pirondi A, Nicoletto G, Cova P, et al. Thermo-mechanical simulation of a multichip press-packed IGBT. Solid-State Electronics. 1998;**42**(12):2303-2307

[22] Pirondi A, Nicoletto G, Cova P, Pasqualetti M, Portesine M. Thermo-mechanical finite element analysis in press-packed IGBT design. Microelectronics Reliability. 2000; **40**:1163-1172

[23] Cova P, Nicoletto G, Pirondi A, et al. Power cycling on press-pack IGBTs: Measurements and thermomechanical simulation. Microelectronics Reliability. 1999;**39**(6):1165-1170

[24] Zhao Z, Deng E, Zhang P, et al. Review of the difference between the press pack IGBT using for converter valve and for DC breaker. Diangong Jishu Xuebao/Transactions of China Electrotechnical Society. 2017;**32**(19):125-133

Section 2

Construction of FETs

Chapter 6

$Ge_{0.83}Sn_{0.17}$ P-Channel Metal-Oxide-Semiconductor Field-Effect Transistors: Impact of Sulfur Passivation on Gate Stack Quality

Dian Lei and Xiao Gong

Additional information is available at the end of the chapter

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Abstract

The effect of sulfur passivation of the surface of $Ge_{0.83}Sn_{0.17}$ is investigated. X-ray photoelectron spectroscopy (XPS) was used to examine the interfacial property between HfO_2 and $Ge_{0.83}Sn_{0.17}$. Sulfur passivation is effective in reducing both the Ge oxides and Sn oxides formation and the Sn atoms segregation. In addition, sulfur passivation reduces the interface trap density D_{it} at the $HfO_2/Ge_{0.83}Sn_{0.17}$ interface from the valence band edge to the midgap. After the implementation of sulfur passivation, $Ge_{0.83}Sn_{0.17}$ p-MOSFETs show improved subthreshold swing S and effective hole mobility μ_{eff}. 25% μ_{eff} enhancement can be observed in $Ge_{0.83}Sn_{0.17}$ p-MOSFETs with sulfur passivation at a high inversion carrier density N_{inv} of 1×10^{13} cm^{-2}.

Keywords: GeSn, p-MOSFETs, sulfur passivation, XPS, dangling bond

1. Introduction

Materials with high carrier mobilities such as germanium (Ge) could replace Silicon (Si) as the channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs) for future high performance logic applications [1–10]. Recently, germanium-tin (GeSn) was reported to have a higher hole mobility than Ge and is a promising channel material for p-channel MOSFETs (p-MOSFETs) [11–18].

Theoretical calculation [11] shows that the light hole effective mass of GeSn decreases with increasing Sn composition. It is also demonstrated experimentally [19] that increasing Sn

composition in GeSn p-MOSFETs increases the effective hole mobility. However, due to the low surface energy and large covalent radius of Sn, Sn atoms may segregate to the surface during growth of GeSn [20–22]. Hence, the thermal stability may be worse at a higher Sn composition. Li et al. reported that a Sn-rich surface layer would form when $Ge_{0.922}Sn_{0.078}$ is annealed at 620°C [23]. A similar phenomenon occurs on $Ge_{0.915}Sn_{0.085}$ surface after annealing at 500°C [24]. For Sn composition as high as 17%, self-assembled Sn wires can form at an annealing temperature as low as 280°C [25]. Severe Sn segregation may reduce carrier mobility and degrade the drive current in MOSFETs. Therefore, in order to achieve high performance GeSn p-MOSFETs with high Sn composition, a fabrication process with low thermal budget may be required to maintain a good quality of the GeSn channel material and the GeSn/high-*k* dielectric interface.

Various passivation techniques have been demonstrated to be effective in improving the gate stack quality of both Ge and GeSn channel p-MOSFETs, such as Si_2H_6 passivation [12, 17], Ge capping [26], $GeSnO_x$ passivation [27, 28], and sulfur passivation [15, 29, 30]. Among these passivation techniques adopted for GeSn p-MOSFETs fabrication, Si_2H_6 passivation and $GeSnO_x$ passivation require a process temperature higher than 370°C and 400°C, respectively. It has already been reported that Sn can segregate out to the GeSn surface during Si passivation process at a temperature of 370°C and degrades the device performance [17]. Therefore, low temperature passivation technique was investigated in this work for the fabrication of GeSn p-MOSFETs with Sn composition of 17%.

The adsorption of sulfur atoms is a promising route to chemically and electrically passivate the highly reactive Ge and GeSn surface [15, 29–31]. Compared with other passivation techniques, room temperature sulfur passivation using $(NH_4)_2S$ solution has several advantages: (1) GeSn surface could be effectively passivated through the formation of covalent S-Ge and S-Sn bond. This will reduce oxide formation which degrades device performance; (2) The formed sulfur passivation layer is very thin with very little increase on the effective oxide thickness (EOT); (3) Sn segregation can be suppressed during the passivation process owning to a lower thermal budget. Sulfur passivation has already been implemented into $Ge_{0.947}Sn_{0.053}$ p-MOSFETs fabrication and demonstrated enhanced peak hole mobility as compared with Si_2H_6 passivation [15]. However, the mechanism of the effect of sulfur passivation on the GeSn/HfO_2 interface quality has not been investigated. In addition, the impact of sulfur passivation on the reduction of D_{it} was not quantified.

In this chapter, sulfur passivation of GeSn surface at room temperature was investigated and implemented in the fabrication of $Ge_{0.83}Sn_{0.17}$ p-channel MOSFETs. To study the impact of sulfur passivation on the quality of high-*k* dielectric/GeSn interface, extensive X-ray photoelectron spectroscopy (XPS) analysis was carried out. Sulfur passivation is found to be effective in suppressing the formation of Sn oxides and Ge oxides, and Sn surface segregation. In addition, sulfur passivation helps to reduce the high-*k* dielectric/GeSn interface trap density D_{it} as extracted using the conductance method. Material study of nickel stanogermanide [Ni(GeSn)] contact formation at low temperatures was also performed for low resistivity [Ni(GeSn)] S/D contact. The sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFETs exhibit smaller subthreshold swing *S*, higher intrinsic transconductance $G_{m,int}$, and higher effective hole mobility μ_{eff} as compared to the non-passivated control. At a high inversion carrier density of 1×10^{13} cm^{-2}, sulfur passivation enhances μ_{eff} by 25% as compared with the non-passivated control.

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2. Experiment

2.1. Material growth and characterization of $Ge_{0.83}Sn_{0.17}$ substrate

The high quality $Ge_{0.83}Sn_{0.17}$ sample was grown using molecular beam epitaxy (MBE). 4-inch (001)-oriented Ge wafers with n-type doping concentration of 5×10^{16} cm^{-3} were used as the starting substrates. After the cyclic cleaning of Ge substrates using dilute hydrofluoric acid (DHF) ($HF:H_2O = 1:50$) and deionized (DI) water, the unintentionally p-type doped $Ge_{0.83}Sn_{0.17}$ film was grown on the Ge substrate using the solid source low temperature MBE system [32, 33]. The growth temperature was set at 100°C. 99.9999% pure Ge and 99.9999% pure Sn were used as Ge and Sn sources, respectively. The growth chamber has a base pressure of 3×10^{-10} Torr. $Ge_{0.83}Sn_{0.17}$ film with the thickness of 10 nm was grown on the Ge substrates. **Figure 1** shows the 5 × 5 μm AFM scan of the as-grown $Ge_{0.83}Sn_{0.17}$ surface. The surface is very smooth with a root-mean-square (RMS) roughness as small as 0.198 nm. High-resolution transmission electron microscopy (HRTEM) was employed to analyze the crystalline quality of the as-grown $Ge_{0.83}Sn_{0.17}$ sample. **Figure 2(a)** shows a low magnification cross-sectional TEM (XTEM) image of an as-grown $Ge_{0.83}Sn_{0.17}$ sample, indicating that the GeSn surface is smooth. The GeSn layer thickness is ~10 nm. The high resolution TEM (HRTEM) image in **Figure 2(b)** shows the smooth $Ge_{0.83}Sn_{0.17}$ surface. In addition, very clear lattice fringes and defect-free GeSn/Ge interface can be observed, as shown in the HRTEM image of **Figure 2(c)**.

High resolution X-ray diffraction (HRXRD) was also used to analyze the Sn composition and strain property of the as-grown $Ge_{0.83}Sn_{0.17}$ substrate. **Figure 3(a)** shows the (004) ω-2θ rocking scan of the as-grown sample. Both Ge and GeSn peaks are well-defined. The peak at smaller 2θ value is the GeSn peak. The relative broad full-width-half-maximum (FWHM) is due to the thin GeSn layer thickness (~10 nm). (115) reciprocal space mapping (RSM) of an as-grown $Ge_{0.83}Sn_{0.17}$/Ge (001) sample is shown in **Figure 3(b)**. The GeSn film is fully strained to the Ge substrate and the substitutional Sn composition is calculated to be 17% from XRD measurement.

Figure 4(a) summarizes the key process steps for fabricating $Ge_{0.83}Sn_{0.17}$ p-MOSFETs. After the MBE growth of ~10 nm $Ge_{0.83}Sn_{0.17}$ film on the lightly n-type doped Ge (100) substrate, pre-gate cleaning using DHF ($HF:H_2O = 1:50$) and DI water was performed. Two splits were

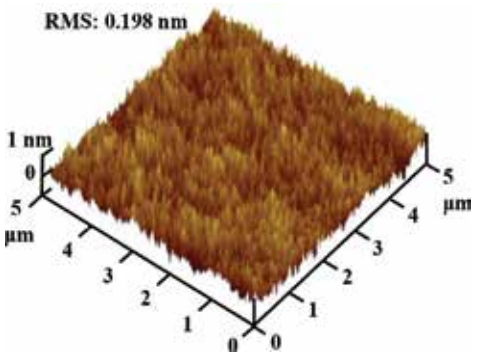

Figure 1. 5 × 5 μm AFM scan of the as-grown $Ge_{0.83}Sn_{0.17}$ substrate. The GeSn surface is very smooth with a RMS roughness as small as 0.198 nm.

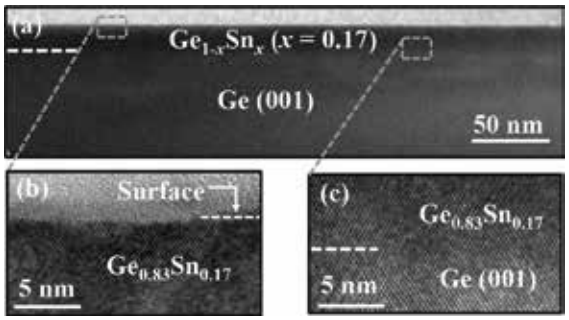

Figure 2. (a) Low magnification XTEM image of an as-grown $Ge_{0.83}Sn_{0.17}$ sample showing the smooth GeSn surface. High magnification XTEM images of the $Ge_{0.83}Sn_{0.17}$ sample shows (c) the zoom-in view of smooth GeSn surface and (d) defect-free $Ge_{0.83}Sn_{0.17}$/Ge interface.

introduced: one with 10 minutes sulfur passivation using $(NH_4)_2S$ solution (24% by weight) at room temperature (25°C) and the other one without sulfur passivation. After that, the samples were loaded into the atomic layer deposition (ALD) chamber immediately to avoid surface oxidation due to air exposure. Surface treatment was done using Trimethylaluminum (TMA) as precursor with pulse duration of 30 ms. This was followed by deposition of 3 nm-thick hafnium dioxide (HfO_2) at 250°C using Tetrakis (dimethylamido) hafnium and H_2O as precursors. The total ALD process duration including the pumping and venting steps is ~ 15 min. After that, 110 nm-thick tantalum nitride (TaN) was deposited using a reactive sputtering system. The metal gate was then patterned by photolithography and etched using chlorine (Cl_2)-based plasma. A 10 nm-thick nickel (Ni) was then deposited using e-beam evaporator and the self-aligned Ni(GeSn) metallic contact was formed by rapid thermal annealing (RTA) at 250°C for 30 s in the N_2 ambient. Finally, excess Ni was removed by selective wet etch using concentrated sulfuric acid (H_2SO_4) (96% by weight). The maximum processing temperature of

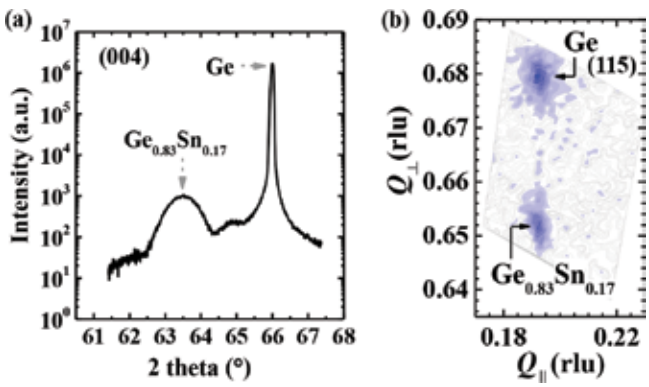

Figure 3. (a) (004) rocking scan of the as-grown sample shows both the $Ge_{0.83}Sn_{0.17}$ and Ge peaks. The well-defined GeSn peak indicates the good crystalline quality of the GeSn layer. The peak is relatively broader than the Ge peak because of the thin layer thickness of the GeSn layer. (b) (115) RSM showing that the $Ge_{0.83}Sn_{0.17}$ film is fully strained to the Ge (001) substrate. The substitutional Sn composition is calculated to be 17%. Device fabrication of $Ge_{0.83}Sn_{0.17}$ p-MOSFETs.

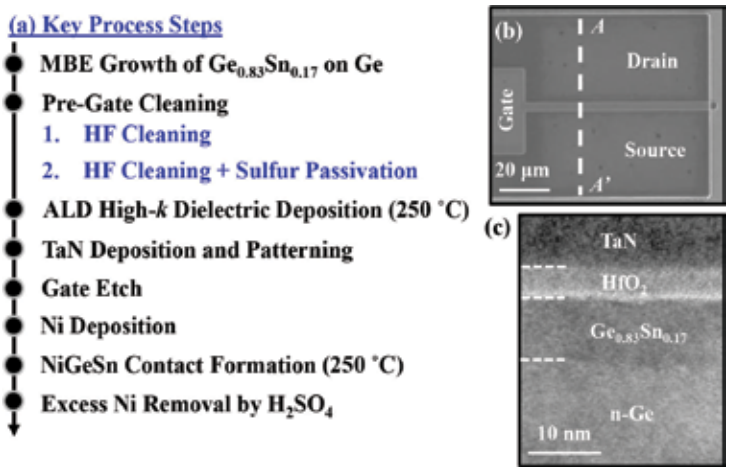

Figure 4. (a) Process flow for fabricating $Ge_{0.83}Sn_{0.17}$ channel p-MOSFETs where a sulfur passivation step was introduced prior to the deposition of high-k gate dielectric (HfO_2). The maximum processing temperature is 250°C. (b) Top-view SEM image showing a completed $Ge_{0.83}Sn_{0.17}$ p-MOSFET with self-aligned NiGeSn S/D contacts. (c) HRTEM image of a $Ge_{0.83}Sn_{0.17}$ channel p-MOSFET as seen in a cross-section along the dash line *AA'* in (b).

the whole fabrication process was 250°C to limit out-diffusion of Sn to the channel surface or into the gate dielectric. A top-view scanning electron microscopy (SEM) image of a completed $Ge_{0.83}Sn_{0.17}$ p-MOSFET with a gate length L_G of 4 μm is shown in **Figure 4(b)**. **Figure 4(c)** shows a HRTEM image of the transistor along the dash line *A-A'* indicated in **Figure 4(b)**.

3. Results and discussion

3.1. Sulfur-passivated gate stack study

The (001) surface of a diamond-structure semiconductor has two dangling bonds per surface atom. GeSn grown on Ge (001) surface has a (001) surface as shown in the atomic structure in **Figure 5(a)** viewed into the [110] direction. One monolayer (ML) of a Group VI element can passivate all the dangling bonds by occupying the bridge site in a (1 × 1) geometry [34, 35]. Sulfur atoms could obtain an ideal (1 × 1) termination of the bivalent (001) surfaces of silicon and Ge. Although sulfur could desorb from the Si surface at room temperature or diffuse into the Si bulk during heating [36], Weser et al. found that an ordered (1 × 1) structure with one sulfur atom bonded on a bulk-like bridge site could be achieved by introducing elemental sulfur atoms on the Ge (001) surface under ultrahigh vacuum (UHV) condition [34, 35]. The formation of Ge-S-Ge bridge bonds after a treatment in $(NH_4)_2S$ solution has also been reported based on various characterization techniques, such as photoelectron spectroscopy [37], ion scattering spectroscopy [38], as well as X-ray standing wave measurements [39]. Similarly, sulfur passivation should also be able to passivate the GeSn (001) surface through the formation of S-Ge and S-Sn covalent bonds which suppress the formation of Ge and Sn oxides at the surface, as illustrated in the atomic schematic shown in **Figure 5(b)**. In this Section, the

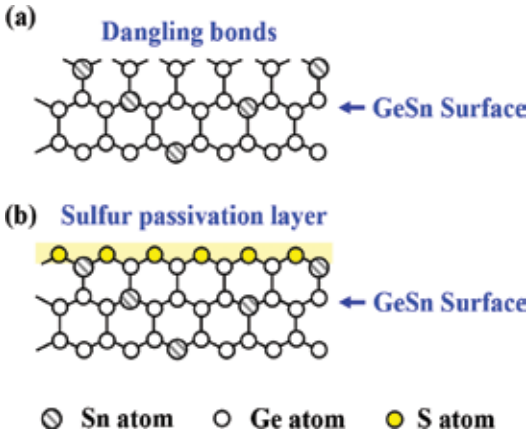

Figure 5. Side view into the [110] direction of (a) non-passivated (1 × 1) and (b) the sulfur-passivated GeSn (001) surfaces.

effectiveness of sulfur passivation on the gate stack of GeSn p-MOSFETs is investigated using XPS. The interface trap density value is also extracted using conductance method and compared with the non-passivated control.

3.2. XPS study on the effect of sulfur passivation

To investigate the interfacial property between the high-*k* dielectric and $Ge_{0.83}Sn_{0.17}$ after sulfur passivation, XPS measurement was carried out to study the change of the interfacial chemical bonds. Two blanket $Ge_{0.83}Sn_{0.17}$ samples were prepared for the measurement. After the cyclic DHF (1:50) cleaning, one of the sample went through 10 minutes aqueous $(NH_4)_2S$ solution (24% by weight) and the other one did not. After that, an ultra-thin (~1 nm) HfO_2 layer was deposited by ALD on these two samples. The HfO_2 layer thickness should be smaller than the XPS information depth [40]. XPS characterization was then performed using a VG ESCALAB 220i–XL imaging XPS system. Monochromatic aluminum (Al) Kα X-ray (1486.7 eV) was used to obtain the core level spectra of these samples. Binding energy was calibrated with standard samples for some pure metals. The binding energy of Carbon (C) *1 s* from adventitious hydrocarbon surface contamination was set at 285.0 eV for further charge correction.

In order to confirm the incorporation of S after the $(NH_4)_2S$ passivation, core level XPS spectra of the S *2p* peak were captured for HfO_2-capped $Ge_{0.83}Sn_{0.17}$ blanket samples with and without sulfur passivation, as shown in **Figure 6(a)**. The black curve represents the S *2p* signal obtained from the non-passivated $Ge_{0.83}Sn_{0.17}$ sample. The circles are the raw data points obtained from the sulfur-passivated sample. Gaussian and Lorentzian line shapes with a Shirley background subtraction were used to fit the raw data. The blue line is the overall fitting of the core level spectra and the gray lines are the fitted peak components. For the S *2p* core level spectra, the well-resolved two peaks correspond to S $2p_{1/2}$ (163.4 ± 0.02 eV) and S $2p_{3/2}$ (162.0 ± 0.02 eV) [41]. The S *2p* signal obtained from the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ sample indicates that S is introduced onto the GeSn surface by the $(NH_4)_2S$ treatment and is still present after the deposition of HfO_2. **Figure 6(b)** shows N *1 s* core level spectra for both samples. The N *1 s*

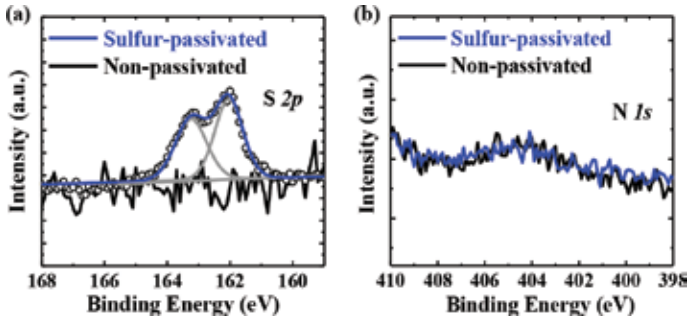

Figure 6. (a) S 2*p* core level XPS spectra for ~1 nm HfO_2-capped $Ge_{0.83}Sn_{0.17}$ samples with and without sulfur passivation. The circles, blue lines and gray lines are the raw data points, the overall fitting curves, and the S $2p_{1/2}$ or S $2p_{3/2}$ peak components, respectively. The black curve represents the S 2*p* signal obtained from the non-passivated sample. (b) N 1*s* core level spectra for both samples.

peak (399.0 ± 0.02 eV) [41] on the sulfur-passivated sample is not observed, indicating that nitrogen is not incorporated. The sulfur passivation layer thickness is calculated using two different photoelectron peaks of the same element at kinetic energies E_1 and E_2 (E_1 and E_2 have sufficiently large differences in λ) [42, 43]. Ge 3*d* and Ge $2p_3$ data (not shown) are used and the equation is shown below:

$$d = \cos\theta \cdot \frac{\lambda_A(E_1) \cdot \lambda_A(E_2)}{\lambda_A(E_1) - \lambda_A(E_2)} \cdot \ln\frac{I_B(E_1)}{I_B(E_2)}, \quad (1)$$

where $\lambda_A(E_1)$ and $\lambda_A(E_2)$ are the attenuation length of Ge 3*d* and Ge $2p_3$, $I'_B(E_1)$ and $I'_B(E_2)$ are corrected photoelectron intensities, and θ is take-off angle. The sulfur passivation layer thickness is calculated to be 0.44 nm using the Ge 3*d* and Ge $2p_3$ XPS signals.

Figure 7(a) and **(b)** show the Sn 3*d* core level spectra of HfO_2-capped $Ge_{0.83}Sn_{0.17}$ blanket samples with and without sulfur passivation, respectively. The circles, blue lines, and gray lines shown in **Figure 7** are the raw data points, the overall fitting curves, and fitted peak components, respectively. Due to spin orbit splitting, two separated Sn 3*d* peaks (Sn $3d_{3/2}$ and Sn $3d_{5/2}$) can be observed on both samples. The left shoulders, binding energy at 486.7 ± 0.2 eV and 494.9 ± 0.2 eV, can be attributed to the formation of Sn oxides (SnO_x) [41]. Similarly, **Figure 7(c)** and **(d)** show the Ge 3*d* core level spectra of HfO_2-capped $Ge_{0.83}Sn_{0.17}$ blanket samples with and without sulfur passivation, respectively. Ge oxides (GeO_2 and GeO_x) can also be observed in both samples. The Ge and Sn oxide signals can be detected on both samples and could come from two sources: (1) ALD HfO_2 deposition as H_2O pulses were introduced in the chamber with a temperature of 250°C, (2) sample transfer before loading into the XPS chamber as the samples were exposed to the air ambient. However, the intensities of both Ge oxides and SnO_x are reduced significantly after the sulfur passivation, indicating the effectiveness of sulfur passivation in suppressing both Ge oxides and SnO_x formation.

The native Ge and Sn oxides formation at the high-*k*/GeSn interface could result in high D_{it} value and gate leakage current. Lee et al. reported that the native Ge oxide could react with Ge at the interface and form GeO which is easily desorbed during thermal processing [44].

$$GeO_2 + Ge \rightarrow 2GeO(\uparrow). \quad (2)$$

This could generate a huge amount of interface states which degrade the gate stack quality [45]. The Sn oxide could also be detrimental to the GeSn gate stack as SnO_2 is known to exhibit metallic behaviour, which leads to high gate leakage current [46, 47]. Therefore, suppressing the Ge and Sn oxides formation is important for achieving good gate quality for $Ge_{0.83}Sn_{0.17}$ p-MOSFETs.

To quantify the impact of sulfur passivation on Ge oxides and SnO_x formation at the high-*k*/GeSn interface, angle-resolved XPS (ARXPS) was performed. Both SnO_x and Ge oxide signals can be detected. The ratio of oxidized Sn (or Ge) atoms to the total Sn (or Ge) atoms can be calculated using

$$\gamma_{Sn-O} = \frac{A_{Sn-O}}{A_{Sn-Sn} + A_{Sn-O}}, \quad (3)$$

$$\gamma_{Ge-O} = \frac{A_{Ge-O}}{A_{Ge-Ge} + A_{Ge-O}}, \quad (4)$$

where $A_{Sn\text{-}O}$, $A_{Sn\text{-}Sn}$, $A_{Ge\text{-}O}$, and $A_{Ge\text{-}Ge}$ are the normalized Sn-O peak area, normalized Sn-Sn peak area (also including Sn-Ge bonding), normalized Ge-O peak area, and normalized Ge-Ge peak area (also including Ge-Sn bonding), respectively [48]. With consideration of Scofield photoionization cross-sections and the transmission function of the spectrometer, $\gamma_{Sn\text{-}O}$ and $\gamma_{Ge\text{-}O}$ can be plotted as a function of the photoelectron take-off angle θ and are shown in **Figure 8**. The inset in **Figure 8** illustrates the definition of θ. θ of 0°, 30°, 45°, and 60° were used. It is observed that $\gamma_{Sn\text{-}O}$ and $\gamma_{Ge\text{-}O}$ increase with increasing θ. This is due to the fact that more Ge and Sn atoms at the surface get oxidized than those at the sub-surface. For larger θ, the information depth is smaller and ARXPS becomes more surface sensitive. For Ge oxides, the oxide percentages of the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ sample increase from 20 to 42% when θ increases from 0 to 60°. However, all the values are 10–20% smaller than those of the non-passivated one. A similar trend is also observed for SnO_x, and the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ sample shows more than 50% reduction in SnO_x percentage than the non-passivated one at all take-off angles. The reduction of oxide formation is more obvious in Sn atoms than Ge atoms. This reveals that sulfur passivation is more effective in suppressing Sn oxide formation than Ge oxide formation. The reduction of both Ge and Sn oxides can be ascribed to the formation of S-Ge and S-Sn bonds on the sample surface. Since both samples went through the DHF treatment, most native oxides were removed and the sample surface becomes H-terminated. As a result, the $Ge_{0.83}Sn_{0.17}$ sample surface has Ge-H, Sn-H bonds, and possibly Ge-O and Sn-O bonds due to the incomplete surface oxide removal in DHF [49]. After sulfur passivation, Ge-H bond (bond energy: 263 kJ/mol [50]) and Sn-H bond (bond energy: 264 kJ/mol) are replaced by more stable Ge-S bond (bond energy: 534 kJ/mol) and Sn-S bond (bond energy: 467 kJ/mol), respectively. The S passivation layer formed at the GeSn surface can suppress the further oxidation of sub-surface Ge and Sn atoms.

To further investigate the effect of sulfur passivation on the interface quality between the high-*k* dielectric and $Ge_{0.83}Sn_{0.17}$, the extent of surface segregation of Sn atom was analyzed

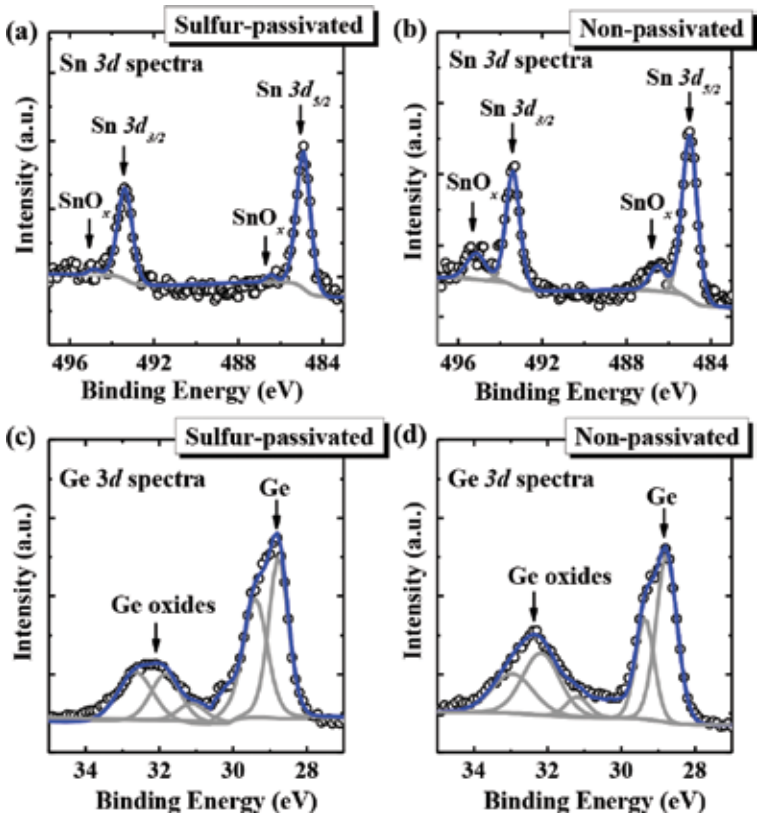

Figure 7. Sn 3*d* and Ge 3*d* core-level spectra of (a) and (c) sulfur passivated and (b) and (d) non-passivated $Ge_{0.83}Sn_{0.17}$ samples obtained by XPS. A 1 nm-thick HfO_2 was deposited on both samples.

using the obtained ARXPS data. The Ge and Sn atomic concentrations can be calculated using the stabilized Ge *3d* and Sn *3d* spectra. The atomic concentrations of Sn ($\gamma_{Sn/(Ge+Sn)}$) and Ge ($\gamma_{Ge/(Ge+Sn)}$) can be expressed as

$$\gamma_{Sn/(Ge+Sn)} = \frac{A_{Sn-Sn} + A_{Sn-O}}{A_{Sn-Sn} + A_{Sn-O} + A_{Ge-Ge} + A_{Ge-O}}, \quad (5)$$

$$\gamma_{Ge/(Ge+Sn)} = \frac{A_{Ge-Ge} + A_{Ge-O}}{A_{Sn-Sn} + A_{Sn-O} + A_{Ge-Ge} + A_{Ge-O}}, \quad (6)$$

and plotted as a function of θ. **Figure 9** shows $\gamma_{Ge/(Ge+Sn)}$ and $\gamma_{Sn/(Ge+Sn)}$ near the surface of $Ge_{0.83}Sn_{0.17}$ as a function of θ for both the sulfur-passivated and non-passivated samples. The calculated $\gamma_{Sn/(Ge+Sn)}$ increases with the increase of θ, indicating that surface segregation of Sn occurred in both samples. The Sn composition of the non-passivated $Ge_{0.83}Sn_{0.17}$ sample even exceeds 20% at θ of 60°. This is because Sn tends to segregate toward the surface, with the severity increasing at higher Sn compositions. Wang et al. reported that Sn segregation can occur at a temperature as low as 200°C for strained $Ge_{0.915}Sn_{0.085}$ grown on Ge [24]. Since our

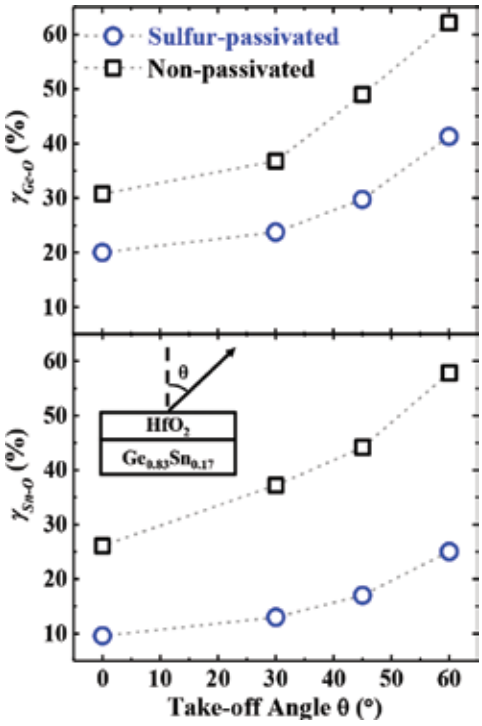

Figure 8. $\gamma_{Sn\text{-}O}$ and $\gamma_{Ge\text{-}O}$ calculated from angle-resolved XPS measurement for both the sulfur-passivated and non-passivated GeSn samples as a function of photoelectron take-off angle θ. The inset shows the definition of θ, which is set to be 0°, 30°, 45°, or 60° in the measurements.

$Ge_{0.83}Sn_{0.17}$ sample went through the ALD deposition process with a temperature of 250°C, Sn segregation could also occur. Although the segregation of Sn occurs on both GeSn samples, the calculated $\gamma_{Sn/(Ge+Sn)}$ of the sulfur-passivated GeSn sample is smaller than that of the non-passivated one at all take-off angles. The S passivation layer appears to suppress the underlying Sn atoms from segregating to the surface and from further oxidation during ALD. The good integrity of high-*k* dielectric/GeSn interface maintained by sulfur passivation through the prevention of Sn out-diffusion and interfacial oxidation may help to improve the carrier transport characteristics in transistors.

3.3. Extraction of interface trap density

In order to extract the D_{it} of $HfO_2/Ge_{0.83}Sn_{0.17}$ interfaces with and without sulfur passivation, $Ge_{0.83}Sn_{0.17}$ MOS capacitors (MOSCAPs) with 4 nm-thick HfO_2 were fabricated. TaN and Al were deposited as the front gate and backside metals by reactive sputtering, respectively. Low temperature *C-V* measurement with frequencies ranging from 10 kHz to 1 MHz was performed on the $Ge_{0.83}Sn_{0.17}$ capacitors. D_{it} was extracted using the conductance method [51]. At a particular gate bias, the peak of the G_p/ω versus frequency curve can be obtained at one sweeping frequency and is referring to the maximum of per-cycle energy loss. The per-cycle energy loss is due to charge trapping and detrapping at certain oxide-semiconductor

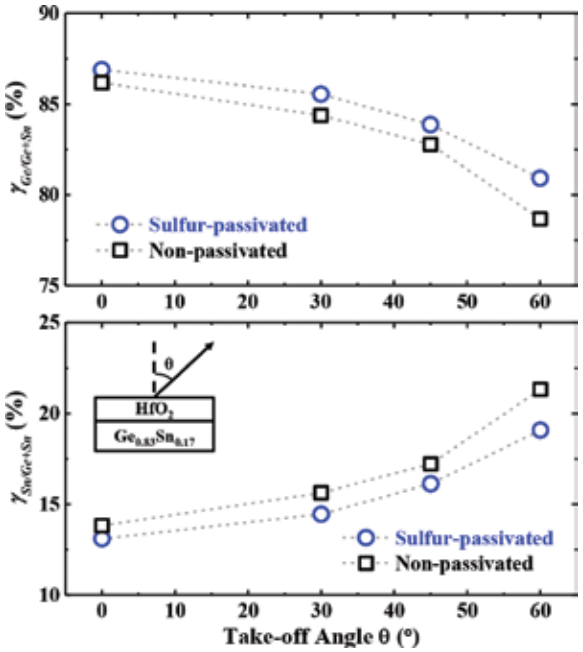

Figure 9. The Ge and Sn atomic concentrations at surface region of $Ge_{0.83}Sn_{0.17}$ as a function of photoelectron take-off angle θ, as determined by angle-resolved XPS.

interface and its maximum occurs when the energy level of the trap states is aligned with the semiconductor surface Fermi-level. The value of D_{it} can be extracted using the following equation:

$$D_{it} = 2.5 \cdot \frac{(G_p/\omega)_{max}}{qA}, \tag{7}$$

where $(G_p/\omega)_{max}$ is the peak energy loss value, q is the electronic charge, and A is the area of capacitor. The band-gap of fully compressively strained $Ge_{0.83}Sn_{0.17}$ on Ge (100) substrate is ~0.45 eV [52]. D_{it} values from the valence band edge to the midgap of GeSn for both sulfur-passivated and non-passivated GeSn capacitors are extracted and plotted as a function of energy in the GeSn band-gap as shown in **Figure 10**. For the sample with sulfur passivation, D_{it} of 10^{13} $cm^{-2}{\cdot}eV^{-1}$ was obtained at E-E_v of 0.13 eV. This is much smaller as compared with the non-passivated sample which has D_{it} of 6×10^{13} $cm^{-2}{\cdot}eV^{-1}$. In addition, sulfur passivation also leads to significant reduction in D_{it} near the valence band edge. Sulfur passivation suppresses Ge and Sn oxide formation and Sn out-diffusion, leading to the reduction of D_{it}. As a result, S of the sulfur-passivated GeSn p-MOSFETs is improved as compared with the non-passivated sample. In terms of the $Ge_{0.83}Sn_{0.17}$ p-MOSFETs, high density interface traps near the valence band edge can be charged when the device is biased to strong inversion, and degrade the effective hole mobility. In order to further improve the effective hole mobility of the $Ge_{0.83}Sn_{0.17}$ p-MOSFETs, further optimization and significant improvement are needed to reduce the D_{it} near the valence band for the high-k/GeSn gate stack.

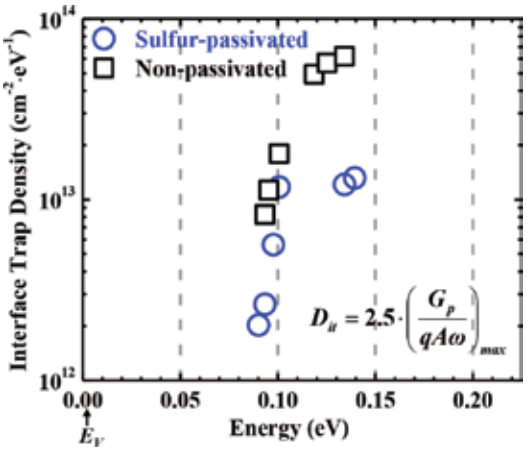

Figure 10. D_{it} distribution from valence band edge to the midgap of GeSn as a function of energy. The sulfur-passivated GeSn sample demonstrates reduced midgap D_{it} as compared to the non-passivated control.

3.4. Electrical characterization of $Ge_{0.83}Sn_{0.17}$ p-MOSFETs

I_{DS} - V_{GS} curves of $Ge_{0.83}Sn_{0.17}$ p-MOSFETs with and without sulfur passivation are shown in **Figure 11(a)**. The blue circles represent the sulfur-passivated sample and the black circles are the data points of the non-passivated one. Both devices have L_G of 4 μm and gate width W_G of 100 μm. The sulfur-passivated GeSn p-MOSFET exhibits S of 100 mV/decade. This is also the smallest reported S for any GeSn p-MOSFETs (non-passivated control shows S of 118 mV/decade). **Figure 11(b)** shows the output characteristics of the same devices in **Figure 11(a)**. 10% on-state current enhancement was demonstrated by sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET as compared to non-passivated control. Drive current of 32 μA/μm was achieved at a gate over drive of −1.0 V and V_{DS} of −1.0 V by the sulfur-passivated device. **Table 1** benchmarks S of the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFETs realized in this work with other GeSn p-MOSFETs reported using various

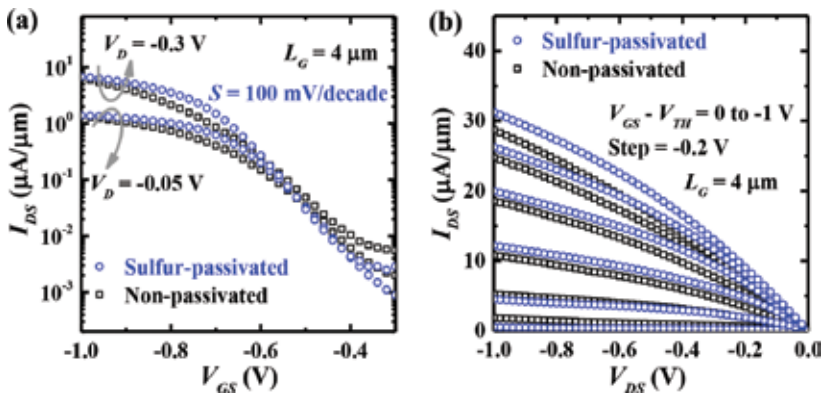

Figure 11. (a) I_{DS} - V_{GS} curves of the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET show S of 100 mV/decade and I_{ON}/I_{OFF} ratio of more than 3 orders of magnitude. S of the sulfur-passivated sample is smaller than that of the non-passivated one. (b) I_{DS} - V_{DS} curves of the same devices in (a).

Work	Passivation Technique	Sn composition (%)	*S* value
[12]	Si passivation	5.3	250
[15]	Sulfur passivation	4.2	220
[53]	Si passivation	3	113
[13]	No passivation	3	250
[16]	Si passivation	4.2	135
[17]	Si passivation	3	158
[14]	Si passivation	8	198
[18]	Ge capping	9	160
This work	Sulfur passivation	17	100

Table 1. ***S*** values of GeSn p-MOSFETs with different Sn compositions and passivation techniques.

passivation techniques [12–18, 53]. Despite the highest Sn composition, the $Ge_{0.83}Sn_{0.17}$ p-MOSFET realized in this work shows the smallest *S* as compared with the other GeSn p-MOSFETs. This could be attributed to the relative low D_{it} at the mid-gap (3.4×10^{12} cm^{-2} eV^{-1}) as compared with the other passivation techniques ($7–9 \times 10^{12}$ cm^{-2} eV^{-1}) [17]. This indicates the high quality of the $Ge_{0.83}Sn_{0.17}$ film grown by MBE which was maintained throughout the fabrication process using low processing temperatures, as well as the Ge and Sn oxides formation between $Ge_{0.83}Sn_{0.17}$ and high-*k* dielectric enabled by sulfur passivation. However, the D_{it} value near the valence band is still high (~1×10^{13} cm^{-2} eV^{-1}) as shown in the D_{it} plot in **Figure 10**. This may degrade the effective hole mobility which will be discussed in the following sections.

Figure 12 shows the capacitance *C* as a function of gate voltage V_{GS} for the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET (L_G = 8 μm, W_G = 100 μm) measured at frequency of 50 kHz, 100 kHz, and 1 MHz. The schematic in the inset illustrates the configuration for *C-V* measurement. A quantum-mechanical *C-V* simulator [54] was used to fit the measured inversion *C-V* curve at 100 kHz and the simulated data were plotted using solid line in **Figure 12**. In the *C-V* simulator, the *C-V* characteristics are obtained through the calculation of hole and electron distributions by solving Schrödinger's and Poisson's equations self-consistently with the Fermi-Dirac distribution. In the simulation, the heavy hole effective mass of 0.27 m_0 and light hole effective mass of 0.025 m_0 (m_0 is the free electron mass) were used for $Ge_{0.83}Sn_{0.17}$ channel [11]. From the simulated *C-V* curve, the equivalent oxide thickness (EOT) is extracted to be 7.5 Å. **Figure 13** shows the forward and backward inversion *C-V* sweeps of one $Ge_{0.83}Sn_{0.17}$ p-MOSFET (L_G = 8 μm, W_G = 100 μm) measured at a frequency of 100 kHz. The hysteresis is small, which indicates good dielectric quality with low density of oxide traps.

The $G_{m,int}$ curves versus V_{GS} at V_{DS} of −0.05 V for both sulfur-passivated and non-passivated devices are shown in **Figure 14**. L_G is 4 μm. $G_{m,int}$ is extracted using:

$$G_{m,int} = \frac{G_{m,ext}}{1 - 0.5 \cdot R_{SD} \cdot G_{m,ext}}, \tag{8}$$

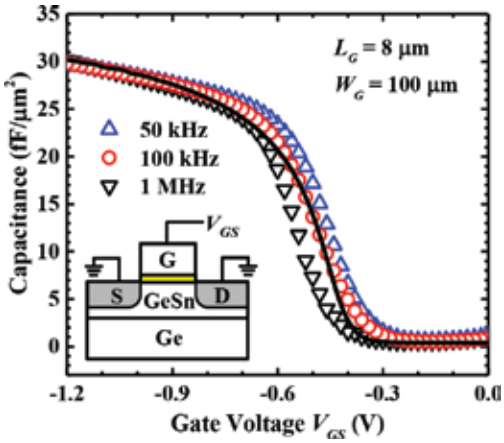

Figure 12. *C vs.* V_{GS} plot of a sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET measured at frequency of 50 kHz, 100 kHz, and 1 MHz. The measured data points are plotted as symbols. The solid curve is obtained using a quantum-mechanical *C-V* simulator to fit 100 kHz *C-V* curve. The inset shows the *C-V* measurement configuration.

where $G_{m,ext}$ is the measured extrinsic transconductance and R_{SD} is the source/drain resistance. Higher peak $G_{m,int}$ was achieved in sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET as compared with that of the non-passivated control. Improvement in $G_{m,int}$ is attributed to better HfO_2/GeSn interface achieved using sulfur passivation.

The μ_{eff} of $Ge_{0.83}Sn_{0.17}$ p-MOSFETs with and without sulfur passivation is extracted using the split *C-V* method:

$$\mu_{eff} = \frac{1}{W_G Q_{inv} \frac{\Delta R_{Total}}{\Delta L_G}}, \tag{9}$$

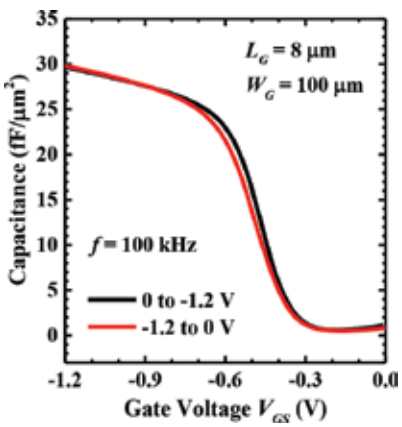

Figure 13. Forward and backward inversion *C-V* sweeps at 100 kHz for one $Ge_{0.83}Sn_{0.17}$ p-MOSFET with a L_G of 8 μm. The hysteresis is small.

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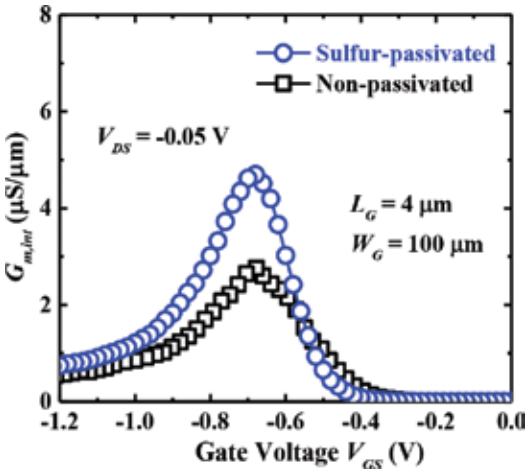

Figure 14. Intrinsic transconductance $G_{m,int}$ *vs.* V_{GS} characteristics for $Ge_{0.83}Sn_{0.17}$ p-MOSFETs with and without sulfur passivation at V_{DS} = −0.05 V. The L_G of the device is 4 μm and W_G is 100 μm.

where Q_{inv} is the inversion charge density in the GeSn channel, and $\Delta R_{Total}/\Delta L_G$ is the slope of total resistance (R_{Total}) versus L_G. Q_{inv} can be obtained by integrating the measured inversion *C-V* curve as shown in **Figure 12**. Using this approach, the impact of R_{SD} on extraction of hole mobility is taken out. **Figure 15** shows the extracted μ_{eff} versus the inversion carrier density (N_{inv}) for both the sulfur-passivated and non-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFETs. The sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET shows a peak hole mobility of 478 $cm^2/V{\cdot}s$ at N_{inv} of ~2×10^{12} cm^{-2}. At N_{inv} of 1×10^{13} cm^{-2}, 25% higher hole mobility is achieved by the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFET as compared with the non-passivated one. This is consistent with the peak intrinsic transconductance results shown in **Figure 14**.

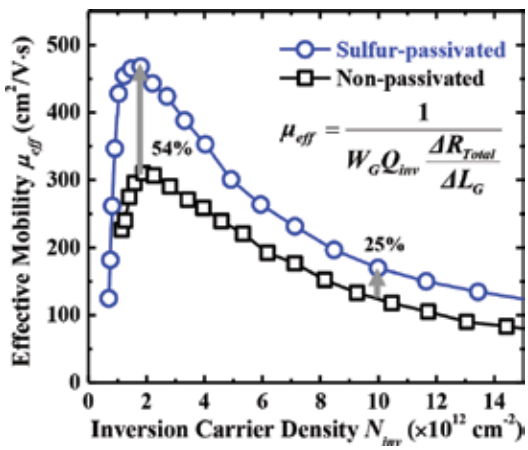

Figure 15. μ_{eff} *vs.* N_{inv} for $Ge_{0.83}Sn_{0.17}$ p-MOSFETs with and without sulfur passivation. The impact of R_{SD} on μ_{eff} extraction was taken out using the inset equation through the total resistance slope method.

4. Conclusion

Sulfur passivation and low temperature process modules are developed and used in the fabrication of $Ge_{0.83}Sn_{0.17}$ p-MOSFET. Reduction in S and improvement in peak $G_{m,int}$ and μ_{eff} are observed for the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFETs as compared with the non-passivated control. This is attributed to the effective suppression of Ge and Sn oxides formation, and suppression of Sn surface segregation by sulfur passivation. In addition, the effect of sulfur passivation on D_{it} reduction is also investigated. It is observed that sulfur passivation reduces the D_{it} from the valence band edge to midgap of GeSn. As a result, the lowest S of 100 mV/decade is achieved by the sulfur-passivated $Ge_{0.83}Sn_{0.17}$ p-MOSFETs. D_{it} level of 10^{13} cm^{-2} eV^{-1} in the sulfur-passivated sample is still very high. Further improvement to significantly reduce D_{it} is needed to increase the hole mobility.

Author details

Dian Lei* and Xiao Gong

*Address all correspondence to: leidian@u.nus.edu

Electrical and Computer Engineering, National University of Singapore, Singapore

References

[1] Pillarisetty R. Academic and industry research progress in germanium nanodevices. Nature. 2011;**479**(7373):324-328

[2] Pillarisetty R, Chu-Kung B, Corcoran S, Dewey G, Kavalieros J, Kennel H, Kotlyar R, Le V, Lionberger D, Metz M, Mukherjee N, Nah J, Rachmady W, Radosavljevic M, Shah U, Taft S, Then H, Zelick N, Chau R. High mobility strained germanium quantum well field effect transistor as the p-channel device option for low power (Vcc = 0.5 V) III-V CMOS architecture. IEEE IEDM Technical Digest. 2010:150-153

[3] Mitard J, Jaeger BD, Leys FE, Hellings G, Martens K, Eneman G, Brunco DP, Loo R, Lin JC, Shamiryan D, Vandeweyer T, Winderickx G, Vrancken E, Yu CH, Meyer KD, Caymax M, Pantisano L, Meuris M, Heyns MM. Record I_{ON}/I_{OFF} performance for 65nm Ge pMOSFET and novel Si passivation scheme for improved EOT scalability. IEEE IEDM Technical Digest. 2008:873-876

[4] Weber O, Bogumilowicz Y, Ernst T, Hartmann JM, Ducroquet F, Andrieu F, Dupre C, Clavelier L, Royer CL, Cherkashin N, Hytch M, Rouchon D, Dansas H, Papon AM, Carron V, Tabone C, Deleonibus S. Strained Si and Ge MOSFETs with high-*k*/metal gate stack for high mobility dual channel CMOS. IEEE IEDM Technical Digest. 2005:137-140

[5] Xie R, Phung TH, He W, Sun Z, Yu M, Cheng Z, Zhu C. High mobility high-*k*/Ge PMOSFETs with 1 nm EOT-new concept on interface engineering and interface characterization. IEEE IEDM Technical Digest. 2008:393-396

[6] Chern W, Hashemi P, Teherani JT, Yu T, Dong Y, Xia G, Antoniadis DA, Hoyt JL. High mobility high-*k*-all-around asymmetrically-strained germanium nanowire trigate p-MOSFETs. IEEE IEDM Technical Digest. 2012:387-390

[7] Hashemi P, Chern W, Lee HS, Teherani JT, Zhu Y, Gonsalvez J, Shahidi GG, Hoyt JL. Ultrathin strained-Ge channel p-MOSFETs with high-*k*/metal gate and sub-1-nm equivalent oxide thickness. IEEE Electron Device Letters. 2012;**33**(7):943-945

[8] Wu H, Si M, Dong L, Zhang J, Ye PD. Ge CMOS: Breakthroughs of nFETs (I_{max} = 714 mA/mm, G_{max} = 590 mS/mm) by recessed channel and S/D. IEEE Symposium on VLSI Technology Digest. 2014:96-97

[9] Gong X, Zhou Q, Owen MHS, Xu X, Lei D, Chen S-H, Tsai G, Cheng C-C, Lin Y-R, Wu C-H, Ko C-H, Yeo Y-C. InAlP-capped (100) Ge nFETs with 1.06 nm EOT: Achieving record high peak mobility and first integration on 300 mm Si substrate. IEEE IEDM Technical Digest. 2014:231-234

[10] Lee CH, Lu C, Nishimura T, Nagashio K, Toriumi A. Thermally robust CMOS-aware Ge MOSFETs with high mobility at high-carrier densities on a single orientation Ge substrate. IEEE Symposium on VLSI Technology Digest. 2014:144-145

[11] Low KL, Yang Y, Han G, Fan W, Yeo Y-C. Electronic band structure and effective mass parameters of $Ge_{1-x}Sn_x$ alloys. Journal of Applied Physics. 2012;**112**(10):103715

[12] Han G, Su S, Zhan C, Zhou Q, Yang Y, Wang L, Guo P, Wang W, Wong CP, Shen ZX, Cheng B, Yeo Y-C. High-mobility germanium-tin (GeSn) p-channel MOSFETs featuring metallic source/drain and sub-370 °C process modules. IEEE IEDM Technical Digest. 2011:402-404

[13] Gupta S, Chen R, Magyari-Kope B, Lin H, Yang B, Nainani A, Nishi Y, Harris JS, Saraswat KC. GeSn technology: Extending the Ge electronics roadmap. IEEE IEDM Technical Digest. 2011:398-401

[14] Liu M, Han G, Liu Y, Zhang C, Wang H, Li X, Zhang J, Cheng B, Hao Y. Undoped $Ge_{0.92}Sn_{0.08}$ quantum well pMOSFETs on (001), (011) and (111) substrates with in situ Si_2H_6 passivation: High hole mobility and dependence of performance on orientation. IEEE Symposium on VLSI Technology Digest. 2014:100-101

[15] Wang L, Su S, Wang W, Gong X, Yang Y, Guo P, Zhang G, Xue C, Cheng B, Han G, Yeo Y-C. Strained germanium–tin (GeSn) p-channel metal-oxide-semiconductor field-effect-transistors (p-MOSFETs) with ammonium sulfide passivation. Solid-State Electronics. 2013;**83**:66-70

[16] Gong X, Han G, Bai F, Su S, Guo P, Yang Y, Cheng R, Zhang D, Zhang G, Xue C, Cheng B, Pan J, Zhang Z, Tok ES, Antoniadis D, Yeo Y-C. Germanium-tin (GeSn) p-channel MOSFETs

fabricated on (100) and (111) surface orientations with sub-400 °C Si_2H_6 passivation. IEEE Electron Device Letters. 2013;**34**(3):339-341

[17] Guo P, Han G, Gong X, Liu B, Yang Y, Wang W, Zhou Q, Pan J, Zhang Z, Tok ES, Yeo Y-C. $Ge_{0.97}Sn_{0.03}$ p-channel metal-oxide-semiconductor field-effect transistors: Impact of Si surface passivation layer thickness and post metal annealing. Journal of Applied Physics. 2013;**114**(4):044510

[18] Huang YS, Huang CH, Lu FL, Lin CY, Ye HY, Wong IH, Jan SR, Lan HS, Liu CW, Huang YC, Chung H, Chang CP, Chu SS, Kuppurao S. Record high mobility (428cm^2/V-s) of CVD-grown Ge/strained $Ge_{0.91}Sn_{0.09}$/Ge quantum well p-MOSFETs. IEEE IEDM Technical Digest. 2016:822-825

[19] Liu Y, Yan J, Wang H, Zhang Q, Liu M, Zhao B, Zhang C, Cheng B, Hao Y, Han G. Strained GeSn p-channel metal-oxide-semiconductor field-effect transistors with *in situ* Si_2H_6 surface passivation: Impact of Sn composition. IEEE Transactions on Electron Devices. 2014;**61**(11):3639-3645

[20] Gurdal O, Desjardins P, Carlsson JRA, Taylor N, Radamson HH, Sundgren J-E, Greene JE. Low-temperature growth and critical epitaxial thicknesses of fully strained metastable $Ge_{1-x}Sn_x$ ($x \leq 0.26$) alloys on Ge(001)2×1. Journal of Applied Physics. 1998;**83**(1):162-170

[21] Oehme M, Kostecki K, Schmid M, Oliveira F, Kasper E, Schulze J. Epitaxial growth of strained and unstrained GeSn alloys up to 25% Sn. Thin Solid Films. 2014;**557**:169-172

[22] Johll H, Samuel M, Koo RY, Kang HC, Yeo Y-C, Tok ES. Influence of hydrogen surface passivation on Sn segregation, aggregation, and distribution in GeSn/Ge(001) materials. Journal of Applied Physics. 2015;**117**(20):205302

[23] Li H, Cui YX, Wu KY, Tseng WK, Cheng HH, Chen H. Strain relaxation and Sn segregation in GeSn epilayers under thermal treatment. Applied Physics Letters. 2013;**102**(25):251907

[24] Wang W, Li L, Zhou Q, Pan J, Zhang Z, Tok ES, Yeo Y-C. Tin surface segregation, desorption, and island formation during post-growth annealing of strained epitaxial $Ge_{1-x}Sn_x$ layer on Ge(001) substrate. Applied Surface Science. 2014;**321**:240-244

[25] Wang W, Li L, Tok ES, Yeo Y-C. Self-assembly of tin wires via phase transformation of heteroepitaxial germanium-tin on germanium substrate. Journal of Applied Physics. 2015;**117**(22):225304

[26] Merckling C, Sun X, Shimura Y, Franquet A, Vincent B, Takeuchi S, Vandervorst W, Nakatsuka O, Zaima S, Loo R, Caymax M. Molecular beam deposition of Al_2O_3 on p-Ge(001)/$Ge_{0.95}Sn_{0.05}$ heterostructure and impact of a Ge-cap interfacial layer. Applied Physics Letters. 2011;**98**(19):192110

[27] Zhao M, Liang R, Wang J, Xu J. Improved electrical properties of Ge metal-oxide-semiconductor devices with HfO_2 gate dielectrics using an ultrathin $GeSnO_x$ film as the surface passivation layer. Applied Physics Letters. 2013;**102**(14):142906

[28] Kato K, Taoka N, Asano T, Yoshida T, Sakashita M, Nakatsuka O, Zaima S. Formation of high-quality oxide/$Ge_{1-x}Sn_x$ interface with high surface Sn content by controlling Sn migration. Applied Physics Letters. 2014;**105**(12):122103

[29] Frank MM, Koester SJ, Copel M, Ott JA, Paruchuri VK, Shang H, Loesing R. Hafnium oxide gate dielectrics on sulfur-passivated germanium. Applied Physics Letters. 2006; **89**(11):112905

[30] Xie R, Zhu C. Effects of sulfur passivation on germanium MOS capacitors with HfON gate dielectric. IEEE Electron Device Letters. 2007;**28**(11):976-979

[31] Sioncke S, Ceuppens J, Lin D, Nyns L, Delabie A, Struyf H, De Gendt S, Müller M, Beckhoff B, Caymax M. Atomic layer deposition of Al_2O_3 on S-passivated Ge. Microelectronic Engineering. 2011;**88**(7):1553-1556

[32] D'Costa VR, Wang W, Zhou Q, Tok ES, Yeo Y-C. Above-bandgap optical properties of biaxially strained GeSn alloys grown by molecular beam epitaxy. Applied Physics Letters. 2014;**104**(2):022111

[33] D'Costa VR, Wang W, Zhou Q, Chan TK, Osipowicz T, Tok ES, Yeo Y-C. Compositional dependence of optical critical point parameters in pseudomorphic GeSn alloys. Journal of Applied Physics. 2014;**116**(5):053520

[34] Weser T, Bogen A, Konrad B, Schnell R, Schug C, Steinmann. Photoemission surface core-level study of sulfur adsorption on Ge(100). Physical Review B. 1987;**35**(15):8184

[35] Weser T, Bogen A, Konrad B, Schnell R, Schug C, Moritz W, Steinmann W. Chemisorption of sulfur on Ge(100). Surface Science. 1988;**201**(1-2):245-256

[36] Han M, Luo Y, Camillone N, Osgood R. Reaction of H_2S with Si(100). The Journal of Physical Chemistry B. 2000;**104**(28):6576-6583

[37] Maeda T, Takagi S, Ohnishi T, Lippmaa M. Sulfur passivation of Ge(001) surfaces and its effects on Schottky barrier contact. Materials Science in Semiconductor Processing. 2006; **9**(4):706-710

[38] Fleischmann C, Sioncke S, Couet S, Schouteden K, Beckhoff B, Müller M, Hönicke P, Kolbe M, Van Haesendonck C, Meuris M, Temst K, Vantomme A. Towards passivation of Ge(100) surfaces by sulfur adsorption from a $(NH_4)_2S$ solution: A combined NEXAFS, STM and LEED study. Journal of the Electrochemical Society. 2011;**158**(5):H589-H594

[39] Lyman P, Sakata O, Marasco D, Lee T-L, Breneman K, Keane D, Bedzyk M. Structure of a passivated Ge surface prepared from aqueous solution. Surface Science. 2000;**462**(1): L594-L598

[40] Watts JF, Wolstenholme J. Compositional depth profiling. In: An Introduction to Surface Analysis by XPS and AES. England: John Wiley & Sons, Ltd; 2005. pp. 79-111

[41] NIST X-ray Photoelectron Spectroscopy Database, Version 4.1. National Institute of Standards and Technology, Gaithersburg 2012; http://srdata.nist.gov/xps/

[42] Bernstein RW, Grepstad JK. XPS intensity analysis for assessment of thickness and composition of thin overlayer films: Application to chemically etched GaAs(100) surfaces. Surface and Interface Analysis. 1989;**14**(3):109-114

[43] Mihailova T, Velchev N, Krastev V, Marinova T. XPS study of residual oxide layers on p-GaAs surfaces. Applied Surface Science. 1997;**120**(3):213-219

[44] Lee CH, Tabata T, Nishimura T, Nagashio K, Kita K, Toriumi A. Ge/GeO_2 interface control with high pressure oxidation for improving electrical characteristics. ECS Transactions. 2009;**19**(1):165-173

[45] Kita K, Takahashi T, Nomura H, Suzuki S, Nishimura T, Toriumi A. Control of high-*k*/germanium interface properties through selection of high-*k* materials and suppression of GeO volatilization. Applied Surface Science. 2008;**254**(19):6100-6105

[46] Schulte-Braucks C, von den Driesch N, Glass S, Tiedemann A, Breuer U, Besmehn A, Hartmann J-M, Ikonic Z, Zhao Q, Mantl S. Low temperature deposition of high-*k*/metal gate stacks on high-Sn content (Si)GeSn-alloys. ACS Applied Materials & Interfaces. 2016;**8**(20):13133-13139

[47] Kılıç Ç, Zunger A. Origins of coexistence of conductivity and transparency in SnO_2. Physical Review Letters. 2002;**88**(9):095501

[48] Wang L, Wang W, Zhou Q, Pan J, Zhang Z, Tok ES, Yeo Y-C. Post-growth annealing of germanium-tin alloys using pulsed excimer laser. Journal of Applied Physics. 2015; **118**(2):025701

[49] Onsia B, Caymax M, Conard T, De Gendt S, De Smedt F, Delabie A, Gottschalk C, Heyns MM, Green M, Lin S, Mertens P, Tsai W, Vinckier C. On the application of a thin ozone based wet chemical oxide as an interface for ALD high-*k* deposition. Solid State Phenomena. 2005;**103**:19-22

[50] Luo Y-R. Comprehensive Handbook of Chemical Bond Energies. CRC press; 2007

[51] Nicollian EH, Goetzberger A. The Si-SiO, interface-electrical properties as determined by the metal-insulator-silicon conductance technique. The Bell System Technical Journal. 1967;**46**(6):1055-1033

[52] Yahyaoui N, Sfina N, Lazzari JL, Bournel A, Said M. Band engineering and absorption spectra in compressively strained $Ge_{0.92}Sn_{0.08}$/Ge (001) double quantum well for infrared photodetection. Physica Status Solidi C. 2014;**11**(11-12):1561-1565

[53] Liu B, Zhan C, Yang Y, Cheng R, Guo P, Zhou Q, Kong EYJ, Daval N, Veytizou C, Delprat D, Nguyen BY, Yeo Y-C. Germanium multiple-gate field-effect transistor with *in situ* boron-doped raised source/drain. IEEE Transactions on Electron Devices. 2013; **60**(7):2135-2141

[54] Yang K, King Y-C, Hu C. Quantum effect in oxide thickness determination from capacitance measurement. IEEE Symposium on VLSI Technology Digest. 1999:77-78

Chapter 7

Graphene Field-Effect Transistor for Terahertz Modulation

Qi-Ye Wen, Yu-Lian He, Jing-Bo Liu, Qi Mao,
Qing-Hui Yang, Zhi Chen and Huai-Wu Zhang

Additional information is available at the end of the chapter

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Abstract

The real-world applications of terahertz (THz) technology necessitate versatile adaptive optical components, for example, modulators. In this chapter, we begin with a brief review on different techniques for THz modulation. After that, we introduce the extraordinary features of graphene along with its advantages and disadvantages as channel materials for field effect transistor (FET). We then discuss two types of graphene FET-based THz modulators, one is rigid and another is flexible. The feasibility of the high-quality THz modulators with different graphene FET structures has been successfully demonstrated. It is observed that by tuning the carrier concentration of graphene by electrical gating, the THz modulation can be obtained with relatively large modulation depth, broad width band, and moderate speed. This chapter helps the reader in obtaining guidelines for the proper choice of a specific structure for THz modulator with graphene FET.

Keywords: graphene, field effect transistor, terahertz, modulator, high-K dielectric layer, flexible

1. Introduction

The terahertz region of the electromagnetic spectrum roughly extends from 0.1 to 10 THz, corresponding to wavelengths from 3 mm to 30 μm. Terahertz (THz) waves interact with a plethora of materials including solid state, chemical, and biological systems. Consequently, THz waves offer numerous applications including material characterization, imaging, wireless communication, and so on [1–4]. Such real-world applications of THz technology necessitate versatile adaptive optical components such as modulators, filters, lens, switches, waveguide,

polarizer, and so on. Among all these desired THz components and devices, modulators stand at on the focus of current interest [5]. Modulators can be used to control the amplitude, phase, polarization state, spatial propagation direction, pulse shape, and many more characteristic properties of electromagnetic waves and thus act as essential parts of sophisticated THz application systems such as wireless telecommunication or security imaging [6].

However, unlike the optical or microwave regime where active modulators are well established, the THz frequency regime is still in great demand for efficient, fast, and versatile active light modulators [6]. This is mainly due to the lack of natural materials that have tunable electromagnetic response to THz wave [5]. Nevertheless, materials including semiconductors [7, 8], metamaterials [9–12], superconductors [13, 14], and phase-transition materials [15, 16] have been intensively explored to control and manipulate THz wave with great progress being made in this direction. Modulators can be categorized by the technique or material system, which is employed to modulate the wave, for example, optical, electronic, thermal, and magnetic modulators.

The all-optical approach is an effective and attractive method to fabricate THz modulators, especially those with broadband or spatial operating features. Semiconductors, especially high-resistive (HR) silicon, have proven to be suitable for all-optical modulation of THz wave by converting photons into electrons upon optical illumination [17]. Generally, the pump laser produces a temporary region of high absorption or reflectance on semiconductor. THz wave, co-projected on this area, is thus modulated [18]. As a result, all optical spatial THz modulators, based on a bare silicon wafer, have previously been proposed to realize photo-designed THz devices [19] or reconfigurable quasi-optical THz components [20, 21]. Si is an attractive candidate for optical opponents because it is earth abundant, chemically stable, and has a suitable band gap. Silicon-based THz devices are particularly desirable as they would enable interfacing with existing and emerging Si-based optoelectronics, thereby providing potential low-cost route toward applications. However, a silicon wafer exhibits strong reflection to both optical light (~40%) and THz radiation (~30%), which greatly limits the achievable tunability and versatility. Xie et al. verified that the modulation depth (MD) of silicon wafer to THz wave is only 19.9% under 800 mW femtosecond laser, although this value could be 98.6% if the pump laser intensity is high enough [21]. Very recently, plasmonic layers [22], graphene [23, 24], and even thin organic layers [25] have been fabricated on the surface of Si to enhance the modulation properties. Si modulators with these additional layers can work under lower pumping power, while having the same or even two to four times larger modulation depth. Very recently, Qi-Ye Wen and his co-workers demonstrated an interesting Si nanostructure for optically driven THz modulators [26]. They showed that nanotip (SiNT) arrays made from silicon wafer can be utilized as antireflection layers for both THz wave and visible light to achieve a low-loss and spectrally broadband THz modulator with a remarkably enhanced MD. Instead of fabricating heterogeneous materials on silicon, the nanotips are directly etched from the Si substrate and thus are structurally stable. Compared with the modulators fabricated on bare silicon, a nearly three times larger MD is achieved with the SiNT modulator. Crucially, the intrinsic THz transmission of the SiNT modulator is as high as 90% due to a strong antireflection effect arising from the nanotip layer as a result of the formation of graded refractive index on the Si surface.

One disadvantage of the semiconductor-based all-optical THz modulators is its relatively low modulation speed. The ultimate modulation speed is decided by the carrier recombination

time of semiconductors, which for intrinsic or HR silicon is beyond 10 μs, limiting the modulation speed to a maximum of ~100 kHz. Though gallium arsenide (GaAs) has very short carrier lifetime (10–100 ps), it requires high-power pulsed laser excitation up to 1 kW/cm^2 to achieve similar results as Si [27]. The reason for this is that the carrier lifetime of semiconductor affects the modulation depth and speed in an opposite way. Further research is ongoing to overcome this problem [27].

Another method of THz modulation is to thermally tune the electrical conductivity and thus the optical response of semiconductors or metal oxides, especial those materials with insulator-metallic phase transition [15, 28–31]. Vanadium dioxide (VO_2), for example, is a typical phase transition material that exhibits a reversible first-order phase transition from an insulating state to a metallic state above room temperature (~68°C). Associated with this metal-insulator transition (MIT) is a lattice structural transition from the monoclinic to tetragonal, a change of conductivity by 3–5 orders of magnitude and significant changes of the optical properties at all wavelengths. Since the insulated state is transparent while conductive state is opaque to THz wave, the THz transmission can thus be dynamically modified from transparent to reflecting modes by controlling the phase transition of the VO_2 film. VO_2 films, separately or integrated with resonant element (e.g., metamaterials), have already been used to control and manipulate THz wave [15, 30, 32, 33].

Although great progress has been made in optically and thermally driven THz modulators, an all-electronic approach is more interesting and attractive for the real application. It is well known that the carrier concentration in semiconductors can be tuned by electric injection or depletion of charge carriers. It is proved that THz wave can be manipulated by the use of two-dimensional electron gases (2DEGs) in semiconductors [7, 8]. A semiconductor-based field-effect transistor (FET) is a very useful architecture to fabricate effective THz modulators.

2. Graphene and graphene field-effect transistors

Graphene is a quasi-two-dimensional isolated monolayer of carbon atoms that are arranged in a hexagonal lattice. It is well known for its remarkable electron mobility at room temperature, with reported values in excess of 15,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [34]. Hole and electron mobilities were expected to be nearly identical. Graphene holds great promise for various material/device applications, including solar cells [35], light-emitting diodes (LED), touch panels, and smart windows or phonesal [36].

Graphene is a zero-band-gap semiconductor where conduction and valence bands meet at the Dirac points. The band gap is an extremely important characteristic of the semiconductor for transistor application, which enables the transistor device to turn off and minimizes leakage current at off state. In this circumstance, the gapless band structure of single-layer graphene makes it unsuitable for the direct use of graphene- based field-effect transistors (FET), though it is one of the most widely discussed applications in electronics. In order to overcome the challenges faced in incorporating graphene into microelectronic applications, great efforts have gone into developing three main aspects including developing a synthesis technique to manufacture graphene over wafer-scale areas, forming a high-quality gate dielectric on the surface of graphene, and, most importantly, opening an energy band gap in graphene. This

results in the observation that narrow ribbon widths down to less than 10 nm are required to open a band gap in graphene and achieve an acceptable level of low off currents. However, fabricating of narrow ribbons of that dimension is a big challenge even with current advanced lithographic techniques [37, 38].

The zero-band-gap characteristic means that the density of states (DOS) in graphene is linear with respect to the energy level. Therefore, gate voltage can modulate the DOS linearly to enable modulation of carrier (current) in the channel. In other words, graphene-based field-effect transistor (GFET) can be used to tune the carrier concentration in graphene by applying a voltage at the gate, making it possible to modulate the absorption/transmission of THz wave through the devices. Recently, such a graphene-based THz modulator was demonstrated by Sensale-Rodriguez et al. and Maeng et al. [39, 40]. It is reported that the transmission of THz wave through graphene can be controlled by electrically tuning the density of states available for intra-band transitions. Though the modulation depth and speed are limited to 15% and 20 kHz by this electrical device prototype, it opens a new direction for graphene application in a transistor structure [39, 40].

3. Enhanced GFET THz modulator with high-k dielectric layer

In most GFET devices, ~300-nm SiO_2 was used as the gate dielectric on top of a p-type silicon (p-Si) substrate. However, when used as a THz broadband modulator, GFET with graphene/~300 nm SiO_2/p-Si structures has drawbacks such as high switching voltage, small modulation depth, and slow modulation speed [39, 40]. Alternatively, Al_2O_3 with a dielectric constant of 7.5 is a high-κ material with numerous outstanding dielectric properties in comparison with SiO_2 [41]. In this chapter, we introduce a high-efficiency broadband THz wave modulator with quicker modulation speed and larger modulation depth by using Al_2O_3-based large-area graphene GFET device. The modulator consists of graphene monolayer/~60 nm Al_2O_3/p-Si structures. In our device, an intensity modulation depth of 22% (1% per 1.36 V) and a modulation speed of 170 kHz have been successfully achieved, which are notable improvements from previously reported 15% and 20 kHz, respectively, in the broadband modulators with graphene/~95 nm SiO_2/Si structures [39].

3.1. Fabrication and characteristics of the enhanced THz modulator

The native oxide layer on the (100) p-Si (ρ~1–10 Ω-cm) substrate was dissolved by buffered oxide etching solution to make a naked hydrophobic silicon surface. An Al_2O_3 film was deposited on top of the silicon substrate by atomic layer deposition (ALD) technique at 120°C using trimethylaluminum (TMA) and O_2 as the source [42]. **Figure 1(a)** shows the X-ray diffraction (XRD) of the Al_2O_3 thin film on Si substrate scanned by the Cu $K\alpha$ radiation. The strong peak at 69°C is attributed to the silicon substrate, and the sharp peak at ~33°C coincides with the reflection of the α-Al_2O_3 phase, which indicates that the Al_2O_3 film is a single crystalline. **Figure 1(b)** shows the cross-section of the sample characterized by scanning electron microscope (SEM). As shown in **Figure 1(b)**, the deposited Al_2O_3 layer is dense and smooth with a thickness of ~60 nm. Both XRD spectrum and SEM image confirm that Al_2O_3 films were well prepared by the ALD system.

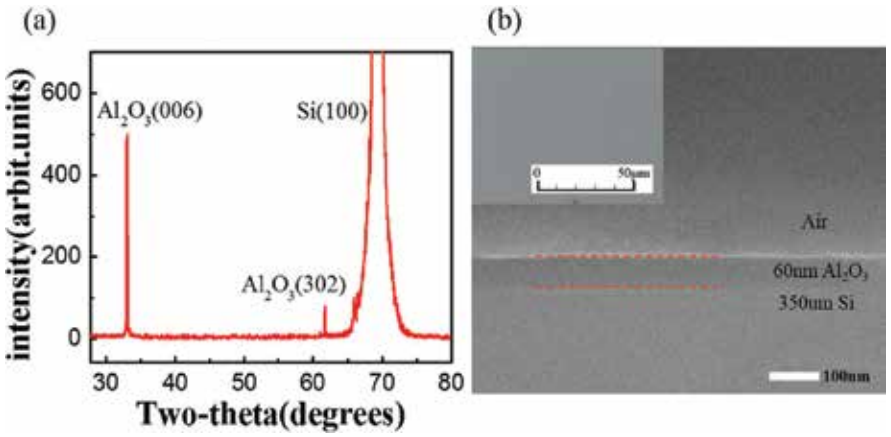

Figure 1. (a) θ–2θ scan of Al_2O_3-based GFET by X-ray diffraction with Cu$K\alpha$ radiation and (b) SEM image of the cross-section of a single crystalline ~60 nm Al_2O_3 film on the Si substrate. The inset shows the surface of graphene/Al_2O_3 obtained by optical microscope. The dash lines are a guide to the eye.

Large-area monolayers of graphene films were synthesized by chemical vapor deposition (CVD) on a copper foil, which were then transferred onto the ~60-nm Al_2O_3/p-Si substrate and 300-nm SiO_2/p-Si substrate, respectively [43, 44]. The SiO_2/p-Si substrate was used to fabricate the reference sample. The transferred graphene monolayers on the Al_2O_3/p-Si and SiO_2/p-Si substrate were characterized by a Raman spectroscopy with a 514 nm laser in **Figure 2(a)**. The two obvious peaks in the Raman spectra of graphene on the Al_2O_3/p-Si substrate are the G peak at ~1591 cm^{-1} and two-dimensional peak at ~2687 cm^{-1}. The peak intensity ratio I_G/I_{2D} is ~0.43, and the full-width at half-maximum (FWHM) of the two-dimensional peak is about 38 cm^{-1}. In addition, the intensity of the D peak at 1341 cm^{-1} is low with an I_D/I_G ratio of ~0.18, indicating that the transferred graphene is a high-quality monolayer which is similar to the sample grown on the SiO_2/p-Si substrate [45, 46]. The optical microscope shows the top view of the graphene/Al_2O_3 in the inset of **Figure 1(b)**, confirming that the device surface is smooth, uniform, and free of pinholes over large areas.

To acquire further understanding of the THz modulation characteristics, we now discuss the carrier properties of the graphene layer under electrical biasing. As graphene can be treated as a thin film, the frequency-dependent amplitude transmission $|T(\omega)|$ is given by $|T(\omega)| = \left|\frac{1}{1+NZ_0\sigma(\omega)/(1+n_s)}\right|$, where $N = 1$ is the number of graphene layer, Z_0 is the vacuum impedance, and n_s is the effective refractive index of the substrate. $\sigma(\omega)$ is the complex sheet conductivity of graphene, which can be described by the simple Drude model, namely $\sigma(\omega) = \frac{iD}{\pi(\omega+i\Gamma)}$, where Γ is the carrier-scattering rate and D is the Drude weight. D can be further expressed as $D = (V_F e^2/\hbar)(\pi|n|)^{1/2}$, where V_F is the Fermi velocity, e is the electron charge, $\hbar$ is the reduced Planck constant, and n is the carrier concentration of graphene. The corresponding variation of the E_F in graphene extracted from $|E_F| = \hbar V_F(\pi|n|)^{1/2}$ clearly shows the relation between E_F and the carrier concentration n. **Figure 2(b)** shows the conical band structures of graphene, whose Fermi level and carrier concentration can be changed by applying different gate biases in a GFET. As a result, the transmittance of the THz wave could be modulated by varying the applied bias voltages at the gate. Ambient atmosphere and processing residual on the surface of graphene often deviates the Dirac point of graphene from the zero voltage point [47]. To tune the transmittance of

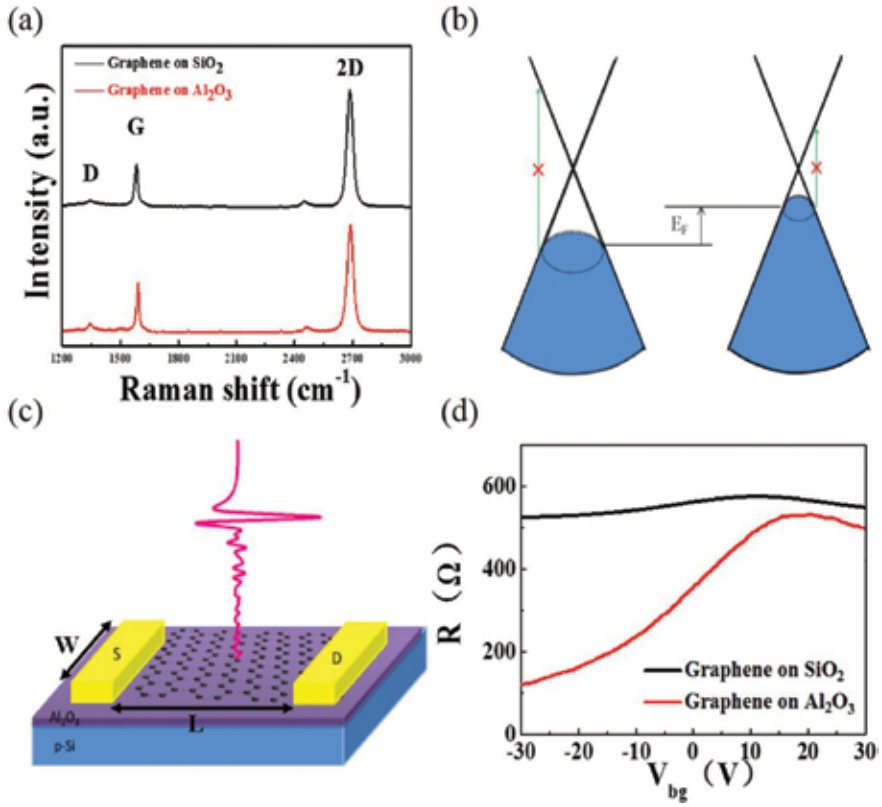

Figure 2. (a) Raman spectra of the monolayer graphene on the 300 nm SiO_2/p-Si and 60 nm Al_2O_3/p-Si substrate. (b) conical band structure of graphene and the sweeping of the Fermi level. (c) the scheme of GFET and THz transmission(W = 5 mm, L = 5 mm). (d) Total resistance R_{total} as a function of back gate voltage V_{bg} in the GFET.

THz wave through the graphene, a bias at gate was applied to deviate E_F further from the charge neutrality point (CNP) where carrier density of state and thus $\sigma_{DC}(E_F)$ and $\sigma(\omega)$ are minimized due to the conical band structure.

In addition, to evaluate the CNP of monolayer graphene, a graphene-based FET based on Al_2O_3/*p*-Si was fabricated with silver paste as the source and drain electrodes, respectively. Meanwhile, *p*-Si was used as the back gate to vary the carrier concentration n and Fermi level E_F of graphene as shown in **Figure 2(c)**. Based on the transfer characteristic measurement, the resistance between source and drain (R_{total})-dependent back gate voltage (V_{bg}) is shown in **Figure 2(d)**. The maximum resistance of the graphene FET occurs at 18 V, where Fermi level is located at the CNP for this device. The Fermi level of graphene would tend to remain with CNP with the back-gate voltage closing to the Dirac voltage. Carrier concentration got the minimum and the THz transmittance got the maximum at the CNP, respectively. The fabrication of SiO_2-based GFET is similar to that of the Al_2O_3-based devices. The CNP of SiO_2-based GFET is ~15 V, which is very close to Al_2O_3-based devices.

The carrier mobility (μ) in GFET can be calculated by $\mu = g_m L/(WC_g V_{ds})$, where $g_m = dI_{ds}/dV_{bg}|_{Vds = constant}$ is obtained from the R_{total} -V_{bg} curve shown in **Figure 2(d)**; both of the length (L) and width (W) of graphene channel are 5 mm; the constant V_{ds} is 1 V; the back-gate capacitance

per unit area, C_g, is 11.9 n F/cm^2 for SiO_2 GFET, and 110.625 nF/cm^2 for Al_2O_3 GFET [48]. With these parameters the carrier mobility of graphene on Al_2O_3 and SiO_2 were calculated to be 682.4 and 546.2 cm^2 V^{-1} s^{-1}, respectively. It can be seen that the carrier mobility of GFET on Al_2O_3 is larger than that on SiO_2. More importantly, the g_m of GFET on Al_2O_3 (~75.5 μS) is calculated to be 11 times higher than that on SiO_2 (~ 6.5 μS) [41]. According to the equation, the huge difference in g_m indicates a large discrepancy in the back-gate capacitance (C_g) and consequently in the carrier density variation for Al_2O_3 and SiO_2-based GFET. Due to the larger g_m and higher carrier mobility, a larger modulation depth and higher speed can be anticipated in Al_2O_3-based GFET modulator, respectively.

3.2. Modulation properties of the enhanced THz modulator

To further compare the THz modulation properties of devices on SiO_2/ p-Si and Al_2O_3/p-Si substrate, we applied to the modulators with back voltages ranging from −20 to 10 V with an increment of 5 V. A blank p-Si substrate was used as a reference sample to eliminate the substrate effect. The THz transmission spectra, we would discussed later, were all normalized to a blank p-Si substrate and the absorption from the substrate was also removed. Therefore, what we analyzed in the following is almost the intrinsic properties of the graphene itself.

We measured the spectral transmission of the modulators by a typical optical-fiber integrated terahertz time-domain spectroscopy (TDS). **Figure 3(a)** shows the normalized THz transmission intensity through a GFET with graphene/~300 nm SiO_2/p-Si sandwich structures under each applied back voltage from −20 to 10 V and 0.4–1.5 THz. A weak modulation of the THz transmission indicates a small swing of graphene Fermi level under the back gate bias between 20 and −10 V. A specific frequency of 1 THz was chosen to discuss the modulation behaviors. The gate-dependent transmission curve exhibited a minimum transmission of 88% at −20 V and gradually reached a maximum of 90% at 10 V. The modulation depth was thus calculated by |(T (10 V)–T (−20 V))/T (10 V)| to be ~2% (1% per 15 V). A thicker SiO_2 back-gate dielectric layer would increase the cavity effect along the transmission direction leading to the weaker modulation [39].

Figure 3(b) shows the modulation curves measured for Al_2O_3-based GFET. A distinctive variation in THz wave transmission was observed at a different gate voltage from −20 to 10 V. At 1 THz, the transmission exhibited a minimum of 71% at −20 V and reached a maximum of 91.3% at 10 V. The total modulation depth was calculated to be 22%. The amplitude of THz transmission is approximately flat from 0.4 to 1.5 THz at each gate voltage, indicating that the Al_2O_3-based GFET is an efficient broadband THz modulator. **Figure 3(c)** shows the extracted modulation depth of Al_2O_3-based GFET from 0.4 to 1.5 THz at different applied gate voltages. It is clear that the maximum modulation depth of 22.5% occurs at 0.85 THz with V_{bg} = −20 V. The transmission of THz wave is primarily determined by carrier density, which in turn can be precisely tuned by V_{bg}. **Figure 3(d)** compares the transmitted amplitudes of THz wave at the frequency of 1 THz through the GFET with SiO_2 and Al_2O_3 gate dielectric at different V_{bg}. As shown in **Figure 3(d)**, the modulation of THz wave transmission can be greatly improved by replacing the SiO_2 with Al_2O_3 as dielectric materials in GFET.

The dynamic modulation characteristics of Al_2O_3-based modulator were further studied with a homemade setup, in which a Virginia Diodes (VDI) continuous-wave (CW) terahertz source with

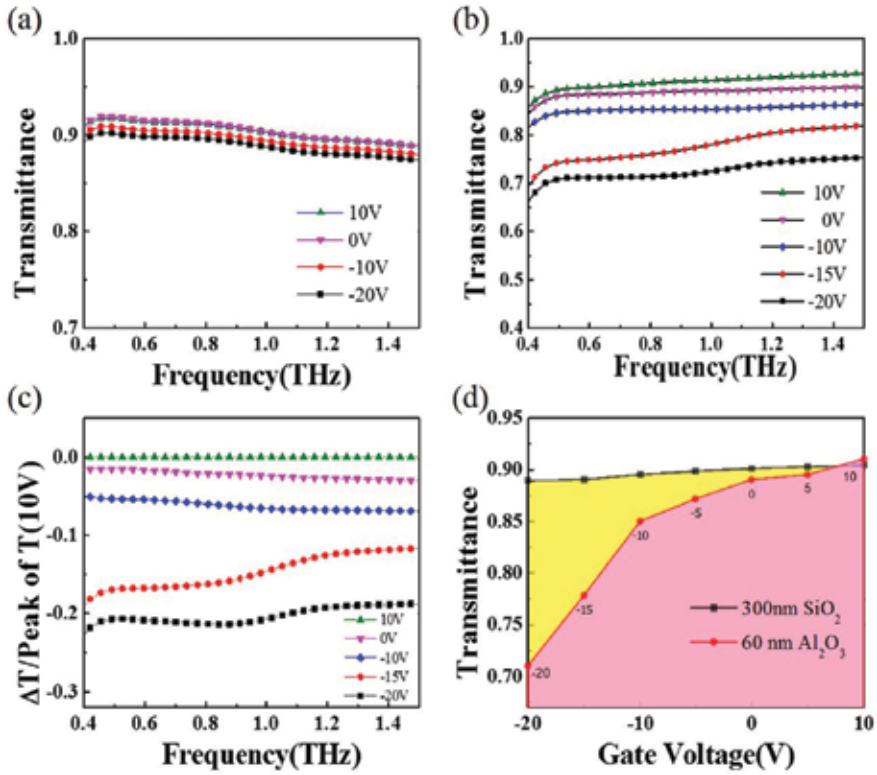

Figure 3. Normalized intensity of transmitted THz wave through the (a) SiO_2- and (b) Al_2O_3-based GFET at different back gate voltage. The modulation depth of Al_2O_3-based GFET as a function of applied gate voltage is shown in (c), and (d) the comparison of the amplitudes of the THz wave transmission through the GFET modulators with SiO_2 and Al_2O_3 dielectric at 1 THz.

a central output in the 340 and a 240–400 GHz zero-bias Schottky diode intensity detector are included. In the measurement, we applied a square biasing voltage to the device and the output modulated THz waveform was recorded by an oscilloscope. The applied voltage pulse is −10 V at the minimum and 10 V at the maximum with various modulation frequencies. **Figure 4(a)** shows the recorded waveform of Al_2O_3-based modulator at a carrier frequency of 340 GHz. **Figure 4(b)** shows the dependence of the normalized modulation magnitude on the modulation frequency, which gives rise to a 3-dB bandwidth (f_c) of 170 kHz. As we know, the RC time constant of a transistor is an important parameter to determine the switch speed. The device resistance (R) was estimated to be 261 Ω by extracting the average resistance as the back voltage sweeping from −10 to 10 V. The capacitance (C) can be expressed by $C = A\varepsilon\varepsilon_0/d$, where ε is the relative dielectric constant of the ALD-deposited Al_2O_3 film (~7.5), ε_0 is the permittivity of free space, A is the effective area of active graphene device of 5 × 5 mm^2, d is thickness of the Al_2O_3 film of 60 nm. The capacitance C is then calculated to be ~27.7 nF. As a result, the calculated RC time constant is ~138.7 kHz, which is very close to the directly measured 3-dB bandwidth (170 kHz). These results confirm that Al_2O_3-based GFET possesses a higher modulation speed than the conventional silicon-based graphene THz modulators [39].

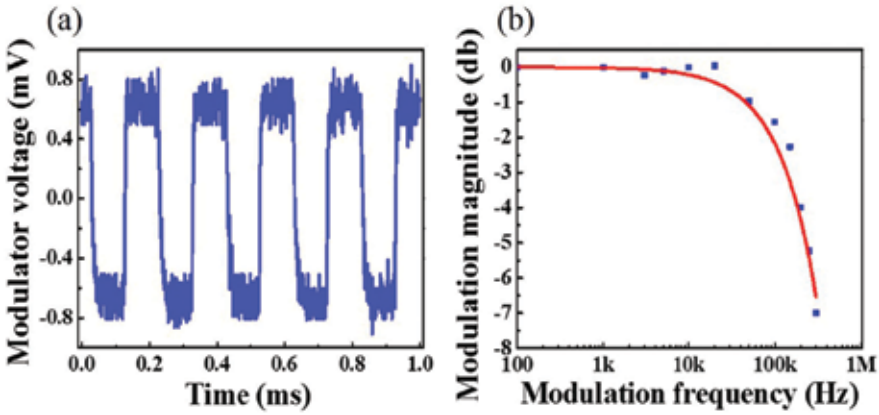

Figure 4. (a) Modulated THz waveform from the Al_2O_3-based modulator under a square voltage pulse at a modulation frequency of 5 kHz. (b) the dependence of the normalized modulation magnitude on the modulation frequency.

Obviously, the Al_2O_3 film is superior over SiO_2 as a gate dielectric in GFET modulator. By replacing 300 nm SiO_2 with 60 nm Al_2O_3, an enhancement of 11 times in modulation depth was observed. Furthermore, the modulation speed increased from 20 to 170 kHz as well. One reason for this significant improvement is that the high-κ dielectrics can remarkably reduce the Coulomb impurity scattering [41] to achieve a high g_m and consequently a larger THz modulation depth [49]. This work provides an effective method to fabricate high quality GFET THz wave modulator with large modulation depth and fast switch speed, which is vital for many THz technology applications as well as for fundamental research.

4. Flexible THz modulator based on graphene FET

In contrast to rigid THz modulators, flexible THz modulators are expected to be used in application fields with complicate surfaces [50]. A typical type of flexible modulator is a field-grating device, with which the intensity or phase of THz wave can be modulated by electrical gating or laser, but its properties remain unchanged under device deformation. This device is highly desired in nonplanar applications. Graphene is a highly flexibility material where its electronic structure can be maintained under deformation. Therefore, it is promising to develop flexible THz modulators based on graphene FET. Here, we give a typical example.

4.1. Device fabrication of the flexible THz modulator

The schematic diagram and photograph of the flexible THz modulator are presented in **Figure 5(a)** and **(b)**, respectively. The whole device is fabricated on a flexible commercial PET substrate. First, monolayer graphene was synthesized by typical chemical vapor deposition (CVD) on the copper foil and then was transferred onto the PET substrate [44–46]. The silver pastes were brushed at the two sides of graphene strip as the source and drain electrodes. The effective length and width of the channel of graphene FET was defined to be 2 and

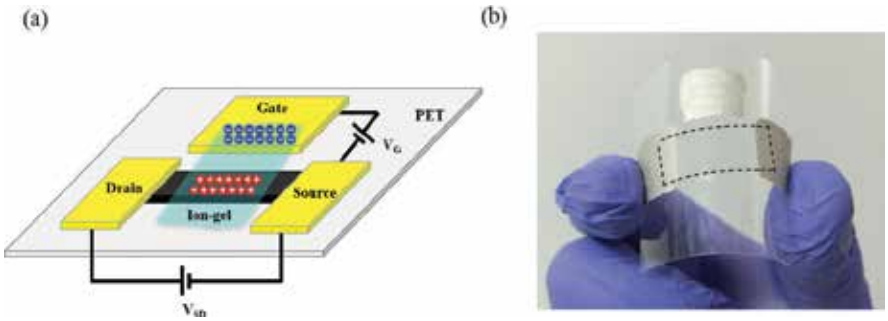

Figure 5. (a) Schematic structure of the flexible THz modulator based on graphene coplanar-gate FET. (b) Photograph of the flexible THz modulator in the bending condition, where the boundary of graphene channel is marked with dotted lines.

1 cm, respectively. The ion-gel, which is a mixture of lithium perchlorate, polyethylene oxide (PEO), and carbinol, was spin coated on the surface of the graphene as the gate dielectric. The work principle of this coplanar-gate FET structure is: when a positive voltage to the device is applied, as shown in **Figure 5(a)**, negative and positive ions in the ion-gel accumulate onto the gate electrode and graphene channel, respectively. A strong electric field is thus imposed to the graphene to modulate the carrier concentration and as a result a modulation to the THz radiation is realized.

4.2. Modulation properties of the flexible THz modulator

The intensity modulation performance of flexible THz modulator has been investigated by using a homemade fiber-coupled THz-time domain spectroscopy (TDS). A pair of photoconductive antenna made on LT-InGaAs/InAlAs is used as both the emitter and detector, which prove a bandwidth of 2 THz approximately. The THz wave from the emitter is focused onto the center of the sample with a beam diameter of 3 mm, covering the active area of the modulator. In order to study the flexible performance of our THz modulator, the device has been measured in the flat, convex, and concave conditions, respectively. The bending strain is ~1%, which is defined as strain ≈ $(t_s–t_p)/2r_c$ (t_s, $t_p >> t_f$) [51]. t_s is the thickness of the flexible PET substrate (~125 μm), t_p the thickness of the ion-gel (~10 μm), t_f the thickness of the graphene film (~0.34 nm), and r_c the curvature radius. In addition, it is noted that, in this work, all transmittances of THz wave through the flexible modulator have been normalized to the reference signal of air.

The modulation performance of flexible THz modulator was studied in detail. The normalized intensities of THz wave through the modulator are plotted in **Figure 6(a)–(c)** in the flat, convex, and concave conditions, respectively. As shown in **Figure 6(a)**, significant modulation changes in THz transmission can be obtained by applying gate bias between −3 and +3 V when the modulator is in the flat condition. From **Figure 6(a)**, it can be observed that the transmittance has a maximum value of 81.3% at 1 V and a minimum value of 63.1% at −3 V. Therefore, the MD of the modulator is calculated to be 22.4%. Importantly, when the graphene modulator is in the convex and concave conditions, the modulation depths estimated from **Figures 6(b)** and **(c)** are 21.3 and 21.4%, respectively, which are very close to that

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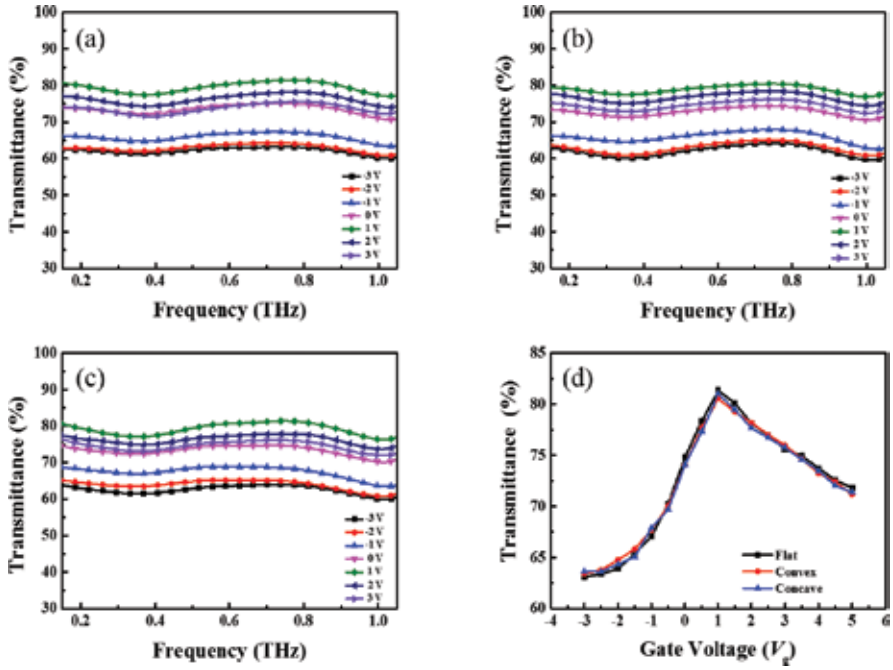

Figure 6. Normalized THz transmittance from the flexible graphene modulator as a function of frequency in the (a) flat, (b) convex, and (c) concave conditions at the fixed gate voltages ranging from −3 to 3 V, with 1 V increment. (d) Normalized THz transmittances as a function of gate voltage from −3 to 5 V at 0.8 THz in the flat, convex, and concave conditions.

in the fat condition. The performances of modulation under flat case, convex, and concave conditions are compared, as shown in **Figure 6(d)**. It can be observed that the three curves of transmittance-dependent gate bias at 0.8 THz are almost coincident. It indicates that the flexible modulator has excellent flexible performance, as the THz intensity modulation performances are steady under different bending deformations.

Further demonstrating the flexible performance of our THz graphene modulator, the repeatability has been studied by performing 1000 bending times. It shows that the THz intensity can still be effectively modulated by electrical gating. The modulation depths are 21.7, 21.1, and 20.5% at 0.8 THz in the flat, convex, and concave conditions, respectively, which are very close to that of the graphene modulator before bending. The curves of transmittances as a function of gate voltage at 0.8 THz before and after bending the graphene modulator 1000 times are nearly coincident, showing its high repeatability. We can conclude that the THz intensity modulation can be maintained not only in the bending condition but also after the long bending times, indicating superior flexible performance of the THz graphene modulator.

More importantly, a low insertion loss of THz wave was observed in our flexible THz modulator. By using air as the reference, the transmittance of the flexible modulator at 1 V gate voltage was measured and normalized, as plotted in **Figure 7**. It shows a broadband transmittance with the insertion loss less than 1.2 dB in the range of 0–1 THz, which is much smaller

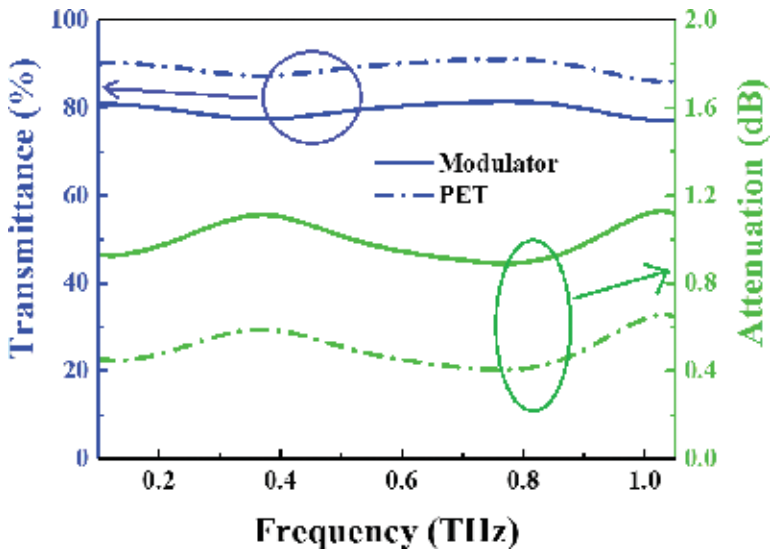

Figure 7. Transmittance and attenuation as a function of frequency for flexible graphene modulator at the gate voltage of 1 V (Dirac point) and PET.

than that of the Si substrate-based rigid graphene modulators (~5 dB) [52]. The extremely low loss can be attributed to the small refractive index of PET (1.65) as compared to that of Si (3.42). Our results indicate that employing a substrate with low refractive index is beneficial for obtaining a THz modulator with low insertion loss.

Modulation depth is one of the crucial parameters that determine the real applications of THz modulators. The typical MD of existing GFET modulators is only 20%. High MD has been achieved by a complex and exquisite integration of GFET with THz quantum cascade lasers

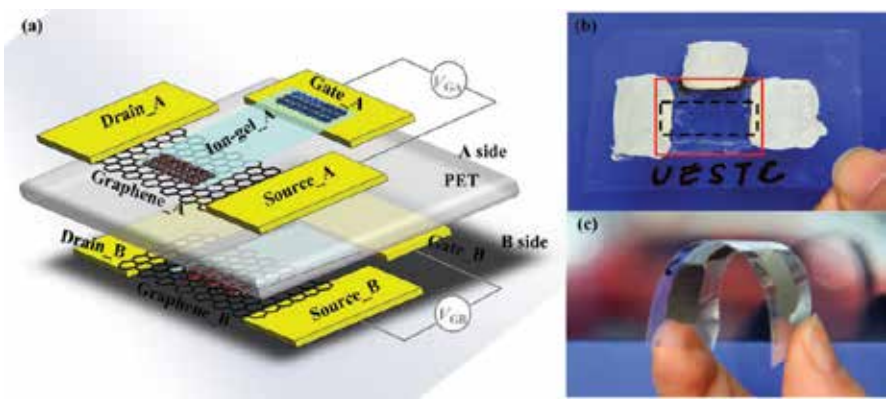

Figure 8. Overview of the cascaded THz modulators. (a) Schematic illustration of the device with cascaded two GFETs on a single PET substrate. (b) Photograph of the devices. The boundaries of graphene channel and ion-gel layer are marked with dark dotted lines and red solid lines, respectively. (c) Optical image showing the flexible nature of the device.

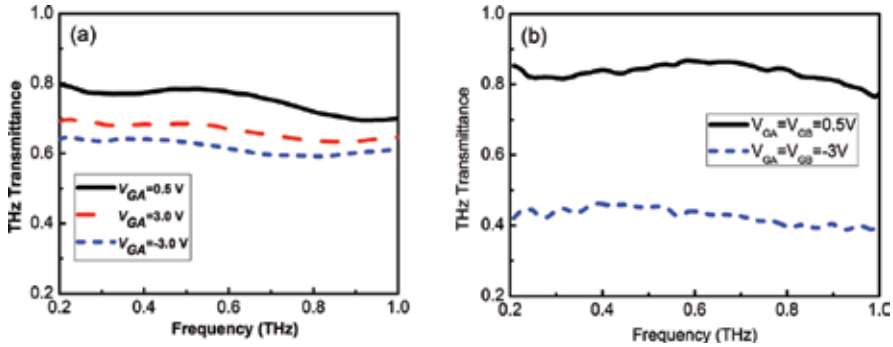

Figure 9. Normalized THz transmittance spectra of cascaded modulators under different gating schemes. Gate voltage applied to (a) single modulator and (b) dual modulators.

(QCL), despite the intrinsic MD of GFET is only 11% [53]. Inspired by the flexible and low-loss PET-GFET we developed previously, here, we propose an effective method to enhance the modulation depth by cascading multiple PET-GFET modulators with little sacrifice of insertion loss. Two GFETs were simultaneously fabricated on both sides of PET substrate to form a cascaded THz modulator, as shown in **Figure 8(a)**. The obtained devices are optically transparent and highly flexible, as shown in **Figure 8(b)** and **(c)**.

Modulation depth and insertion loss, two critical parameters of THz modulators are investigated. To investigate the modulation of the cascaded device, the THz transmittance was measured with an optimized gating scheme. **Figure 9** shows the transmission intensity of the THz waves through the graphene modulators at the frequency from 0.2 to 1.0 THz, which is normalized to the spectrum of air. Broadband modulation is obtained across the whole spectrum. When gate voltage is only applied to one modulator (**Figure 9(a)**), the transmittance at 0.6 THz reaches the maximum of 77.56% at 0.5 V and minimum of 61.41% at −3.0 V, respectively, leading to an MD of 20.8%. Maximum modulation depth was obtained when gate electrodes of both modulators were simultaneously driven. An enhanced MD of ~51% is achieved with an IL of only 1.4 dB. To our best knowledge, this is the largest MD reported for flexible and broadband THz modulators and can be further improved by stacking more similar structures.

5. Conclusion

Field-effect transistors are one of the most widely discussed applications of graphene in microelectronics and opto-electronics. However, graphene is intrinsically a zero-band-gap semiconductor, which is believed to be unsuitable for use in an electronic transistor. Fortunately, graphene FET finds its potential usage as THz modulators since THz wave is highly sensitive to the free carrier concentration, which can be effectively tuned by electrical gating in a graphene FET. In this chapter, the physics principle, device structure, and the modulation characteristics of GFET-based THz modulators, both rigid and flexible, are discussed

and experimentally demonstrated. It shows that THz modulators can be easily realized with graphene FET, and highly desired properties can be obtained such as the large modulation depth, high speed, broad width band, and insert loss.

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Conflict of interest

The authors declare no conflict of interest.

Author details

Qi-Ye Wen[1]*, Yu-Lian He[1], Jing-Bo Liu[2], Qi Mao[2], Qing-Hui Yang[1], Zhi Chen[3] and Huai-Wu Zhang[1]

*Address all correspondence to: qywen@163.com

1 State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu, Sichuan, PR China

2 School of Electrical Engineer and Intelligentization, Dongguan University of Technology, Dongguan, Guangdong Province, PR China

3 National Key Laboratory of Science and Technology of Communication, University of Electronic Science and Technology of China, Chengdu, PR China

References

[1] Chan WL, Deibel J, Mittleman DM. Imaging with terahertz radiation. Reports on Progress in Physics. 2007;**70**:1325-1379

[2] Jepsen PU, Cooke DG, Koch M. Terahertz spectroscopy and imaging, modern techniques and applications. Laser & Photonics Reviews. 2011;**5**:124-166

[3] Kleine-Ostmann T, Nagatsuma T. A review on terahertz communications research. Journal of Infrared, Millimeter, and Terahertz Waves. 2011;**32**:143-171

[4] Ho L, Pepper M, Taday P. Terahertz spectroscopy: Signatures and fingerprints. Nature Photonics. 2008;**2**:541-543

[5] Chen HT, Padilla WJ, Zide JMO. Active terahertz metamaterial devices. Nature. 2006;**444**: 597-600

[6] Rahm M, Li JS, Padilla WJ. THz wave modulators: A brief review on different modulation techniques. Journal of Infrared, Millimeter, and Terahertz Waves. 2013;**34**:1-27

[7] Ostmann TK, Dawson P, Pierz K. Room temperature operation of an electrically driven terahertz modulator. Applied Physics Letters. 2004;**84**:3555-3557

[8] Shrekenhamer D, Rout S, Strikwerda A C. High speed terahertz modulation from metamaterials with embedded high electron mobility transistors. Optics Express. 2011; **19**:9968-9975

[9] Chan WL, Chen HT, Taylor AJ. A spatial light modulator for terahertz beams. Applied Physics Letters. 2009;**94**:213511

[10] Chen HT, Padilla WJ, Cich MJ. A metamaterial solid-state terahertz phase modulator. Nature Photonics. 2009;**3**:148-151

[11] Chen HT, Padilla WJ, Zide JMO. Ultrafast optical switching of terahertz metamaterials fabricated on ErAs/GaAs nanoisland superlattices. Optics Letters. 2007;**32**:1620-1622

[12] Chen HT, Yang H, Singh R. Tuning the resonance in high temperature superconducting terahertz metamaterials. Physical Review Letters. 2010;**105**:247402

[13] Jin BB, Zhang CH, Engelbrecht S. Low loss and magnetic field-tunable superconducting terahertz metamaterial. Optics Express. 2010;**18**:17504-17509

[14] Wen QY, Zhang HW, Yang QH. Terahertz metamaterials with VO_2 cut-wires for thermal tenability. Applied Physics Letters. 2010;**97**:021111

[15] Xiong Y, Wen QY, Chen Z. Tuning the phase transitions of VO_2 thin films on silicon substrates using ultrathin Al_2O_3 as buffer layers. Journal of Physics D: Applied Physics. 2014;**47**:455304

[16] Alius H, Dodel G. Amplitude-, phase-, and frequency modulation of far-infrared radiation by optical excitation of silicon. Infrared Physics. 1991;**32**:1-11

[17] Vogel T, Dodel G, Holzhauer E. High-speed switching of far-infrared radiation by photoionization in a semiconductor. Applied Optics. 1992;**31**:329-337

[18] Okada T, Tanaka K. Photo-designed terahertz devices. Scientific Reports. 2011;**1**:121

[19] Cheng LJ, Liu L. Optical modulation of continuous terahertz waves towards cost-effective reconfigurable quasi-optical terahertz components. Optics Express. 2013;**21**:28657-28667

[20] Xie ZW, Wang XK, Ye JS. Spatial terahertz modulator. Scientific Reports. 2013;**3**:3347

[21] Wen TL, Zhang DN, Wen QY. Enhanced optical modulation depth of terahertz waves by self-assembled monolayer of plasmonic gold nanoparticles. Advanced Optical Materials. 2016;**4**:1974-1980

[22] Weis P, Garcia-Pomar JL, Hoh M. Spectrally wide-band terahertz wave modulator based on optically tuned graphene. ACS Nano. 2012;**6**:9118-9124

[23] Wen QY, Tian W, Mao Q. Graphene based all-optical spatial terahertz modulator. Scientific Reports. 2014;**4**:7409

[24] Zhang B, He TT, Shen JL. Conjugated polymer-based broadband terahertz wave modulator. Optics Letters. 2014;**39**:6110-6113

[25] Shi ZW, Cao XX, Wen QY. Terahertz modulators based on silicon nanotip array. Advanced Optical Materials. 2018;**6**:1700620

[26] Kannegulla A, Shams MIB, Liu L. Photo-induced spatial modulation of THz waves opportunities and limitations. Optics Express. 2015;**23**:32098-32112

[27] Driscoll T, Kim HT, Chae BG. Memory metamaterials. Science. 2009;**325**:5947

[28] Driscoll T, Palit S, Qazilbash MM. Dynamic tuning of an infrared hybrid-metamaterial resonance using vanadium dioxide. Applied Physics Letters. 2008;**93**:024101

[29] Seo M, Kyoung J, Park H. Active terahertz nanoantennas based on VO_2 phase transition. Nano Letters. 2010;**10**(6):2064-2068

[30] Goldam MD, Driscoll T, Chapler B. Reconfigurable gradient index using VO_2 memory metamaterials. Applied Physics Letters. 2011;**99**:044103

[31] Shi QW, Huang WX, Zhang YX. Giant phase transition properties at terahertz range in VO2 films deposited by sol-gel method. ACS Applied Materials & Interfaces. 2011;**3**(9): 3523-3527

[32] Kyoung J, Seo M, Park H. Giant nonlinear response of terahertz nanoresonators on VO_2 thin film. Optics Express. 2010;**18**(16):16452-16459

[33] Castro Neto AH, Guinea F, Peres NMR. The electronic properties of graphene. Reviews Modern Physics. 2009;**81**:109-162

[34] Zhong MY, Xu DK, Yu XG. Interface coupling in graphene/fluorographene heterostructure for high-performance graphene/silicon solar cells. Nano Energy. 2016;**28**:12-18

[35] Akinwande D, Tao L, Yu Q. Large-area graphene electrodes: Using CVD to facilitate applications in commercial touchscreens, flexible nanoelectronics, and neural interfaces. IEEE Nanotechnology Magazine. 2015;**9**(3):6-14

[36] Han MY, Ozyilmaz B, Zhang Y. Energy band-gap engineering of graphene nanoribbons. Physical Review Letters. 2007;**98**:206805

[37] Chen Z, Lin YM, Rooks MJ. Graphene nano-ribbon electronics. Physica E: Low-dimensional Systems and Nanostructures. 2007;**40**:228

[38] Sensale-Rodriguez B, Yan R, Kelly MM. Broadband graphene terahertz modulators enabled by intraband transitions. Nature Communications. 2012;**3**:780

[39] Maeng I, Lim S, Chae SJ. Gate-controlled nonlinear conductivity of Dirac fermion in graphene field-effect transistors measured by terahertz time-domain spectroscopy. Nano Letters. 2012;**12**:551

[40] Liao L, Bai J, Qu Y. Single-layer graphene on Al_2O_3/Si substrate: Better contrast and higher performance of graphene transistors. Nanotechnology. 2010;**21**:15705

[41] Gronera MD, Elama JW, Fabreguette FH. Electrical characterization of thin Al_2O_3 films grown by atomic layer deposition on silicon and various metal substrates. Thin Solid Film. 2002;**413**:186

[42] Li X, Cai W, An J. Large-area synthesis of high-quality and uniform graphene films on copper foils. Science. 2009;**324**:1312

[43] Liu JB, Li PJ, Chen YF. Large-area synthesis of high-quality and uniform monolayer graphene without unexpected bilayer regions. Jounal of Alloys Compounds. 2014; **615**:415-418

[44] Malard LM, Pimenta MA, Dresselhaus G. Raman spectroscopy in graphene. Physics Reports. 2009;**473**:51

[45] Ferrari AC, Meyer JC, Scardaci V. Raman spectrum of graphene and graphene layers. Physical Review Letters. 2006;**97**:187401

[46] Liang X, Sperling BA, Calizo I. Toward clean and crackless transfer of graphene. ACS Nano. 2011;**5**:9144-9153

[47] Schwierz F. Graphene transistors. Nature Nanotechnology. 2010;**5**:487

[48] Konar A, Fang T, Jena D. Effect of high-K gate dielectrics on charge transport in graphene-based field effect transistors. Physical Review B. 2010;**82**:15452

[49] Tao H, Bingham CM, Strikwerda AC. Highly flexible wide angle of incidence terahertz metamaterial absorbers: Design, fabrication, and characterization. Physical Review B. 2008;**78**:241103

[50] Wang ZG, Chen YF, Li PJ. Flexible graphene-based electroluminescent devices. ACS Nano. 2011;**5**:7149-7154

[51] Mao Q, Wen QY, Tian W. High-speed and broadband terahertz wave modulators based on large-area graphene field-effect transistors. Optics Letters. 2014;**39**:5649-5652

[52] Liang G, Hu X, Yu X. Integrated terahertz graphene modulator with 100% modulation depth. ACS Photonics. 2015;**2**:1559-1566

[53] Liu JB, Li PJ, Chen YF. Flexible terahertz modulator based on coplanar-gate graphene field-effect transistor structure. Optics Letters. 2016;**41**:816-819.1

Chapter 8

Electrical Characterization of Thin-Film Transistors Based on Solution-Processed Metal Oxides

João P. Braga, Guilherme R. De Lima,
Giovani Gozzi and Lucas Fugikawa Santos

Additional information is available at the end of the chapter

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Abstract

This chapter provides a brief introduction to thin-film transistors (TFTs) based on transparent semiconducting metal oxides (SMOs) with a focus on solution-processed devices. The electrical properties of TFTs comprising different active layer compositions (zinc oxide, aluminum-doped zinc oxide and indium-zinc oxide) produced by spin-coating and spray-pyrolysis deposition are presented and compared. The electrical performance of TFTs is evaluated from parameters as the saturation mobility (μ_{sat}), the TFT threshold voltage (V_{th}) and the on/off current (I_{on}/I_{off}) ratio to demonstrate the dependence on the composition of the device-active layer and on ambient characterization conditions (exposure to UV radiation and to air).

Keywords: semiconducting metal oxides, electrical properties, thin-film transistors, spray-pyrolysis, spin-coating

1. Introduction

The development of electronic and optoelectronic devices attending the increasing demand of new features like high-resolution, fast response, transparency and flexibility has motivated the pursuit of circuits using new active materials and/or new processing technologies. In this sense, semiconducting metal oxides (SMOs) as zinc oxide (ZnO) [1–9] and related compounds like aluminum-doped zinc oxide (AZO) [10–13], indium zinc oxide (IZO) [14, 15] and indium gallium zinc oxide (IGZO) [16, 17] are promising materials for flexible, transparent and high-performance electronics.

SMOs are particularly interesting to be used as the active layer of thin-film transistors (TFTs), which constitute the basic electronic device for drive circuits of active-matrix displays (AMDs)

and more sophisticated logic circuits which can be used in memories, microcontrollers and processors. Recently, the manufacture of metal oxide thin films using organic precursor solutions or nanoparticle suspensions became widespread [1–10], permitting the use of low-cost and nonsophisticated deposition techniques as spin coating, ink-jet printing and spray pyrolysis [18–21]. These techniques produce very uniform and homogeneous nanoscaled films, with high control of thickness and of other physical properties. This chapter aims to describe briefly the manufacturing processes of TFTs using solution-processed metal oxides as the semiconducting active layer, focusing on the electrical characterization and the study of the electrical properties relevant to the evaluation of device performance.

2. Semiconducting metal oxide thin-film transistors

Semiconducting metal oxides are promising materials to replace semiconductors as amorphous silicon (a-Si) and polycrystalline silicon (poly-Si) in applications as drive circuits of active-matrix (AM) flat-panel displays commonly used in cell phones, notebooks and monitor screens. They present interesting features like high optical transmittance in the visible range, high electronic mobility, low fabrication cost and compatibility to large-area applications. In the past 15 years, substantial efforts have been made to achieve high-performance SMO TFTs which are suitable to transparent and flexible substrates, enabling the development of the next generation of thin-flat panel displays.

As the active layer of thin-film transistors, SMOs usually present field-effect mobilities higher than 10 $cm^2.V^{-1}.s^{-1}$ (with a reported values as high as 172 $cm^2V^{-1}s^{-1}$) when deposited by techniques like RF sputtering and pulsed-laser deposition [22–27], which is a great advantage if we consider that a-Si can hardly present field-effect mobilities higher than 1 $cm^2V^{-1}s^{-1}$. Compared to poly-Si, which presents carrier mobilities up to 100 $cm^2V^{-1}s^{-1}$, SMOs present higher-film uniformity and considerably lower-processing temperatures, allowing large-area applications and low-production costs.

2.1. Zinc oxide and related compounds

Zinc oxide and related compounds and alloys are the most studied semiconducting metal oxides used as active materials in electronic and optoelectronic devices. Applications in thin-film transistors, light-emitting diodes and UV photodetectors and photosensors are feasible due to their chemical stability and exceptional electronic and physical properties. ZnO is transparent in the whole visible spectrum, has a wide (direct) band gap (E_g ~ 3.37 eV), a high electron mobility and large exciton binding energy (~ 60 meV). It crystallizes in either cubic zinc blend or hexagonal wurtzite structure, with the latter being the most thermodynamically stable form at ambient conditions. At relatively high temperatures and pressures, the rocksalt (NaCl) crystalline structure can also be formed. **Figure 1** shows the representation of the ZnO unit cell with wurtzite structure. In this structure, each cation is surrounded by four anions at the corners of a tetrahedron and vice versa, with a typically sp^3 covalent bonding nature coordination.

Even though large single crystals of ZnO can be obtained using appropriate substrates via very controlled deposition techniques like pulsed laser deposition (PLD), chemical vapor deposition

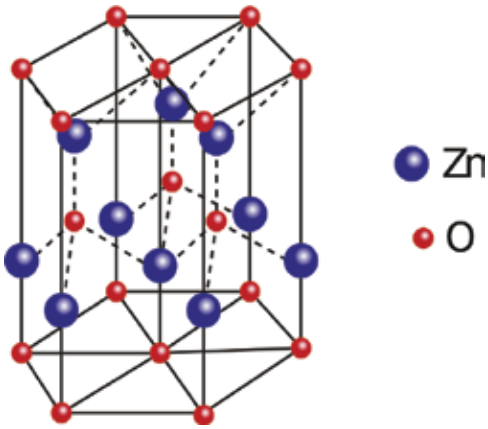

Figure 1. Representation of the ZnO unit cell with wurtzite structure.

(CVD) and molecular-beam epitaxy (MBE), most of the technological applications use thin films which are polycrystalline or formed by large-size crystallites separated by grain boundaries (as obtained by RF sputtering), presenting limitations to the charge-carrier transport.

Zinc oxide is known as an unintentionally doped semiconductor, due to the presence of native (intrinsic) defects in the crystal lattice. These defects can be vacancies (missing atoms at regular lattice positions), interstitials (extra atoms occupying interstices in the lattice) and antisites (an anion occupying a cation position in the lattice or vice versa) [28]. Although controversial, oxygen vacancies and zinc interstitials have been often credited as the major source of the observed unintentional n-type conductivity in ZnO [9, 24, 29–32]. The oxygen vacancies (V_o) have the lowest formation energy among the native defects which act as donors in ZnO and are frequently associated in the literature to the n-type character of ZnO. However, density functional calculations have shown that V_o's behave more as deep donor defects instead of shallow donors and some authors affirm that they cannot be responsible for the n-type carrier transport in ZnO [33, 34]. Zinc interstitials (Zn_i), on the other hand, behave as shallow donors but are usually present in very low concentrations in n-type ZnO. An alternative explanation is that n-type conductivity is due to unintentional substitutional hydrogen impurities, which is supported by theoretical calculations [35, 36]. Therefore, the actual origin of n-type conductivity in ZnO still remains controversial since a great number of experimental reports on the electrical properties of thin-film ZnO electronic devices demonstrate a correlation between oxygen concentration (during deposition and/or device handling) and the electrical conductivity [23, 37, 38], disagreeing with results obtained from first-principle theoretical calculations in crystals.

2.1.1. Thin-film deposition methods

Electronic and optoelectronic devices based on metal oxides usually comprise thin-films deposited on appropriate substrates. High-quality crystalline ZnO layers can be obtained by using extremely controlled deposition processes like pulsed laser deposition (PLD), molecular beam epitaxy (MBE), chemical vapor deposition (CVD), metal–organic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD) [12, 33, 39] and even using less sophisticated methods like RF magnetron sputtering [22–25].

However, with the recent increase on field-effect mobility of TFTs produced with the active layer deposited from solution processes [3, 5, 6, 17, 19, 20], more attention has been attracted to the possibility of using very simple and low-cost deposition methods to obtain high-performance TFTs. Solution-based deposition processes allow the use of techniques like dip coating, spin coating, spray coating, ink-jet printing, silk screen and numerous others which are compatible to large-area, flexible, affordable and scalable applications. **Figure 2** shows a schematic representation of the basic features of common low-cost deposition methods for fabrication of metal oxide TFTs. RF magnetron sputtering (**Figure 2a**) and PLD (**Figure 2b**) produce highly crystalline films with relatively good thickness and uniformity control; however, target materials, vacuum and partial gas pressure systems as well as RF source or laser beam are needed, making these techniques more sophisticated when compared to solution-based processes like spin coating (**Figure 2c**), airbrush spray pyrolysis (**Figure 2d**) or ultrasonic spray pyrolysis (**Figure 2e**).

Spin coating is a widespread used deposition technique which yields very thin (ranging from few nanometers up to micrometers) and uniform films by spreading a solution of the desired material onto cleaned substrates and making them spin at high rotation speeds (about 1000–8000 rpm) promoting solvent evaporation. The technique is very successful in the formation of organic or polymeric films but can be used to deposit inorganic materials solutions or suspensions as well. Spray pyrolysis is based on spraying a solution of an organic precursor onto a preheated substrate (usually at a temperature above the degradation temperature of the

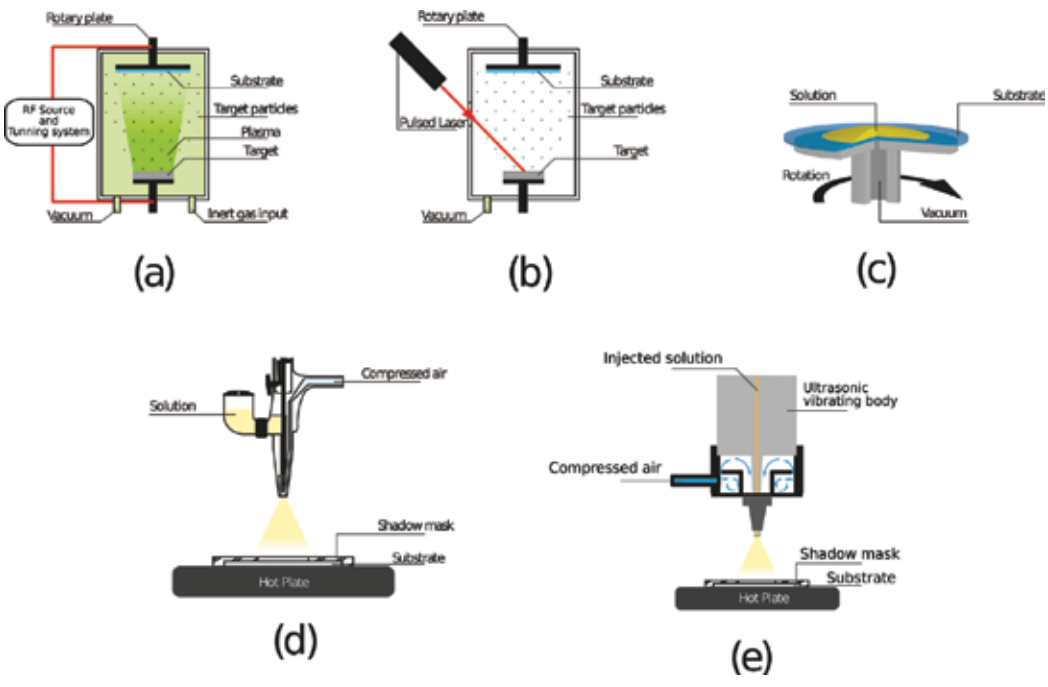

Figure 2. Summary of the frequently used low-cost deposition techniques used to produce electronic devices based on semiconducting metal oxides. (a) RF magnetron sputtering; (b) pulsed laser deposition (PLD); (c) spin-coating; (d) airbrush spray-pyrolysis (ASP); and (e) ultrasonic spray-pyrolysis (USP).

organic phase of the precursor material) to produce thin and highly uniform metal-oxide films. Difference between airbrush and ultrasonic spray deposition is that, in the former, a mechanically actuated needle is responsible to release the precursor solution, which flows due to gravity through the spray nozzle whereas in the latter, a piezoelectric nozzle driven by an ultrasonic power supply is used to nebulize the precursor solution which is injected by a micro-syringe pump. In both cases, compressed dry air or inert gas is used to carry the nebulized material. Ultrasonic spray has the advantage to provide higher droplet size control (in the order of tens of microns) and to economize precursor solution whereas airbrush is a low-cost and simple alternative to obtain very uniform films which can be used to produce high-performance TFTs [13].

2.2. Solution-processed metal oxide thin films

Solution-processed metal oxide thin films used as the active layer of transistors can be deposited from any of the techniques mentioned previously. An important key to obtain high performance and reproducible devices is the film uniformity, which can be macroscopically inspected by visual observation (translucent and shiny films usually represent superior quality films) or microscopically from techniques like profilometry (which can measure the surface roughness), atomic force microscopy (AFM) or scanning electron microscopy (SEM). The solution preparation method plays a significant role in the film formation and must be meticulously planned to obtain improved performance devices. The most commonly used solution processing techniques used to produce SMO TFTs are based on: (i) the calcination or pyrolysis of an organic precursor of the desired metal oxide which is soluble in an organic solvent or (ii) on the physical agglomeration or chemical reaction of previously synthesized nanoparticles which can form a uniform suspension in water or in other polar protic solvents.

2.2.1. Organic precursor pyrolysis

The solutions used to prepare SMO films deposited by spin-coating and spray technique are frequently obtained by the dissolution of organic salts containing the metallic atom which forms the metal oxide. **Figure 3** shows the scheme that most common organic salts used metal oxide precursors. Special attention is devoted to zinc acetate dihydrate (**Figure 3a**), which is the basic compound used to obtain ZnO and is soluble in water and other polar protic solvents like ethanol, isopropanol and methanol. Very often, 2-methoxyethanol is used as the solvent with ethanolamine as stabilizer [11, 15, 26] due to the credited better precursor dissolution and film formation.

Spin-coating deposition is commonly carried out using solution concentrations in the (0.03–0.3 M) range to originate organic precursor films which undergo a pyrolysis process by heating up the substrates in a hotplate or in an oven at temperatures above the degradation temperature of the organic compound (usually above 300°C). After the thermal decomposition of the precursor organic phase, oxide agglomerates intermediated by voids, but which can be interconnected along macroscopic distances (superior to few millimeters), are formed. To form a continuous and uniform oxide film, the multiple deposition of precursor layers by spin coating is performed, intercalated by the thermal treatment process to promote the oxide formation and to avoid the dissolution of the previous layers [14].

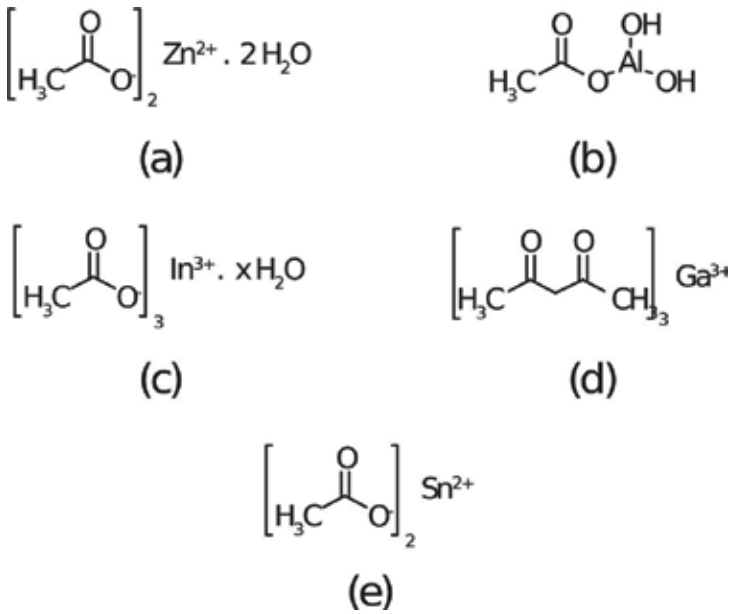

Figure 3. Scheme of the chemical structure of most commonly used organic precursors of metal oxides. (a) Zinc acetate dihydrate; (b) aluminum acetate dibasic; (c) indium acetate hydrate; (d) galium acetyl acetonate; (e) tin acetate.

Spray-pyrolysis deposition, on the other hand, is a much simpler method which does not require intermediate processing like the multilayer spin-coating method described earlier, being more suitable to industrial scalable processes. During spray deposition, precursor solution droplets reach a substrate heated up to a temperature much higher than the solvent boiling point, forming a solvent vapor layer that avoids the droplet to touch the hot substrate surface (Leidenfrost effect [40]), causing a randomly distributed deposition of micrometric/nanometric precursor particles on the surface. Since the substrate is also at a temperature above the organic precursor decomposition temperature, oxide formation initiates immediately during spray deposition, producing, if optimum deposition parameters are chosen [8], much more uniform and better quality films than the produced by spin coating.

From the considerations abovementioned concerning the organic precursor degradation temperature, it is of extreme importance to know in advance the physical chemical properties of the precursor salt. **Figure 4a** shows the Fourier-transform infrared spectra (FTIR) in attenuated reflectance mode (ATR) of zinc acetate dihydrate films treated at different temperatures, from 150 to 400°C. Peak (1) at 3377 cm^{-1} is from the asymmetric stretching mode of hydroxyl groups, whereas peaks (2) and (3) are from the stretching modes of the precursor ester groups (C=O and C—O, respectively). Peaks (4) and (5) are bending modes associated with the CH_3 groups and peaks (6) and (7) are due to bending modes of C=C bonds and COO^- groups, respectively. Peaks (8) and (9) correspond to Zn—OH and Zn—O stretching modes. One observes that the peaks associated to the organic phase of zinc acetate [10] gradually disappear by increasing the temperature, remaining only species associated with the inorganic phase (Zn—O) for temperatures above 400°C. Thermogravimetric analysis (**Figure 4b**) shows two main mass loss peaks, one around 100°C, due to loss of adsorbed water and water of crystallization and another around 290°C, due to the thermal degradation of the organic phase

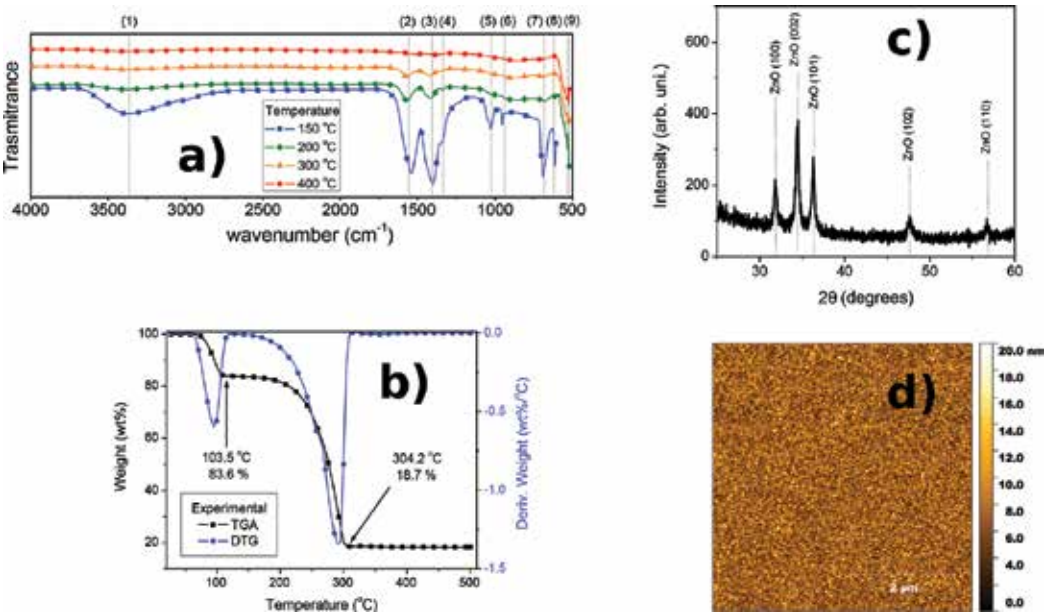

Figure 4. (a) Thermogravimetric analysis of zinc acetate; (b) FTIR spectra of zinc acetate at different temperatures; (c) DRX data from a spray-coated film at 350°C; and (d) AFM image of a spray-coated film.

of the precursor. Above 305°C, no significant mass loss is no longer observed up to 500°C, indicating that, probably, most of the remaining mass is due to the inorganic phase (ZnO).

The X-ray diffraction results shown in **Figure 4c** (obtained from a spray-coated sample deposited at 350°C) corroborate the expected results observed from FTIR and TGA/DTG analysis due to the typical pattern of the ordered hexagonal wurtzite phase (according to JCPDS Card No. 36-1451). Atomic force microscopy (AFM) of a spray-coated film at 350°C is shown in **Figure 4d** demonstrating the previously discussed uniform film morphology. Average surface roughness is less than 5 nm and observed rod-like structures have diameters inferior to 100 nm.

2.2.2. Metal oxide nanoparticles

Another interesting approach to obtain thin-film devices from solution is by the use of metal oxide nanoparticles which can be dispersed in water or organic solvents [5–7, 13]. The used nanoparticles are usually obtained by known inorganic synthesis methods and some options are commercially available. These nanoparticles can be used in the form of colloidal suspensions (which often need stabilizers to remain stable) to permit solution processing. The great advantage to use oxide nanoparticles is that the semiconducting phase is already present in the colloidal suspensions and deposition can be carried out at room temperature, without the need of further thermal treatment. This feature is important for the use of flexible substrates, which do not stand temperatures higher than 200°C. However, oxide nanoparticles suspensions usually give rise to lower quality films, with high roughness and large grain boundaries that are deleterious to the film electrical properties. Future improvements in the quality of films produced from oxide nanoparticles suspensions might improve device performance and make this alternative more interesting than processes involving the pyrolysis of organic precursor materials.

2.3. Thin-film transistors

Thin-film transistors are electronic devices in which all the active layers (semiconductor, electrodes and dielectric layer) are deposited as thin-films onto a supporting (non-active) substrate. The main role of the substrate in a TFT is to give mechanical support to the device structure and it does not interfere on the electrical characteristics of the transistor. The main use of this type of structure is as an electronic switch, having the current between two electrodes (drain and source) controlled (or modulated) by the voltage applied to a gate electrode which is separated from the drain and source electrodes by a highly insulating dielectric layer. Ideally, the current through the gate electrode (I_g) should be extremely small and could be neglected when compared to the current between the drain and source electrodes (I_{DS}), which can vary several orders of magnitude by varying the gate voltage (V_g). The drain-source current flows in the plane of the film direction, perpendicularly to the applied gate voltage, and is also dependent on the applied drain-source voltage (V_{DS}). Drain and source electrodes are usually formed by two long parallel metal stripes separated by a distance *L* known as *channel length*. The overlapping distance of the drain and source electrodes in the plane of the film is defined as the *channel width*, *w*.

From the point of view of the structure, TFTs can be constructed in diverse ways, with four basic distinct structures as depicted in **Figure 5**. The difference among these structures is the position of the electrodes relative to the active semiconducting layer. In a top-gate, bottom-contact (TGBC) configuration (**Figure 5a**) the gate electrode is the uppermost layer, on top of the dielectric layer, and the drain and source electrodes are the lowermost layers, being underneath the semiconducting layer. In this structure, drain and source electrodes can be deposited by lift-off photolithography or shadow mask thermal evaporation directly onto the substrate. Another characteristic of this structure is that the insulating layer must be deposited onto the semiconducting layer, a condition which cannot be achieved, depending on the deposition method of the dielectric material. Top-gate, top-contact (TGTC) configuration (**Figure 5b**) is similar to TGBC configuration with the difference that the drain and source electrodes are deposited onto the semiconducting layer. This configuration has also the same limitations concerning the dielectric layer deposition as the TGBC. Bottom-gate configurations (**Figure 5c** and **d**) are interesting from the point of view that they have three common stages (substrate, gate electrode and dielectric layer) and are very convenient when only the semiconducting active layer is changed (particularly for bottom-gate, bottom-contact, BGBC). However, bottom gate structures are not appropriate for use when the dielectric layer does not support temperatures higher than the deposition temperature of the semiconducting layer or does not resist to the solvent used to deposit the active layer.

Thin-film transistors have the electrical performance evaluated mainly by two characteristic current–voltage curves, namely, the *output* and the *transfer* curves. The output curve is defined by the drain-source current (I_{DS}) versus the drain-source voltage (V_{DS}) at different constant values of the gate voltage (V_g), whereas the transfer curve is obtained by measuring I_{DS} *versus* V_g at different constant values of V_{DS}. In a TFT configuration, the channel conductance (between drain and source electrodes) depends on the amount of free charge carriers present in the transistor channel, which can be controlled by the application of a bias voltage at the gate electrode.

If the semiconducting material is n-type, free electrons are accumulated next to the semiconductor/dielectric interface when a positive voltage is applied at the gate electrode (respective to the

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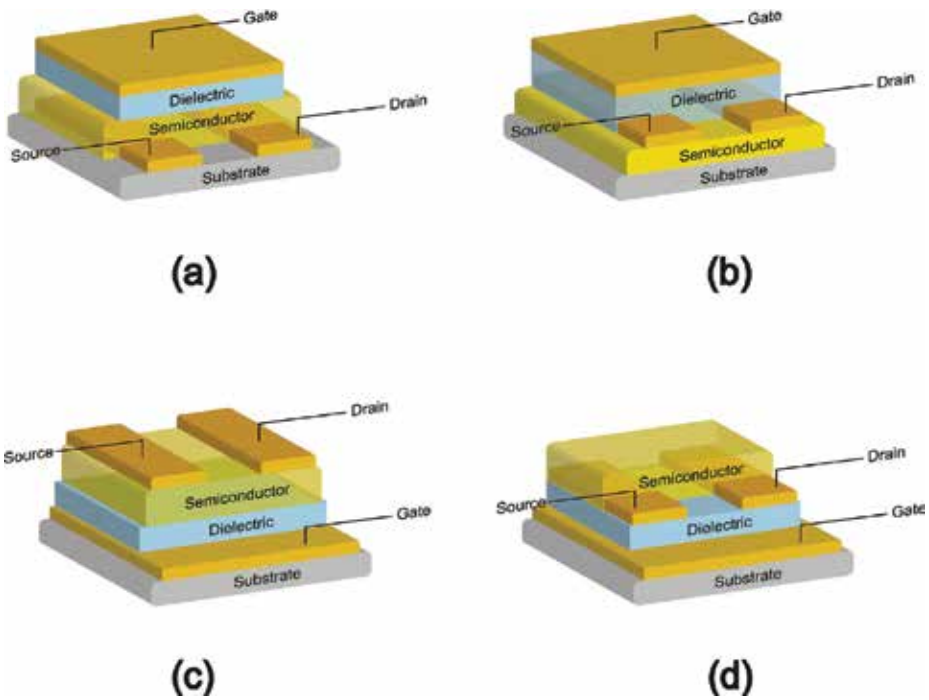

Figure 5. Most common electrode configuration for thin-film transistors: (a) top-gate, bottom-contact; (b) top-gate, top-contact; (c) bottom-gate, top-contact and (d) bottom-gate, bottom-contact.

source electrode), increasing the channel conductance (accumulation regime). The higher the positive gate bias, the more conductive becomes the transistor channel. However, for a negative gate bias, free electrons are repelled from the semiconductor/dielectric interface, decreasing the density of free charge carriers in the transistor channel (depletion regime) and, consequently, reducing the channel conductance. As a consequence, the channel current for a negative V_g is almost negligible when compared to the current for a positive V_g. For a p-type semiconductor, the majority free charge carriers are holes and the transistor is in the accumulation regime (conductive channel) when a negative bias is applied to the gate electrode and in depletion regime (resistive channel) when a positive bias is applied to the gate electrode.

The dependence of I_{DS} on V_{DS}, for low values of V_{DS}, is approximately linear, since, for a fixed value of V_g much higher than V_{DS} and in the absence of fixed charged defects at the semiconductor/dielectric interface, the channel majority free charge carrier distribution is nearly uniform. As the value of V_{DS} increases, the I_{DS} starts to deviate from the linear behavior (toward a sublinear behavior) since the charge near the drain electrode is reduced by the semiconductor potential. At a certain drain-source voltage, the accumulated charge next to the drain electrode is reduced near to zero, forming what is called the *pinch-off* point, which moves toward the source electrode as V_{DS} continues to increase. However, the voltage at the pinch-off point remains nearly constant. Therefore, the amount of charge that arrives at the pinch-off point remains the same (as well as the channel current) when a voltage beyond the formation of the pinch-off point (V_{sat}) is applied, despite the reduction on the effective channel length.

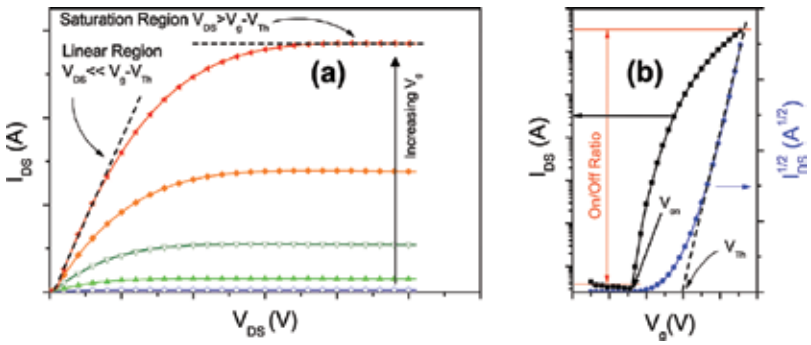

Figure 6. Characteristic curves of TFTs (a) output curves with characteristic linear and saturation regions; (b) transfer curve and $I^{1/2}$ versus vg (linear scale) extrapolation of Vth and slope for saturation mobility determination;.

This means that, for V_{DS} higher than V_{sat}, the channel current achieves a saturation regime, as observed in the output curves of **Figure 6a**.

The drain-source current in the linear regime can be approximated by [41, 42]:

$$I_{DS,\ lin} = \frac{w\mu C_{ox}}{L}\left(V_g - V_{th} - \frac{V_{DS}}{2}\right)V_{DS} \quad for\ V_{DS} \ll \left(V_g - V_{th}\right) \tag{1}$$

where μ is the charge carrier mobility, C_{ox} is the capacitance per unit area of gate dielectric layer ($C_{ox} = C/A = k\varepsilon_0/d$, with ε_0 the vacuum electric permittivity, k, the dielectric constant of the insulating layer and d, its thickness) and V_{th} is the *threshold voltage*, a voltage associated to the presence of charged traps at the semiconductor/dielectric interface and the difference of the work function between the semiconductor and the dielectric material, which is necessary to achieve the flat-band condition in the transistor channel. The channel current in the saturation regime, on the other hand, can be given by [41, 42]:

$$I_{DS,\ sat} = \frac{w\mu C_{ox}}{L}\left(V_g - V_{th}\right)^2 \quad for\ V_{DS} \gg \left(V_g - V_{th}\right) \tag{2}$$

Eq. (2) means that the square root of the channel current depends linearly on the gate voltage. Consequently, a plot of $(I_{DS})^{1/2}$ versus V_g (curve in blue in **Figure 6b**) may give a straight line which intercepts the abscissa at V_{th} and which slope gives the transistor *transconductance*, g_m:

$$g_m = \left[\frac{\partial\sqrt{I_D}}{\partial V_g}\right]_{V_{DS}=cte} \tag{3}$$

Combining with Eq. (2), the carrier mobility in the saturation regime can be calculated:

$$\mu_{sat} = \frac{2L\left(\frac{\partial\sqrt{I_D}}{\partial V_g}\right)^2}{w\,C_{ox}} \tag{4}$$

Even though the carrier mobility in a TFT can be obtained in different conditions, the saturation regime is very important on the transistor operation, the reason why most of the papers use the saturation mobility as one of the relevant parameters (along with V_{th}) used to evaluate the transistor performance.

Considering that TFTs can be used as electronic switches, other electrical parameters concerning the switching capacity are also used to evaluate the transistor performance: (1) the *on/off ratio* (I_{on}/I_{off}); (2) the onset voltage (V_{on}) and (3) the subthreshold swing (SS). The on/off ratio, which extraction method is shown in the transfer curve of **Figure 6b**, represents the ratio between the channel currents when the transistor is in the conduction mode (*Ion*) and when it is switched off (I_{off}). Since the ideal I_{off} value is minimal (to avoid power consumption when not operating), I_{on}/I_{off} should be the highest as possible. Typical good values for on/off ratio are above 10^5–10^6. The onset voltage is defined as the gate voltage necessary for the transistor switch from the "off state" to the "on state" and can be directly determined from the transfer curve as shown in **Figure 6b**. The subthreshold voltage (which is measured in volts/decade) is defined by:

$$SS = \left[\frac{\partial V_g}{\partial \log(I_{DS})}\right]_{min} \tag{5}$$

and can also be determined from the transfer curve data. It gives the information on how much gate voltage in needed to make the drain-source current increase by a factor of 10. Thus, the lowest this value, the better is the transistor performance.

2.3.1. Solution-processed ZnO TFTs

In the present section, we compare the results from the electrical characterization of ZnO TFTs with the active deposited by spray-pyrolysis and by spin-coating, annealed at different temperatures (300 and 500°C) after deposition. **Figure 7a–d** shows the output curves of the produced devices. Substrates are p-type (Boron) doped Si wafers with a thermally grown SiO_2 insulating layer (100 nm thick) used in a bottom-gate structure. Aluminum top drain and source electrodes were deposited on top of the ZnO layer, with a channel width of 5 mm and a channel length of 100 μm (*w*/*L* ratio of 50).

The output curves show that spray-coated devices present better transistor characteristics compared to spin-coated transistors. Operating currents of spray-coated devices are considerably higher (more than 7 times for devices annealed at 300 oC and more than 13 times for devices annealed at 500 oC) than the operating currents observed for devices produced by spin-coating. Moreover, spin-coated devices have much higher off currents (for $V_g = 0$ V), probably due to higher lateral leakage current (spin-coated films cover the whole substrate area whereas spray-coated films can be deposited selectively in a smaller active area) and/or higher leakage current through the gate dielectric (due to Leidenfrost effect, spray-pyrolysis deposition promote less cracks in the insulating SiO_2 bottom layer than spin-coating).

The transfer curves (**Figure 7e** and **f**) also show strong dependence on deposition method and annealing temperature. Spray-coated devices, as expected from the output curves, present much higher on/off ratios (about 10^6 against 10^3) and also saturation mobility values almost 10 times higher than spin-coated TFTs. Subthreshold swing (SS) values of spray-coated TFTs are smaller and do not present significant variation on annealing temperature as observed for spin-coating. Improved device characteristics of spray-coated devices can be explained by better film quality and crystallinity, which promotes less charge trapping and scattering. The temperature influence on the transfer curves for devices produced by the same deposition method indicates that at higher temperatures the semiconductor intrinsic conductivity increases due to more efficient elimination of organic residues and better film crystallinity.

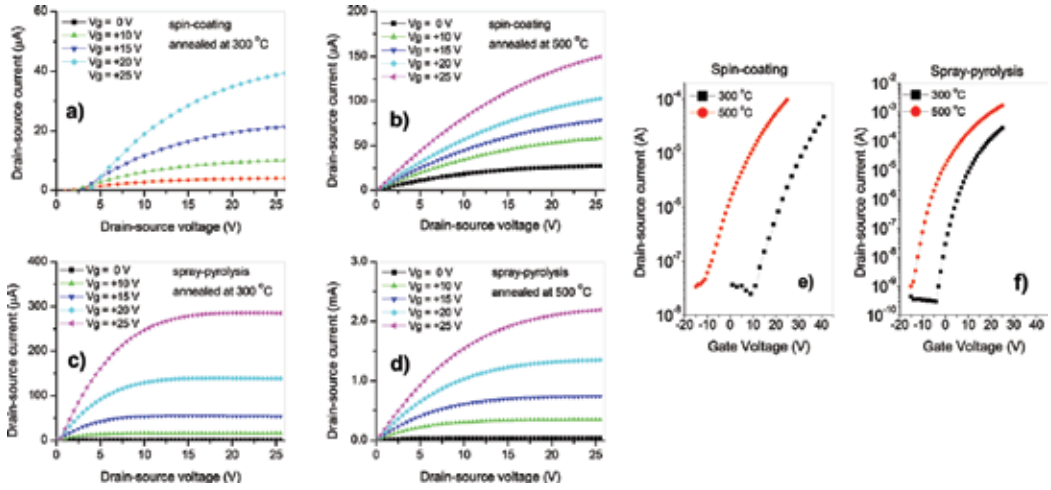

Figure 7. Output curves for solution-processed ZnO TFTs prepared by spin-coating and spray-pyrolysis and annealed at temperatures. Transfer curves for a spin-coated and spray-coated TFTs annealed at different temperatures.

Deposition method/ Annealing temperature	μ_{sat} ($cm^2.V^{-1}.s^{-1}$)	V_{th} (V)	V_{on} (V)	I_{on}/I_{off}	SS (V/dec)
Spin-coating/ 300 °C	0.14	+10.0	+10.1	1.3×10^3	2.91
Spin-coating/ 500 °C	0.36	+4.5	-12.3	3.0×10^3	6.37
Spray-coating/ 300 °C	1.29	+10.0	+3.3	1.3×10^6	2.00
Spray-coating/ 500 °C	5.55	+4.5	-14.5	2.1×10^6	2.13

Table 1. Electrical parameters obtained from the TFT data presented on **Figure 7**.

Higher intrinsic conductivity decreases both the threshold and the onset voltages, since more negative voltages are needed to deplete the transistor channel from intrinsic n-type charge carriers. **Figure 7e** also shows that higher annealing temperatures promote the reduction of electron traps at the semiconductor/dielectric interface, which are responsible to displace V_{th} and V_{on} to positive values. **Table 1** summarizes the electrical parameters obtained from the curves presented on **Figure 7**.

2.3.2. TFTs based on ZnO-related compounds

The electrical properties of solution processed ZnO films can change dramatically by incorporating other metallic elements in the precursor solution, obtaining doped ZnO or ternary or quaternary metal oxide alloys. When a small amount of a precursor as aluminum acetate dibasic (**Figure 3b**) is added to a zinc acetate solution, aluminum-doped zinc oxide (AZO) films can be obtained after precursor pyrolysis. Aluminum atoms can substitute zinc atoms in the crystalline lattice, originating a donor level close to the conduction band, increasing the material conductivity by doping.

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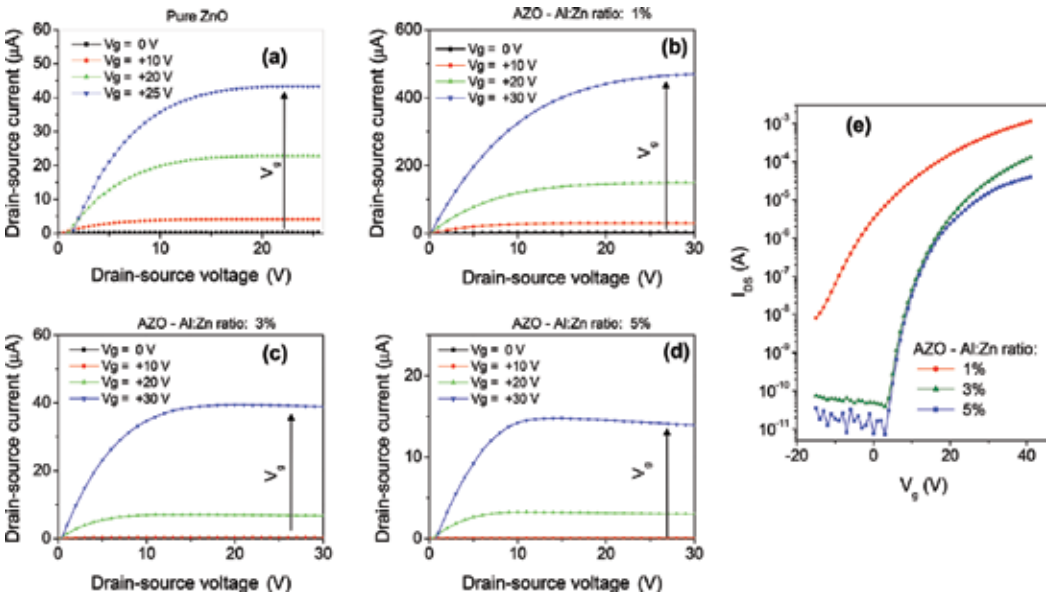

Figure 8. Output (a–d) and transfer (e) curves from spin-coated AZO TFTs produced using different active layer compositions.

Figure 8 depicts the characteristic TFT curves of spin-coated AZO devices produced using Al:Zn ratios which varied from 0% (pure ZnO) to 5%. One observes that a small addition of Al (1%) is responsible for a substantial increase (more than 10 times) on the operating current when compared to a pure ZnO TFT, corroborating the expectation of semiconductor doping. By increasing the Al concentration, however, the device current gradually decreases (for 5%, the currents are smaller than for pure ZnO). At Al concentrations equal and higher than 10%, the currents became so small that transistor characteristics could not even be observed. Such behavior can be explained that, for higher Al concentrations, the formation of insulating aluminum-related compounds (like aluminum oxide) becomes more efficient than the semiconductor doping, and the phase separation between semiconducting and insulating regions leads to poorer morphological properties of the film, reducing the overall conductivity.

The transfer curves of **Figure 8e** show that the TFT with 1% AZO active layer has a higher on current (and, consequently, higher mobility in saturation) and a higher intrinsic conductivity as well, which affects negatively the threshold voltage and the on/off ratio. At this point, it is important to notice that to obtain good TFT performance, it is not important to only increase the material conductivity, but also improve the film quality and control the number of defects at the semiconductor/dielectric interface.

The addition of a precursor like indium acetate hydrate (**Figure 3c**) to a zinc precursor solution does not cause doping like in AZO (differently than Al, In atoms do not substitute Zn atoms in the lattice), but the formation of a ternary compound, indium zinc oxide (IZO). In ternary compounds, the relative concentration metal atoms must be much higher compared to doped compounds to result on significant changes in the electrical properties of the material. **Figure 9a** and **b** show the

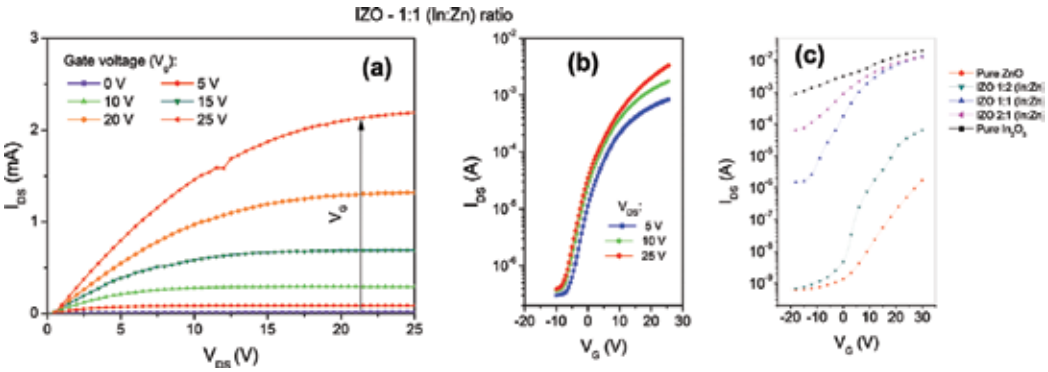

Figure 9. Output (a) and transfer (b) curves for a spin-coated IZO (1:1) TFT; (c) transfer curves for spin-coated TFTs at different IZO/ZnO compositions.

characteristic curves of a spin-coated IZO TFT using a 1:1 In:Zn molar ratio and treated at 350°C. It presents much improved TFT properties when compared to a ZnO TFT fabricated using similar processing method (**Figure 7a**). A saturation mobility of 5.32 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 4.3×10^4 is obtained, against 0.14 $cm^2V^{-1}\ s^{-1}$ and 1.3×10^3 for the pure ZnO TFT (first row of **Table 1**). Spray-coated TFTs comprising IZO layer were not produced due to the need of optimization of the spray deposition method for the solvent (2-methoxyethanol). However, the expectation is to obtain transistors with much superior performance by using spray-pyrolysis IZO active layer.

The transfer curves of TFTs comprising different active layers (pure ZnO, pure indium oxide and IZO at 1:2, 1:1 and 2:1 In:Zn molar ratios) are presented in **Figure 9c**. A gradual increase on the on current (and on the saturation mobility) is observed when the indium concentration increases from pure ZnO up to 1:1 In:Zn. For higher In concentrations, the increase in the on current is not significant. However, the off current (and the intrinsic conductivity as well) always increase with the indium concentration. As a result, the transistor performance improves due to the increase of the mobility until a In:Zn molar ratio of 1:1, but deteriorates for higher indium concentrations due to decrease of the on/off ratio and displacement of V_{th} and V_{on} toward negative values. Once again, we observe that a too conductive material like pure indium oxide does not result on superior performance transistor. As observed in **Figure 9c**, the pure indium oxide transistor has a too low on/off ratio and is not suitable for switching applications.

2.3.3. Atmosphere influence on TFT performance

In Section 2.1 we discussed briefly about the nature of the native defects which are responsible to the n-type character of ZnO. Theoretical calculations demonstrate that oxygen vacancies cannot be responsible for the unintentional n-doping of ZnO [12, 34, 35, 39]. However, reports on the increase of conductivity by increasing the oxygen pressure during sputtering deposition [14, 28, 40] are frequently mentioned as evidence that they play a key role in metal oxides n-type conductivity.

Atmospheric oxygen can also influence the electrical properties of ZnO TFTs even after the device manufacture. In **Figure 10a**, the transfer curves of a spray-coated ZnO TFT deposited at 350°C are presented as a function of exposure time in air. Previously to the experiment, the samples were annealed, in vacuum, at 150°C, for 1 h. Although differences in the electrical

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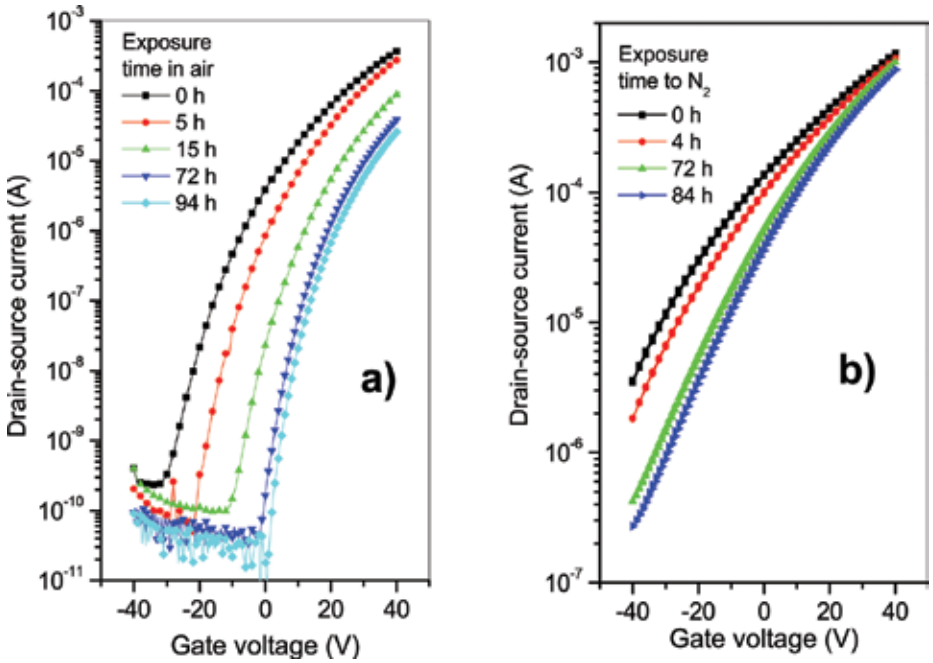

Figure 10. Transfer curves for a spray-coated ZnO TFT in different atmospheres: (a) in air; (b) in N_2, with H_2O and O_2 levels below 10 ppm (glove-box).

measurements could not be observed for short time intervals like few minutes, a significant change can be observed after 5 h in air. Both the intrinsic and on current continuously decrease as a function of time until about 40 h in air. After 40 h, the transfer curve seems to stabilize, with no substantial change until 94 h. **Figure 10b** shows the transfer curves for another transistor which was fabricated and annealed according the same conditions, but it was left inside a glove-box, with oxygen and water content lower than 10 ppm. The transfer curves show a slight variation in the first few hours, but also stabilize after about 40 h in N_2 atmosphere.

Figure 11 presents the evolution in time of the saturation mobility and the threshold voltage for the transistor exposed to air and for the transistor left in inert atmosphere (N_2). The variation in both parameters was higher for the transistor exposed to air. Moreover, the saturation mobility decreases when exposed to air and, in N_2, presents a small increase in the first 24 h. The threshold voltage, in both cases, shifts toward positive values. However, in N_2, it is still negative whereas, in air, it is positive. Negative V_{th} values in n-type TFTs are more associated to the increase of the intrinsic conductive than to the presence of charged defects. On the other hand, positive values of V_{th} in a n-type semiconductor is better explained by charge traps at the semiconductor/dielectric interface.

The significant variation on the electrical behavior of the ZnO TFT by exposure to oxygen rich atmosphere cannot be used, however, as evidence that the electron conductivity in ZnO is due to oxygen vacancies. Adsorbed atmospheric oxygen species can actually act as electron traps in ZnO, decreasing the electrical conductivity, but this effect can occur independently on which native defect generate free n-type charge carriers.

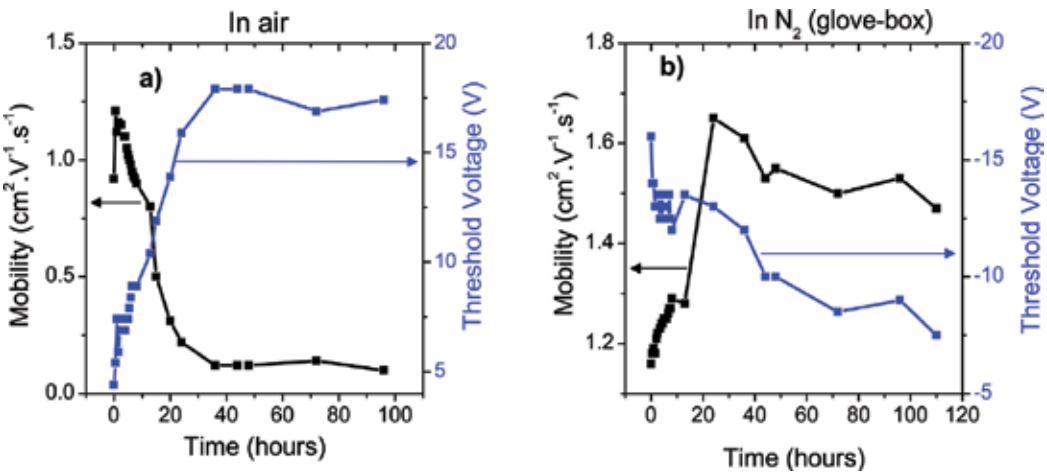

Figure 11. Time dependence of the mobility and threshold voltage for a spray-coated ZnO TFT in different atmospheres: (a) in air; (b) in N_2, with H_2O and O_2 levels below 10 ppm (glove-box).

2.3.4. TFT photoresponse in the UV range

The wide bandgap of zinc oxide (E_g ~ 3.37 eV) makes it a suitable UV sensing material since its response is not affected by visible light, differently to, for example, Si-based photosensors [32, 43–45]. Another interesting feature of ZnO-based devices is the occurrence of persistent photoconductive, that is, the material conductivity remains higher than the dark conductive even several hours after UV-light exposure. **Figure 12** shows this effect on a spray-coated ZnO TFT deposited at 350°C. The transistor was irradiated for 2 min by a UV LED (peak at 355 nm, irradiance of 68 μW/cm²) and then several transfer curves were recorded in a 6 h interval. The experiment shows that the saturation mobility increases more than 3 times and the threshold voltage shifts almost 15 V toward negative voltages by UV irradiation, taking more than 6 h return to the original values.

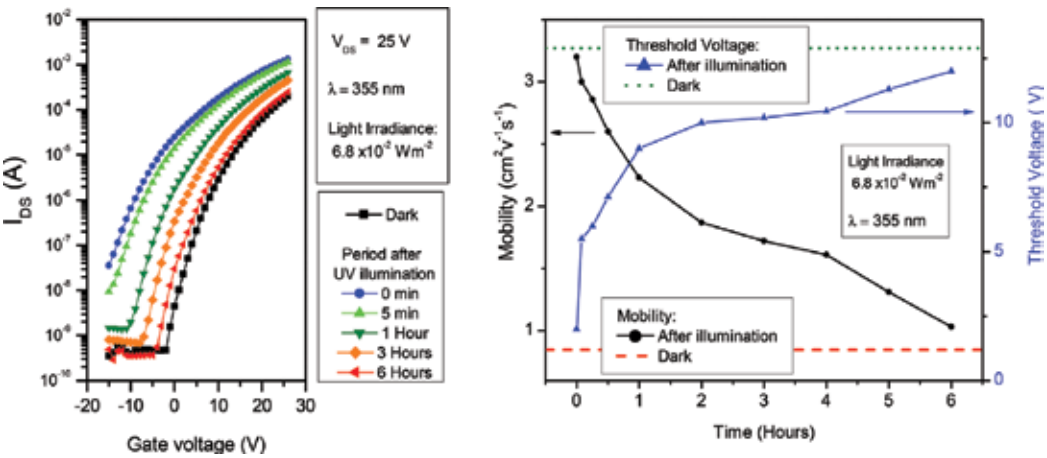

Figure 12. Electrical characteristics of ZnO TFT after UV exposure in air.

Such effects can be explained by the adsorption of atmospheric species, specially molecular oxygen, to the film surface. As described in the previous section, oxygen from the air adsorbs to the ZnO surface and acts as free electrons traps, decreasing the semiconductor conductivity. The photogeneration of electron–hole pairs causes the release of the adsorbed O_2 molecule by the recombination of the trapped electrons with the photogenerated holes [38], leaving free electrons in the bulk and, consequently, increasing the conductivity. The slow readsorption of oxygen molecules from the air is, therefore, the main mechanism behind the persistent photoconductivity effect observed in ZnO TFTs.

3. Conclusions

We made a brief review on the basic properties of semiconducting metal oxides and presented the advantages of using solution-processed metal oxides films as the active layer of high-performance thin-film transistors for transparent, low-cost and large-area applications. The presented results from ZnO TFTs indicate that spray-pyrolysis deposition has an enormous potential to provide devices with improved performance when compared to other deposition methods like spin coated, suggesting that further improvement can be achieved by using doped or ternary ZnO-related compounds like AZO or IZO. The observed dependence of the electrical properties of ZnO TFTs on the environment oxygen content and on the UV-light exposure endorse them as excellent candidates for gases, volatile compounds or UV-radiation sensors. The fact that ZnO TFTs present sensing responses that can be quantified by multiple parameters (μ_{sat}, V_{on}, V_{th}, I_{on}/I_{off}, SS, etc.) is a great advantage compared to the commonly proposed sensing units which usually present variations in a single parameter (like resistance, conductance or capacitance).

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Author details

João P. Braga[1], Guilherme R. De Lima[1], Giovani Gozzi[2] and Lucas Fugikawa Santos[2]*

*Address all correspondence to: lucas.fugikawa@unesp.br

1 Physics Department, IBILCE, São Paulo State University (UNESP), São José do Rio Preto, SP, Brazil

2 Physics Department, IGCE, São Paulo State University (UNESP), Rio Claro, SP, Brazil

References

[1] Kwack YJ, Choi WS. Solution-processed zinc-tin-oxide thin-film transistor by electrohydrodynamic spray. Electronic Materials Letters. 2012;**8**:341-344. DOI: 10.1007/s13391-012-1069-3

[2] Adamopoulos G, Bashir A, Wöbkenberg PH, Bradley DDC, Anthopoulos TD. Electronic properties of ZnO field-effect transistors fabricated by spray pyrolysis in ambient air. Applied Physics Letters. 2009;**95**:133507. DOI: 10.1063/1.3238466

[3] Li CS, Li YN, Wu YL, Ong BS, Loutfy RO. Performance improvement for solution-processed high-mobility ZnO thin-film transistors. Journal of Physics D: Applied Physics. 2008;**41**:125102. DOI: 10.1088/0022-3727/41/12/125102

[4] Krunks M, Mellikov E. Zinc oxide thin films by the spray pyrolysis method. Thin Solid Films. 1995;**270**:33-36. DOI: 10.1016/0040-6090(95)06893-7

[5] Lim SC, Oh JY, Koo JB, Park CW, Jung S-W, Na BS, Chu HY. Electrical properties of solution-deposited ZnO thin-film transistors by low-temperature annealing. Journal of Nanoscience and Nanotechnology. 2014;**14**:8665-8670. DOI: 10.1166/jnn.2014.10002

[6] Oh J-Y, Kang S-Y, Hwang C-S, Kim G-H, Ahn SD, Kim C-A, Koo JB, Suh K-S, Shim H-K. P-28: ZnO TFTs fabricated at room temperature by solution process. SID Symposium Digest of Technical Papers. 2008;**39**:1274. DOI: 10.1889/1.3069371

[7] Jun JH, Park B, Cho K, Kim S. Flexible TFTs based on solution-processed ZnO nanoparticles. Nanotechnology. 2009;**20**:505201. DOI: 10.1088/0957-4484/20/50/505201

[8] de Lima GR, Braga JP, Gozzi G, and Santos LF. Optimization of the electrical performance of metal oxide thin-film transistors by varying spray deposition parameters. MRS Advances. 2018;**3**:247-253. DOI: 10.1557/adv.2018.35

[9] Meyers ST, Anderson JT, Hung CM, Thompson J, Wager JF, Keszler DA. Aqueous inorganic inks for low-temperature fabrication of ZnO TFTs. Journal of the American Chemical Society. 2008;**130**:17603-17609. DOI: 10.1021/ja808243k

[10] Martins DE, Gozzi G, Santos LF. Influence of spray-pyrolysis deposition parameters on the electrical properties of aluminium zinc oxides thin films. MRS Advances. 2018;**3**:283-289. DOI: 10.1557/adv.2018.121

[11] Md Sin ND, Mamat MH, Mohammad RM. Optical properties of nanostructured aluminum doped zinc oxide (ZnO) thin film for thin film transistor (TFT) application. Advances in Materials Research. 2013;**667**:511-515. DOI: 10.4028/www.scientific.net/AMR.667.511

[12] Lin M-L, Huang J-M, Ku C-S, Lin C-M, Lee H-Y, Juang J-Y. High mobility transparent conductive Al-doped ZnO thin films by atomic layer deposition. Journal of Alloys and Compounds. 2017;**727**:565-571. DOI: 10.1016/j.jallcom.2017.08.207

[13] Diallo AK, Gaceur M, Fall S, Didane Y, Ben Dkhil S, Margeat O, Ackermann J, Videlot-Ackermann C. Insight about electrical properties of low-temperature solution-processed Al-doped ZnO nanoparticle based layers for TFT applications. Materials Science and Engineering B. 2016;**214**:11-18. DOI: 10.1016/j.mseb.2016.07.015

[14] Walker DE, Major M, Yazdi MB, Klyszcz A, Haeming M, Bonrad K, Melzer C, Donner W, von Seggern H. High mobility indium zinc oxide thin film field-effect transistors by semiconductor layer engineering. ACS Applied Materials & Interfaces. 2012;**4**:6835-6841. DOI: 10.1021/am302004j

[15] Park SM, Lee DH, Lim YS, Kim DK, Yi M. Effect of aluminum addition to solution-derived amorphous indium zinc oxide thin film for an oxide thin film transistors. Microelectronic Engineering. 2013;**109**:189-192. DOI: 10.1016/j.mee.2013.03.121

[16] Kim GH, Kim HS, Shin HS, Du Ahn B, Kim KH, Kim HJ. Inkjet-printed InGaZnO thin film transistor. Thin Solid Films. 2009;**517**:4007-4010. DOI: 10.1016/j.tsf.2009.01.151

[17] Yoon S, Kim SJ, Tak YJ, Kim HJ. A solution-processed quaternary oxide system obtained at low-temperature using a vertical diffusion technique. Scientific Reports. 2017;**7**:43216. DOI: 10.1038/srep43216

[18] Liu F, Qian C, Sun J, Liu P, Huang Y, Gao Y, Yang J. Solution-processed lithium-doped zinc oxide thin-film transistors at low temperatures between 100 and 300 °C. Applied Physics A: Materials Science & Processing. 2016;**122**:311. DOI: 10.1007/s00339-016-9903-3

[19] Zhang X, Zhai J, Yu X, Zhu R, Zhang W. Effect of annealing temperature on the performance of SnO_2 thin film transistors prepared by spray pyrolysis. Journal of Nanoscience and Nanotechnology. 2015;**15**:6183-6187. DOI: 10.1166/jnn.2015.10198

[20] Thomas SR, Pattanasattayavong P, Anthopoulos TD. Solution-processable metal oxide semiconductors for thin-film transistor applications. Chemical Society Reviews. 2013;**42**: 6910. DOI: 10.1039/c3cs35402d

[21] Perednis D, Gauckler LJ. Thin film deposition using spray pyrolysis. Journal of Electroceramics. 2005;**14**:103-111. DOI: 10.1007/s10832-005-0870-x

[22] Fortunato EMC, Barquinha PMC, Pimentel ACMBG, Gonçalves AMF, Marques AJS, Martins RFP, Pereira LMN. Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature. Applied Physics Letters. 2004;**85**:2541-2543. DOI: 10.1063/1.1790587

[23] Nomura K, Takagi A, Kamiya T, Ohta H, Hirano M, Hosono H. Amorphous oxide semiconductors for high-performance flexible thin-film transistors. Japanese Journal of Applied Physics. 2006;**45**:4303-4308. DOI: 10.1143/JJAP.45.4303

[24] Martins R, Barquinha P, Ferreira I, Pereira L, Gonçalves G, Fortunato E. Role of order and disorder on the electronic performances of oxide semiconductor thin film transistors. Journal of Applied Physics. 2007;**101**:44505. DOI: 10.1063/1.2495754

[25] Fortunato E, Barquinha P, Martins R. Oxide semiconductor thin-film transistors: A review of recent advances. Advanced Materials. 2012;**24**:2945-2986. DOI: 10.1002/adma.201103228

[26] Shi P, Huang L, Cui G, Zhang S, Zhang Y, Dong J, Yu W, Wang Y, Han D, Cong Y, Zhang X. High mobility transparent flexible nickel-doped zinc oxide thin-film transistors with small subthreshold swing. Electronics Letters. 2015;**51**:1595-1596. DOI: 10.1049/el.2015.2041

[27] Nomura K, Ohta H, Ueda K, Kamiya T, Hirano M, Hosono H. Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor. Science. 2003;**300**:1269-1272. DOI: 10.1126/science.1083212

[28] Morkoc H, Ozgur U. General properties of ZnO. In: Zinc Oxide. Fundamentals, Materials and Device Technology. Weinheim, Germany: Wiley-VCH Verlag GmbH & Co. KgaA; 2009. pp. 1-76. DOI: 10.1002/9783527623945.ch1

[29] Tsakonas C, Kuznetsov VL, Cranton WM, Kalfagiannis N, Abusabee KM, Koutsogeorgis DC, Abeywickrama N, Edwards PP. Low temperature sputter-deposited ZnO films with enhanced hall mobility using excimer laser post-processing. Journal of Physics D: Applied Physics. 2017;**50**:485306. DOI: 10.1088/1361-6463/aa9316

[30] Fortunato E, Pereira L, Barquinha P, Ferreira I, Prabakaran R, Gonçalves G, Gonçalves A, Martins R. Oxide semiconductors: Order within the disorder. Philosophical Magazine. 2009;**89**:2741-2758. DOI: 10.1080/14786430903022671

[31] Look DC, Farlow GC, Reunchan P, Limpijumnong S, Zhang SB, Nordlund K. Evidence for native-defect donors in n-type ZnO. Physical Review Letters. 2005;**95**:225502. DOI: 10.1103/PhysRevLett.95.225502

[32] Look DC. Progress in ZnO materials and devices. Journal of Electronic Materials. 2006;**35**:1299-1305. DOI: 10.1007/s11664-006-0258-y

[33] Özgür Ü, Alivov YI, Liu C, Teke A, Reshchikov MA, Doğan S, Avrutin V, Cho SJ, Morko¸ H. A comprehensive review of ZnO materials and devices. Journal of Applied Physics. 2005;**98**:1-103. DOI: 10.1063/1.1992666

[34] Janotti A, Van de Walle CG. Fundamentals of zinc oxide as a semiconductor. Reports on Progress in Physics. 2009;**72**:126501. DOI: 10.1088/0034-4885/72/12/126501

[35] Janotti A, Van de Walle CG. Hydrogen multicentre bonds. Nature Materials. 2007;**6**:44-47. DOI: 10.1038/nmat1795

[36] Brox-Nilsen C, Jin J, Luo Y, Bao P, Song AM. Sputtered ZnO thin-film transistors with carrier mobility over 50 $cm^2 V^{-1} s^{-1}$. IEEE Transcations on Electron Devices. 2013;**60**:3424-3429. DOI: 10.1109/TED.2013.2279401

[37] Kim H, Gilmore CM, Piqué A, Horwitz JS, Mattoussi H, Murata H, Kafafi ZH, Chrisey DB. Electrical, optical, and structural properties of indium–tin–oxide thin films for organic light-emitting devices. Journal of Applied Physics. 1999;**86**:6451. DOI: 10.1063/1.371708

[38] Kamiya T, Nomura K, Hosono H. Present status of amorphous In–Ga–Zn–O thin-film transistors. Science and Technology of Advanced Materials. 2010;**11**:44305

[39] Lin Y-Y, Hsu C-C, Tseng M-H, Shyue J-J, Tsai F-Y. Stable and high-performance flexible ZnO thin-film transistors by atomic layer deposition. ACS Applied Materials & Interfaces. 2015;**7**:22610-22617. DOI: 10.1021/acsami.5b07278

[40] Cui Q, Chandra S, McCahan S. The effect of dissolving gases or solids in water droplets boiling on a hot surface. Journal of Heat Transfer. 2001;**123**:719. DOI: 10.1115/1.1376394

[41] Schroder DK. Semiconductor Material and Device Characterization. Hoboken, NJ, USA: John Wiley & Sons, Inc.; 2005. 599 p. DOI: 10.1002/0471749095

[42] Sze SM, Ng KK. Physics of Semiconductor Devices. Hoboken, NJ, USA: John Wiley & Sons, Inc.; 2006. 815 p. DOI: 10.1002/0470068329

[43] Varma T, Periasamy C, Boolchandani D. Performance evaluation of bottom gate ZnO based thin film transistors with different W/L ratios for UV sensing. Superlattices and Microstructures. 2018;**114**:284-295. DOI: 10.1016/j.spmi.2017.12.054

[44] Vidor FF, Meyers T, Hilleringmann U, Wirth GI. Influence of UV irradiation and humidity on a low-cost ZnO nanoparticle TFT for flexible electronics. IEEE-NANO 2015-15th International Conference on Nanotechnology, Vol. 2. 2015. pp. 1179-1181. DOI: 10.1109/NANO.2015.7388836

[45] Jin Y, Wang J, Sun B, Blakesley JC, Greenham NC. Solution-processed ultraviolet photodetectors based on colloidal ZnO nanoparticles. Nano Letters. 2008;**8**:1649-1653. DOI: 10.1021/nl0803702

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In recent years, research on microelectronics has been specifically focused on the proposition of efficient alternative methodologies and materials to fabricate feasible integrated circuits. This book provides a general background of thin film transistors and their simulations and constructions. The contents of the book are broadly classified into two topics: design and simulation of FETs and construction of FETs. All the authors anticipate that the provided chapters will act as a single source of reference for the design, simulation and construction of FETs. This edited book will help microelectronics researchers with their endeavors and would be a great addition to the realm of semiconductor physics.

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