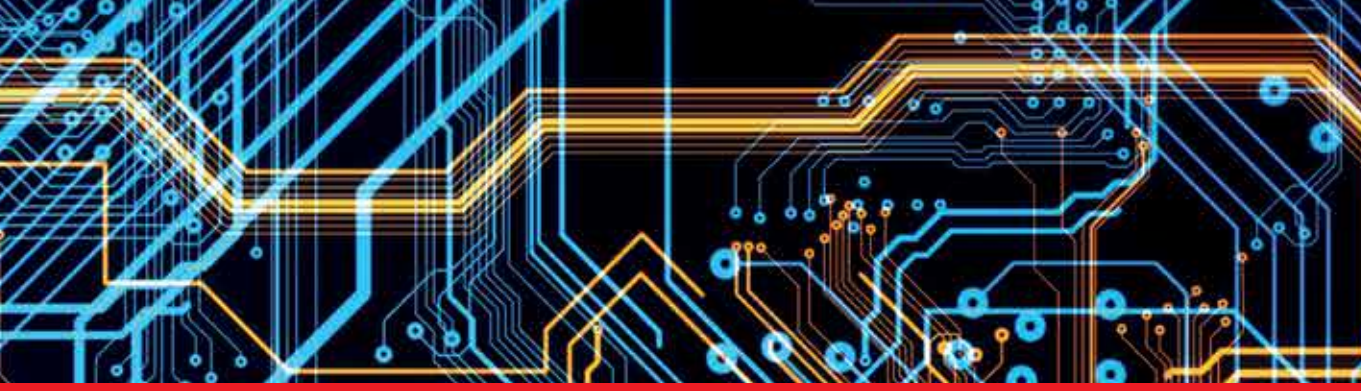

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Advanced Electronic Circuits

Principles, Architectures and Applications on Emerging Technologies

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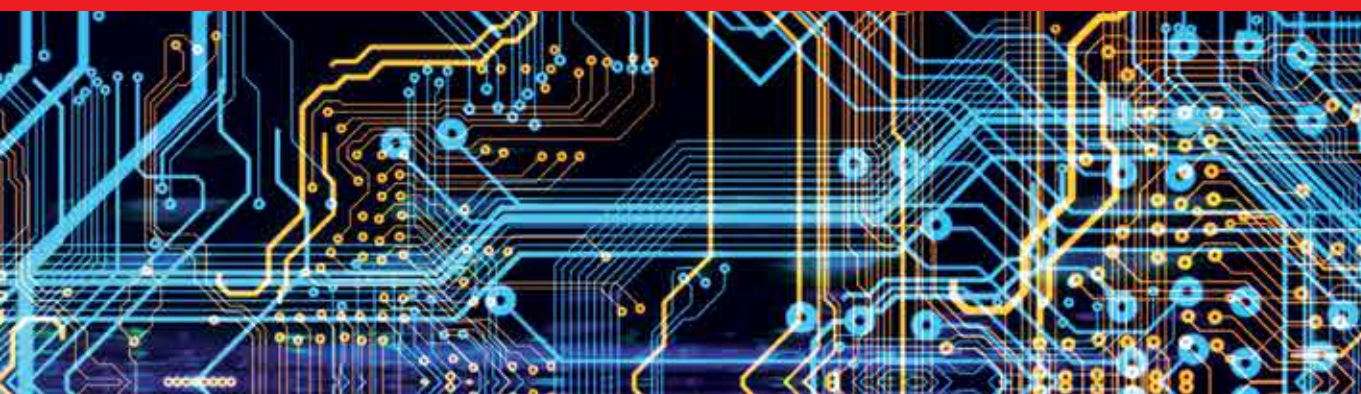

ADVANCED ELECTRONIC CIRCUITS - PRINCIPLES, ARCHITECTURES AND APPLICATIONS ON EMERGING TECHNOLOGIES

Edited by **Mingbo Niu**

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Meet the editor

Mingbo Niu received a BEng degree in Electronic Engineering from Northwestern Polytechnical University in China and an MSc (Eng.) degree (first-class) major in Communication and Information Systems from the same university. Prior to pursuing his PhD, he worked at the National Key Laboratory on Information and Signal Processing. He received his PhD degree in Electrical and Computer Engineering from the University of British Columbia, Canada, in 2013. From 2008 to 2012, he was a research assistant at Optical Wireless Communications Laboratory and Integrated Optics Laboratory, where he contributed to the development of ultra-high-speed optical data transmission links. Dr. Niu held a 2-year postdoctoral fellowship at Queen's University. He also worked for Defence Research and Development Canada (DRDC) at Calian Tech. Ltd where he contributed to statistical evaluation models of MIMO compressive sensing projects. He is now a professor of Electrical Engineering at Okanagan College, Canada. Dr. Niu has coauthored more than 20 IEEE and OSA papers and supervised a number of students' projects. Dr. Niu was the recipient of numerous scholarships during his undergraduate and graduate studies, which included a Chinese Government Award, two University of British Columbia University Graduate Fellowships, and a HuaWei Tech. Ltd Special Fellowship (first class). His current research and teaching interests include digital communications, microcontrollers, MIMO, DSP, energy harvesting, millimeter wave, electronic circuit theory, and ICs for data communication networks. Dr. Niu is a licensed Professional Engineer in British Columbia.

Contents

Preface

In the past several decades, the demand for high-speed, high reliable commercial and consumer electronic devices has increased exponentially. New technologies, architecture renovation, and new materials have been applied to the developed electronic circuit systems. The eight chapters in this book volume aim to introduce emerging advanced circuit design, structures, and applications, including ZnO nanomaterials, millimeter wave, energy harvesting circuitry, as well as compressive sensing technique in electrical and electronic systems.

Chapter 1 describes a novel self-starting DC-DC converter circuit using SiC for power electronic applications in up to 300 °C environments. The work presented in this chapter could be of interest to professionals who work in the field of power electronics. Chapter 2 presents ZnO nanomaterial-based piezoelectric structure design in the applications of polycrystalline solar cells. Based on the design, a prototype for energy harvesting operation was built and tested in a variety of irradiance operating conditions. Chapter 3 introduces a new nanoarchitecture for quantum-dot cellular automata principles and design, especially for high-speed digital circuit applications. Chapter 4 proposes an emerging millimeter wave receiver design, which would be of interest to the readers working on this frontier technology. The multiport circuit design work shown in this chapter can be a useful reference for millimeter wave engineers and researchers. Experimental results validate the theory and performance of this design. Chapter 5 discusses another emerging technology, compressive sensing. Compressive sensing has become an attractive technique in many applied research and engineering fields, such as big data, image processing, radar system, and wireless sensor networks. This chapter implemented compressive sensing technique in radar and localization applications. Chapter 6 gives a review on two popular memory technologies, namely, SRAM and DRAM. A new design of P-3T1D DRAM cell with much faster reading time is proposed for high-speed embedded system memory applications. Chapter 7 presents three small-scale wind energy harvester circuits for high-voltage applications. The methods, designs, and measurement results given in this chapter can be useful to energy harvesting circuit design engineers. Chapter 8 describes an experimental work on characterizing electrical nonlinear bimodal transmission line. The experimental approach proposed in this work allows tracing the curve dispersion of a nonlinear transmission line.

These eight chapters cover a wide range of topics: from new materials and architectures to emerging technologies and advanced circuit design. This high-quality book volume would not have been possible without the collaboration of the authors, the reviewers, and the staff at InTech Open who assisted in the initial preparation, quality check, and final production phases. I would like to thank all of them for their invaluable work and time in producing this book volume. I hope that the readers enjoy this book volume and find it as a good reference in circuit design and applied research.

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Section 1

New Materials for Electric Circuits

Chapter 1

Self-Oscillatory DC-DC Converter Circuits for Energy Harvesting in Extreme Environments

Ming-Hung Weng, Daniel Brennan, Nick Wright and Alton Horsfall

Additional information is available at the end of the chapter

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Abstract

A novel self-starting converter circuit technology is described for energy harvesting and powering wireless sensor nodes, constructed from silicon carbide devices and proprietary high temperature passives for deployment in hostile environments. After a brief review of the advantages using Silicon Carbide (SiC) over other semiconductors in extreme environments, the chapter will describe the advantages and principles when designing circuitry and architectures using SiC for power electronics. The practical results from a novel self-starting DC-DC converter are reported, which is designed to supply power to a WSN for deployment in high temperature environments. The converter operates in the boundary between continuous and discontinuous mode of operation and has a Voltage Conversion Ratio (VCR) of 3 at 300°C. This topology is able to self-start and so requires no external control circuitry, making it ideal for energy harvesting applications, where the energy supply may be intermittent. Experimental results for the self-starting converter operating from room temperature up to 300°C are presented. The converter output voltage, switching frequency, total power loss and efficiency were presented at temperatures up to 300°C.

Keywords: wide band gap semiconductors, silicon carbide, SiC, energy harvesting, wireless sensor networks, high temperature circuit, switching frequency, MOSFETs, JFETs, DC-DC power converters, field effect transistor switches

1. Introduction

In recent years there has been increasing demand to investigate and monitor ever more hostile environments including those containing high temperatures and/or extreme radiation flux [1–3]. Silicon carbide (SiC) boasts a much higher band gap than conventional silicon and is therefore

more chemically stable allowing electronic circuits made from this material to be deployed in environments where conventional silicon based electronics cannot function.

The development of silicon carbide (SiC) technology has become increasingly rapid in recent years with significant improvements in wafer and epitaxy growth technology of 8-inch and beyond [4]. By offering scalable and cost-effectively materials processing, SiC devices have become part of the mainstream in power electronic applications [5, 6] and a number of conferences are running dedicated sessions to the deployment of this technology from niche to mainstream. Further advantages in terms of small, signal level devices [7], sensors [8] and CMOS circuitry [9] have resulted in significant improvements in capabilities, however these are still only available at research level, where a number of groups are active. During recent years, SiC has emerged as a promising material for electronics where the underlying rationale for the continued investment in SiC technology is the excellent material properties. SiC is the only technologically relevant semiconductor that has a stable thermal oxide (SiO_2) [10] and can exist in a large number of polytypes – different crystal structures built and derived from the high chemical stability of the SiC sub-unit organised into different stacking sequences. All forms of SiC are considered a wide bandgap material since the electronic bandgaps of the different polytypes range from 2.4 to 3.3 eV. The bandgap of 4H SiC is 3.23 eV at room temperature (compared to 1.12 eV for silicon) and this dramatically reduces the intrinsic carrier concentration in comparison to semiconductors such as silicon or gallium arsenide and this allows devices to theoretically operate at temperatures up to 1000°C [11]. Electrical properties of SiC tailored toward devices also has a high saturation electron velocity, 2×10^7 cm·s^{-1}, a thermal conductivity in excess of copper at room temperature and a critical electric field that is almost an order of magnitude higher than that of silicon. Fulfilling technical parameters and standards, SiC has been exploited in the high performance power MOSFETs and diodes that are commercially available, but also have the potential to realise high performance, high frequency oscillators, amplifiers and different topologies power inverters.

For these high temperature environments are incompatible with standard battery technologies, and so, energy harvesting is a suitable technology when remote monitoring of these extreme environments is performed through the use of wireless sensor nodes (WSNs) [12–14]. There is now a variety of energy harvesting devices available which are capable of producing sufficient energy from the ambient surroundings to intermittently power a WSN [15–17]. Energy harvesting devices often produce voltages which are unusable directly by electronic loads and so require power management circuits to convert the electrical output to a level which is usable by monitoring electronics and sensors. Therefore a DC-DC step-up converter that can handle low input voltages is required [18, 19]. The required gate-drive circuitry for these converters need to be placed next to the switches to minimise system complexity, however, the successful operation of the gate drivers, especially with no heat sink in hostile environments will increase the power density for DC-DC converter modules. The advantages of SiC based power devices include high current densities, faster switching speeds and high temperature capabilities. To fully utilise the benefits of SiC devices in DC-DC converters used in harsh environments, the gate drive design requires special attention. To match the high temperature capabilities of SiC devices, the gate drivers also need to be capable of operation at these elevated temperatures [20, 21].

SiC based switches such as SiC JFETs are capable of tolerating these elevated temperatures, however, various other components such as passives, magnetics or amplifiers will make this task rather challenging. From a system point of view, the gate drive requirements of normally-on SiC JFETs are a significant challenge. The issue with the start-up process in addition to the differences in the gate voltage requirements make them less desirable for power designers [22, 23]. However, the specific on-resistance of normally-off (enhancement-mode) JFETs is almost 15% higher than their normally-on counterparts [24]. Therefore in a circuit where on state losses are expected to be the dominant power losses, the normally-on (depletion mode) JFETs are better alternatives. Another disadvantage of normally-off SiC JFETs is that in order to keep the device in the on state, the gate-source junction must be forward biased [25]. This implies that similar to SiC based BJTs, there is a considerable drive current requirement, which undesirable.

2. Power sources and energy options for wireless sensor nodes

2.1. Power sources for wireless sensor nodes

Wireless sensor networks have become a very popular enabling technology and have already entered the market place in a number of sectors. The majority of these platforms are powered by limited-life batteries. Hence alternative power sources are being continuously investigated and employed [26].

The rapid reduction in the size and power consumption of electronic components has helped speed up the research on communication nodes and wireless sensors. As the size of these WSNs decreases, their use becomes more widespread in the automobile industry, industrial environments and aerospace industry. However, their respective power supply has become a major issue, because the size reduction in CMOS electronics has significantly outpaced the energy density improvements in batteries, which are the most commonly used power sources. Consequently, the power supply is the limiting factor on both the size and lifetime of the sensor node. Energy reservoir power sources such as micro-scale batteries, micro-fuel cells, ultra-capacitors are characterised by their energy density and can be used to power WSNs but at the cost of increased size and reduced lifetime. Power scavenging sources are an alternative power source. Unlike energy reservoirs, power scavenging sources are characterised by their power density; the energy provided from these sources depends on the amount of time each source is in operation [26–29]. One of the popular power scavenging sources is via temperature gradients [30, 31]. Energy can be scavenged from the environment using the temperature variations that naturally occur. The maximum power-conversion efficiency from a temperature difference, the Carnot efficiency is given below in Eq. (1), where the temperature is in Kelvin:

$$\eta = \frac{\left(T_{high} - T_{low}\right)}{T_{high}} \tag{1}$$

Assuming a room temperature of 27°C and for a source 5°C above room temperature, the maximum efficiency is 1.64% and for a source 10°C above room temperature is maximum efficiency is 3.22%. At low temperature differences and small scales, conduction will dominate

and convection and radiation can be neglected. The heat flow through conduction is given by Eq. (2), where L is the length of material that the heat is flowing through and k is the thermal conductivity of the material used:

$$q' = k\frac{(\Delta T)}{L} \tag{2}$$

Assuming a length of 1 cm and a temperature difference of 10°C, the heat flow (power) for silicon with a thermal conductivity of 140 W/mK is 14 W/cm^2. Assuming that Carnot efficiency could be achieved, the output power would be 451 mW/cm^2 which is significantly higher than comparable power sources. In practice, the efficiencies for this type of energy harvester are well below the Carnot efficiency. One of the most common ways to convert the generated power from temperature differences to electricity is by using thermoelectric generators.

2.2. Thermoelectric generators

Driving a wireless sensor node from ambient is attractive as it eliminates the need for wires or batteries. Despite the clear advantages of energy harvesting, these systems require a suitable power management strategy to convert the low voltage levels to a level usable by the wireless sensor systems. Many WSNs monitor physical quantities, which change slowly and therefore the measurements can be taken and transmitted less frequently. This means lower operating duty cycle and therefore many wireless sensor systems consume very low average power, hence they are suitable candidates for energy harvesting power sources.

Thermoelectric generators (TEGs) are energy harvesting devices capable of producing large amounts of current at low voltages from a thermal gradient across the device; through a phenomenon known as the Seebeck effect [32]. Modern TEG's are constructed out of p-n junctions of different semiconductor materials depending on their operational requirements, but commonly bismuth telluride (Bi_2Te_3). The mechanical construction of a typical TEG is shown in **Figure 1**.

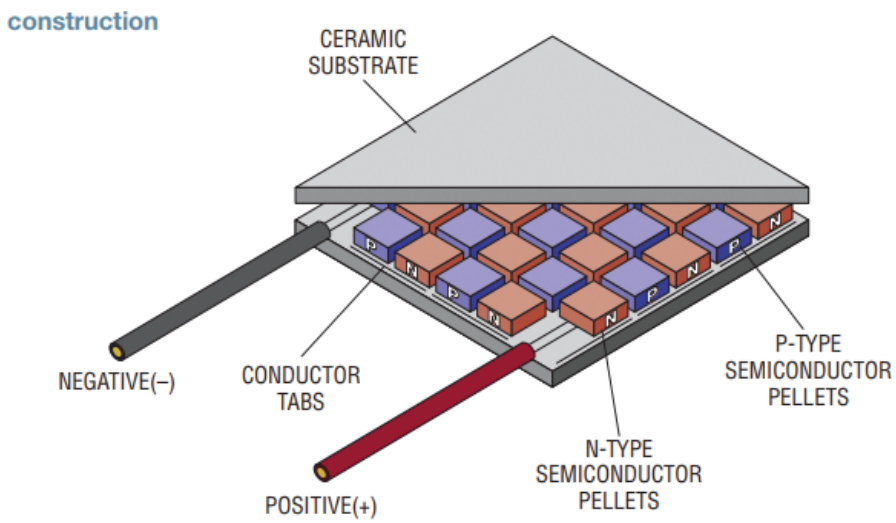

Figure 1. Construction of a thermoelectric generator [33].

In this work a standard off-the-shelf TEG manufactured by Marlow (product number TG 12-801 L) was characterised in terms of the electrical output as a function of temperature difference between the two surfaces. A ceramic hotplate was used to provide a controlled temperature heat source whilst a thermocouple embedded into the base of a heat sink and fan provided the cooler side thus creating a measurable temperature difference across the device. The higher the temperature difference, the greater the output voltage becomes at any given current. **Figure 2** shows the output power of the thermoelectric generator as a function of the output voltage. The solid line intersects with the waveforms where the maximum output power is at the optimum output voltages. The optimum voltage for the TEG is generally below 1.3 V and needs to be boosted in order to enable the operation of the circuit for remote sensor applications.

2.3. The need for a high temperature self-starting DC-DC converter

In addition to the Voltage Conversion Ratio (VCR) requirements to supply a SiC sensor circuit, operating in a very high temperature environment (up to 300°C) demands a high temperature step-up DC-DC converter. In addition to the power stage of the converter, the gate-drive circuitry is also required to operate at elevated temperatures. To eliminate the need for a high temperature gate driver and also to reduce the size of the power management circuitry, a self-starting DC-DC converter is desired [34]. Here, a self-starting DC-DC converter was designed to boost the low DC output voltage of a thermoelectric generator to a level sufficient to run a SiC sensor circuit for wireless monitoring of inhospitable environments [35–37]. These environments may be subject to high temperatures in the case of exhaust gas monitoring in turbine engines or oven environments, they may also be subject to radiation in the nuclear industry whether they are used in power generation or waste monitoring. The proposed DC-DC converter does not need an auxiliary power supply to drive the normally-on JFET. The converter self-starts and does not suffer from a start-up shoot through. The requirement of self-oscillation needs a depletion mode device (e.g. normally-on JFET) as there will be no current flowing at start otherwise.

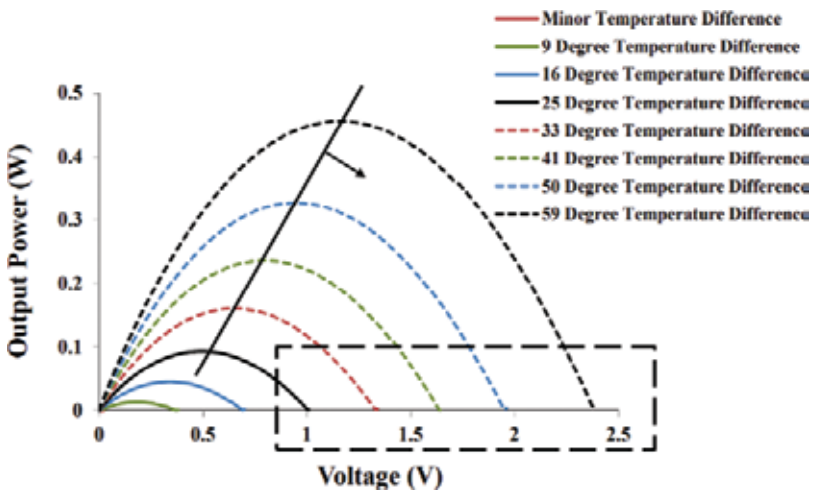

Figure 2. Output power as a function of voltage for the thermoelectric generator for various temperature differences.

3. Theory behind the self-starting DC-DC converter

Figure 3 shows the circuit diagram of the proposed self-starting DC-DC converter designed for boosting low level voltages from the TEG, denoted in the **Figure 3** as V_{in}. The input capacitance of the circuit, C_{in}, represents the capacitance of the p-n junctions of the TEG. Based upon a standard boost converter topology and a blocking oscillator, the key aspect of the design is the use of a counter-wound secondary winding in conjunction with a normally-on device which is used to provide the self-oscillatory behaviour, thus eliminating the need for an external gate drive [38]. The elimination of a separate gate drive is crucial for the successful commissioning of a silicon carbide energy harvesting system designed for use with low voltage DC sources such as solar cells and thermogenerators. The voltages provided by these sources are magnitudes smaller than the voltages required to provide the gate drive requirements for a conventional converter topology; therefore a self-oscillating design becomes the only viable option.

The simplicity of the design is also important when considering the capability of high temperature components. At present, commercially available SiC components are limited to discrete power devices and do not include the control circuitry required for complex designs. The commercial drive behind silicon carbide electronic devices to date has been focussed on the power electronics market, where the ability of silicon carbide to operate at high frequencies and with low power losses has been utilised for the realisation of highly efficient circuits that offer significant space saving over conventional systems. Here it is demonstrated that the ability of silicon carbide components to operate at these high temperatures can be harnessed for the production of a step-up converter with the ability to power circuits within the high temperature environment itself, with minimum component count, thus reducing the overall cost of a high temperature energy harvesting system.

3.1. Principle of operation

As shown in **Figure 4**, the self-oscillating converter circuit uses a depletion mode JFET and a Schottky diode in a boost configuration, wherein coupled inductors are used to feed the gate-source of the SiC based switching device and act to initialise the oscillations. The operation of the circuit is as follows; at start-up and as the input voltage rises, the SiC JFET as a normally-on device conducts and the current flows through the inductor. The current in the primary

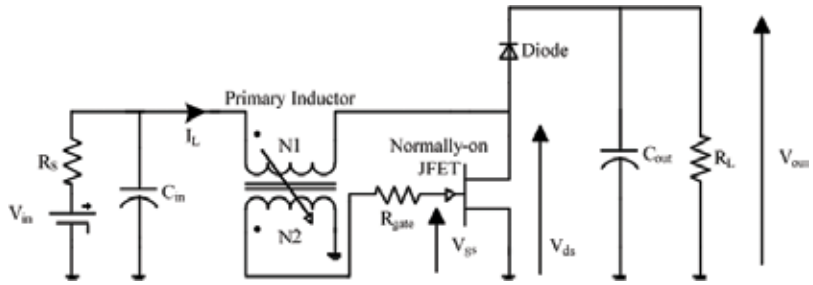

Figure 3. The proposed self-starting boost converter.

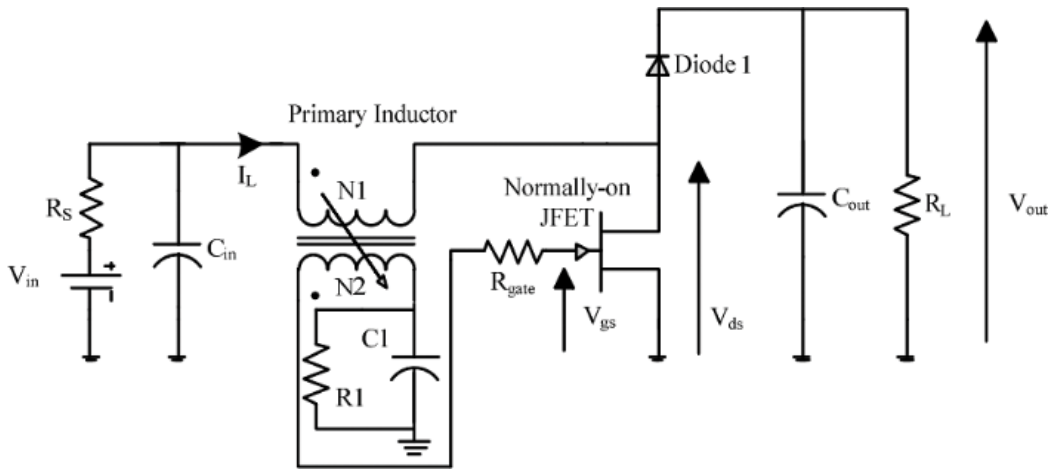

Figure 4. The self-starting step-up converter with the paralleled RC.

winding of the coupled inductor increases exponentially with time reducing the voltage across the primary winding, inducing a voltage on the secondary winding of the transformer due to the change in the primary current. Capacitor C1 is charged to a negative voltage with respect to the circuit ground. When the bias across the capacitor exceeds the pinch off potential of the JFET, the on state resistance of the JFET increases, so that the current through the FET drops to zero. This reduction in current flowing through the JFET results in the decrease in the current flow through the primary winding of the transformer. When the current in the primary winding becomes zero, the voltage on the secondary winding reaches zero as well and C1 is discharged through the resistor R1 to ground. Once the bias across the capacitor falls below the pinch off potential of the JFET, the on state resistance of the JFET reduces significantly, current flows through the primary winding of the inductor and the circuit operation repeats. The switching frequency of the converter is determined primarily by the gate-source capacitance of the SiC JFET and the inductance of the primary side of the drive transformer.

As shown by the circuit topology in **Figure 5** the RC circuit connected to the JFET gate can be removed and the secondary winding directly connected to ground. The stray capacitance of the primary winding is sufficient to enable the self-oscillation occur and the converter operates without the inclusion of the external RC components.

When the normally-on silicon carbide JFET conducts, current begins to flow through the primary winding of the transformer and the channel of the JFET to ground, this induces a negative bias in the secondary winding. As the current flowing through the primary winding increases, the negative voltage on the secondary winding increases in magnitude and the channel of the JFET is progressively pushed toward pinch off. Once the magnitude of the voltage on the secondary winding reaches the threshold voltage of the JFET, the JFET becomes non-conducting. This causes the magnetic field contained in the ferrite core of the transformer to collapse and the voltage in the primary winding increases as is observed in a standard boost converter topology. Whilst the JFET is non-conducting, power is transferred to the output

through the silicon carbide Schottky diode at a higher voltage level. The voltage induced on the secondary winding then drops due to reduced current flow in the primary and the JFET transistor becomes conducting again to complete the switching cycle.

During operation the converter operates at the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM), the operating point often described as critical conduction mode. When the JFET is non-conducting, the voltage induced on the secondary winding decreases due to reduced current flow in the primary. Therefore the JFET becomes fully conducting again when the inductor current has reached zero, which results in a zero voltage on the gate of the normally-on JFET. The schematic in **Figure 6** illustrates the current waveform in the primary inductor for a converter operating in critical conduction mode. During the on time (denoted by DT) the energy stored in the inductor increases and during the off-state (the remainder of the waveform) the inductor fully discharges. The end of the switching period coincides with the point at which the current through the inductor and hence the energy stored in the inductor falls to zero. In **Figure 6**, the average current I_{avg} is half the peak current, I_{peak}. This peak current is determined by the rate of change of current through the primary inductor during the charging and discharging portions of the waveform.

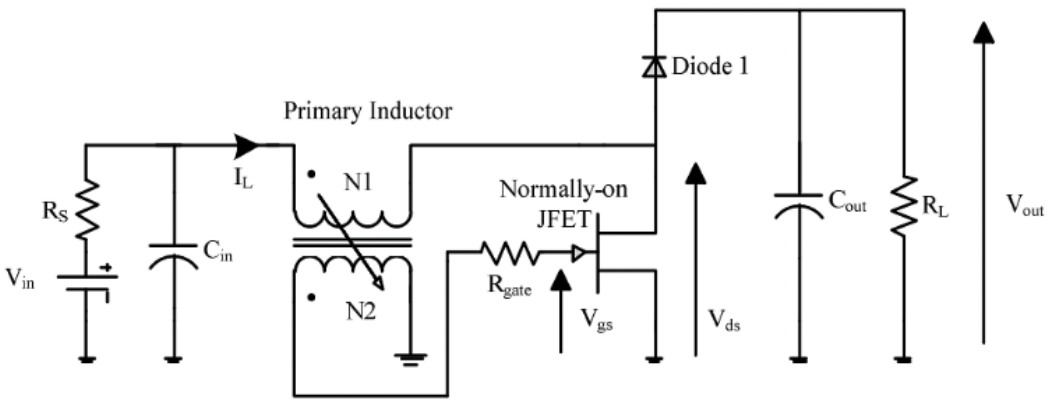

Figure 5. The self-starting step-up converter without the paralleled RC.

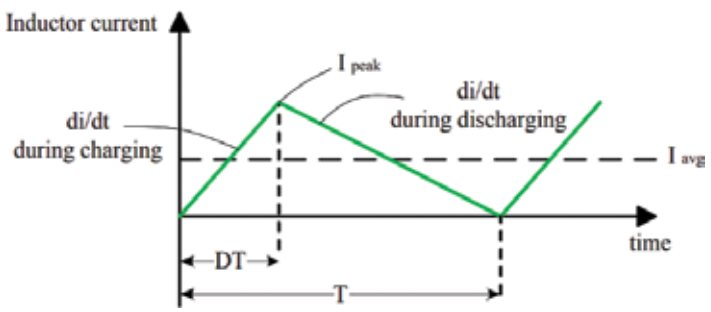

Figure 6. The critical mode of operation, boundary between CCM and DCM.

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4. The self-starting DC-DC converter

4.1. Experimental results

The SiC JFET and SiC Schottky diode were packaged in high temperature ceramic packages and the circuit was tested in a temperature controlled oven. Both the Schottky diode and JFET were fabricated using process techniques developed at Newcastle University [39–41]. The data in **Figure 7** show the I-V characteristics of the JFET used in the circuit.

Of note is the pinch off potential of the device, which is approximately −6.5 V, which is found to be optimal. FETs with a more negative pinch potential require a higher rate of change of current through the primary inductor in order to pinch off the channel – making them unsuitable for use in energy harvesting environments. A pinch off potential closer to zero offers advantages in terms of requiring a lower rate of change of current through the primary inductor. However, when the gate voltage is zero, the on state resistance of the channel is higher [42] and this reduces the efficiency of the converter. As shown by the circuit schematic in **Figure 8**, a 100 kΩ resistor was used as the load to mimic a wireless sensor node designed for high temperature energy harvesting applications. Typically due to the low power levels available in a circuit powered by energy scavenging, sensor nodes are designed to intermittently use the power generated, thus reducing the time averaged power draw, as there is insufficient power generated to continuously run a sensor node. This is specifically relevant where the node is based on the wireless transmission of data to a remote access node [43].

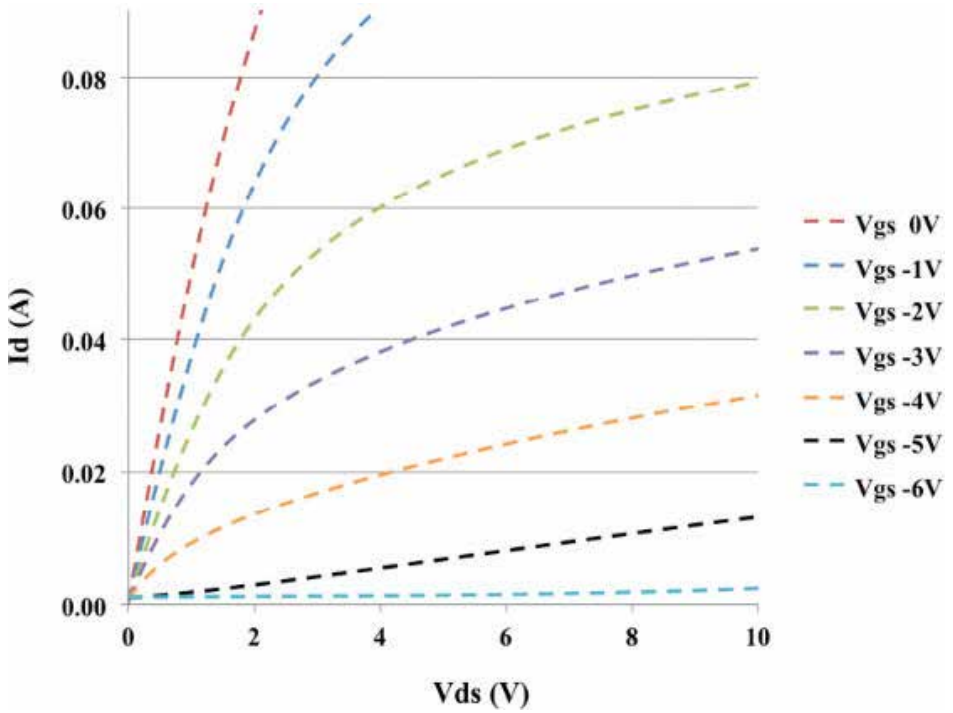

Figure 7. I-V characteristics of the SiC JFET used in the converter at 25°C.

The data in **Figure 9** show the voltage waveforms of the JFET during room temperature operation with an input voltage of 1 V. From **Figure 9** it can be observed that the gate voltage of the FET (denoted by Vgs) reaches the pinch off potential, setting the current thorough the FET to zero, before rapidly becoming positive, resulting in a significant reduction in the on state resistance. The voltage across the FET channel, denoted by Vds, increases as the gate voltage becomes more negative, reaching a value of 5.5 V when the channel is fully pinched off. This enhancement in the voltage across the FET in comparison to the input voltage arises from the energy stored in the inductor and is the fundamental principle behind the operation of a boost converter. The voltage across the JFET reduces to zero when the gate voltage is positive, showing that the JEFT is conducting.

The data in **Figure 10** show the variation in converter output voltage as a function of temperature for a range of input voltages that are relevant to energy harvesting from a thermoelectric generator. It can be seen that the boost converter can successfully operate at input voltages

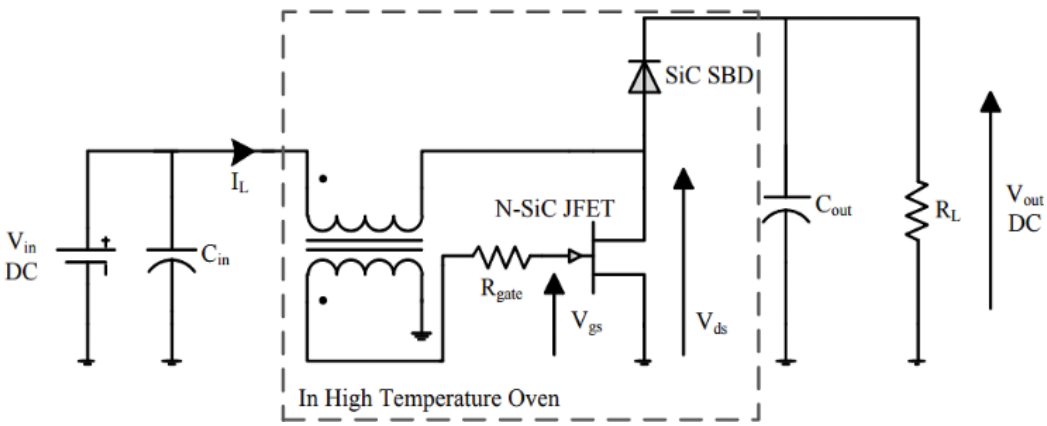

Figure 8. Schematic of the SiC self-starting DC-DC converter.

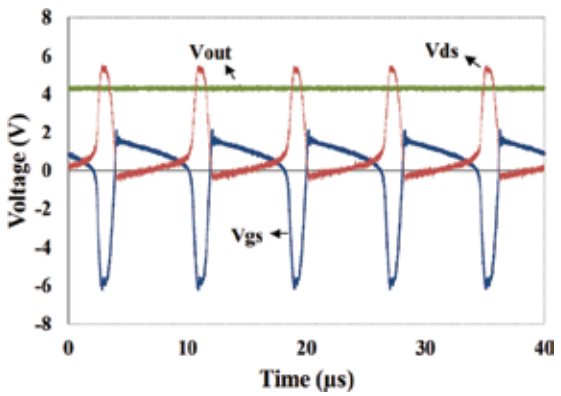

Figure 9. Voltage waveforms of the self-starting boost converter.

between 1.3 and 2.5 V over the full 300°C range, demonstrating boost capabilities of up to 4.5 times the input voltage. At higher temperatures, the output voltage drops due to the increased SiC diode forward voltage drop, increased JFET on-resistance and increased copper loss in the inductor windings. The effect of these is also apparent in the data shown in **Figure 12**. At input voltages below 1.2 V, the converter does not self-start at high temperatures. At input voltages of 1, 1.1 and 1.2 V the converter failed to self-start at temperatures above 150, 200 and 250°C, respectively. This is thought to be related to the reduction of the mutual inductance between the primary and secondary windings of the inductor caused by the magnetic properties of the ferrite being adversely affected. Therefore the voltage induced in the secondary as a result of the rate of change of current in the primary winding is lower, resulting in the gate voltage of the JFET being insufficient to reach the pinch off potential. In this situation the current through the JFET does not reduce to zero and the energy stored in the inductor is not transferred to the load as the voltage is lower than the turn on voltage of the diode and the converter does not operate.

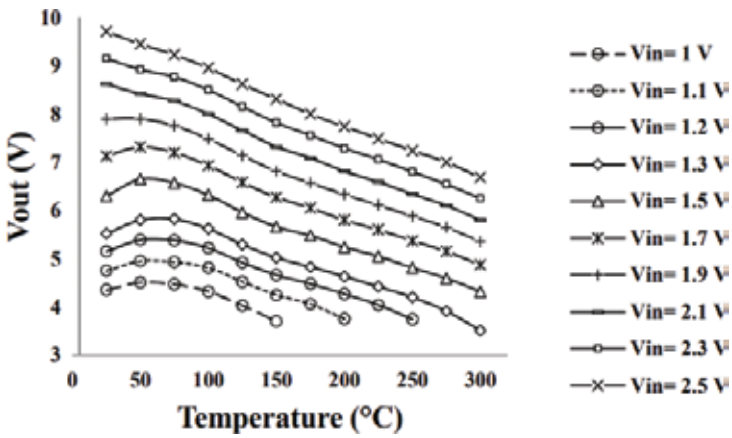

Figure 10. Output voltage as a function of temperature.

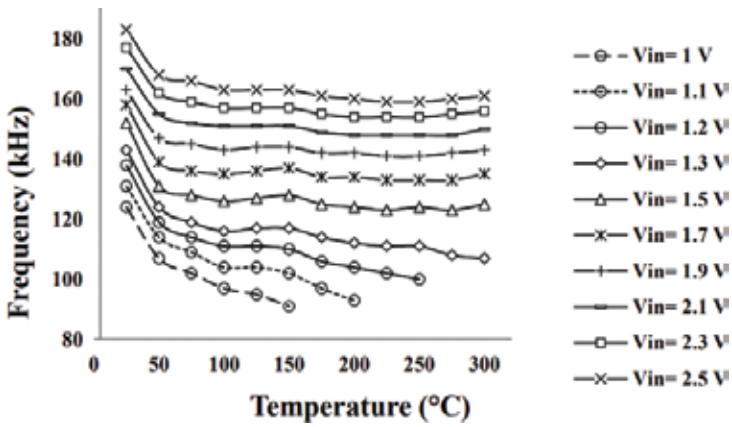

Figure 11. Switching frequency as a function of temperature.

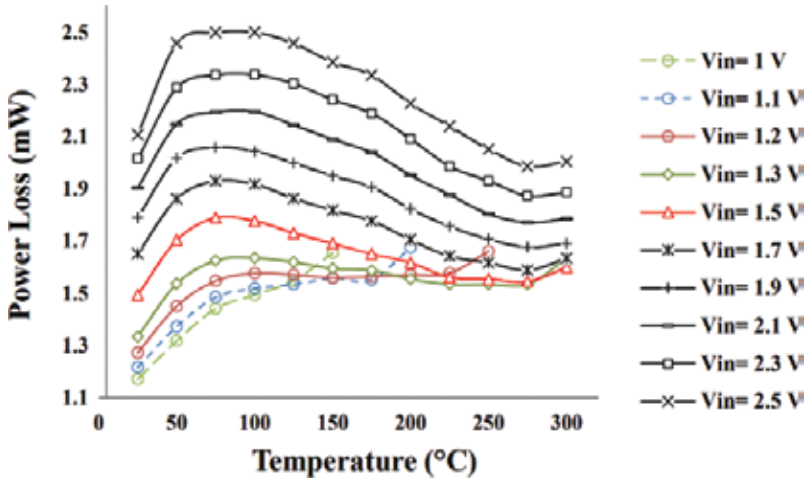

Figure 12. Power losses as a function of temperature.

In order to enable operation at lower input voltages, the turns ratio between the primary and secondary coils of the transformer can be increased, however this is limited by the physical size of the ferrite core used in this work. Based on the data shown in **Figure 8**, it can be seen that this converter is capable of boosting the energy harvested from a thermogenerator with a temperature difference of 40°C. Energy harvesting from lower temperature differences is possible using two thermogenerators connected electrically in series but thermally in parallel.

The results in **Figure 11** show the effect of temperature on the operating frequency of the circuit. As described previously, the frequency of operation is determined by the rate of change of current in the primary winding of the transformer (which can be described in terms of the inductance of the winding) and the input voltage from the thermogenerator. This is directly related to change in the material properties of the ferrite core with temperature. As the temperature increases, the permeability and saturation magnetisation of the ferrite core reduces, resulting in the shift in the magnitude of the inductance of the primary winding. Therefore increasing the ambient temperature from 25 to 300°C, results in the switching frequency of the converter decreasing from 183 to 161 kHz and from 143 to 107 kHz at input voltages of 2.5 and 1.3 V, respectively. As can be seen from the data in **Figure 11**, the switching frequency also increases with input voltage when increasing the supply from 1 to 2.5 V. This increase is directly linked to the rate of change of current in the primary winding.

The overall power losses and efficiency of the converter circuit as a function of temperature is shown in **Figures 12** and **13**, respectively. As can be seen from the data, the efficiency is lower at higher temperatures. This reduction is to be expected, as the resistance of the JFET channel increases due to the reduction in electron mobility [44] and the parasitic resistance of the inductor winding increasing. The diode voltage drop of the SiC Schottky diode also increases with temperature [45], however the effect is minor in comparison to the changes in the JFET and inductor. Hence, the overall power losses in the circuit increase. Increasing the input voltage results in higher power losses in the converter, due to the increased reverse voltage

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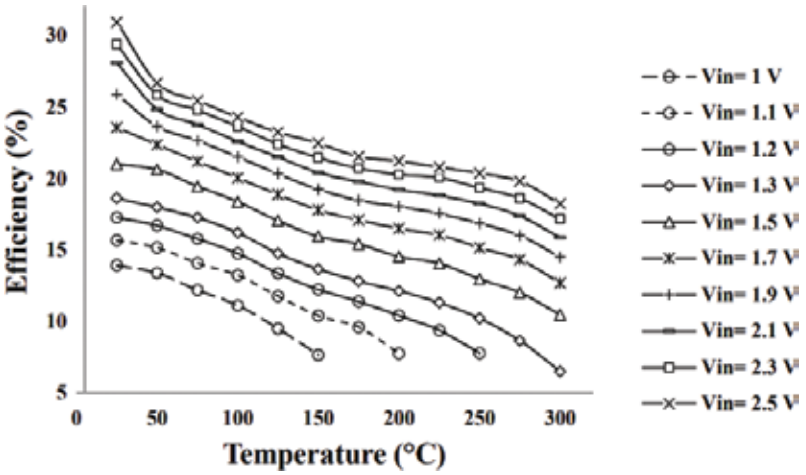

Figure 13. Efficiency of boost converter as a function of temperature.

across the SiC JFET during switching. The current ripple in the inductor also increases, resulting in higher conduction losses in the inductor. As the output voltage changes with temperature, the output power transferred to the constant resistive load also changes with temperature.

As can be seen from the data in **Figure 12**, the increasing temperature results a reduction in the overall power losses; which can be explained by the reduced current in the resistive load due to the reduced output voltage. The reduction in the output voltage with temperature results in a reduced drain-source voltage for the JFET, resulting in the JFET operating in the linear region (as can be seen from the data in **Figure 7**), resulting in the SiC JFET acting more like a resistor at temperatures above 275°C and so the power losses start to increase with temperature. This can be seen in **Figure 12** for the data relating to input voltages of 1 and 1.1 V, where a significant increase in power loss occurs at 150 and 200°C respectively. As the output power from the converter is low, the losses in the circuit will play a significant role in the overall efficiency of the circuit.

To assess the converter performance at higher output currents, a 10 kΩ resistor was connected as the load and the converter performance was characterised for a range of input voltages at different temperatures. The converter output voltage as a function of temperature for a range of input voltages is shown by the data in **Figure 14**. As can be seen from the data, the output voltage of the converter decreases as the temperature increases, in a manner similar to that for the 100 kΩ load, as shown in **Figure 10**. At higher output current levels, the overall conduction and switching losses increase in the converter, resulting in a drop of the output voltage. As the load current has increased (10 kΩ), the output voltage of the converter is lower when compared to the case with a 100 kΩ load, due to the increased conduction losses.

Similarly to the operation of the converter with the 100 kΩ output resistor, at input voltages below 1.3 V, the converter is not capable of self-starting at high temperatures. At input voltages of 1, 1.1, 1.2 and 1.3 V the converter did not self-start at temperatures above 125, 175, 200 and 250°C,

respectively. At a higher output current, the effective voltage across the primary inductor is lower; due to the increased voltage drop across the parasitic resistance in the inductor, resulting in a lower induced voltage in the secondary winding. As described for the 100 kΩ load above, if this gate voltage on the JFET, which is equal to the voltage induced in the secondary winding does not reach the pinch off potential of the device, the converter will not oscillate. Hence for the higher output current (10 kΩ load) the converter is capable of self-starting operation at lower temperatures in comparison to the case with a 100 kΩ load resistor.

The converter overall efficiency as a function of temperature is shown by the data in **Figure 15**. As can be seen from the data, the efficiency of the converter is approximately twice that of the

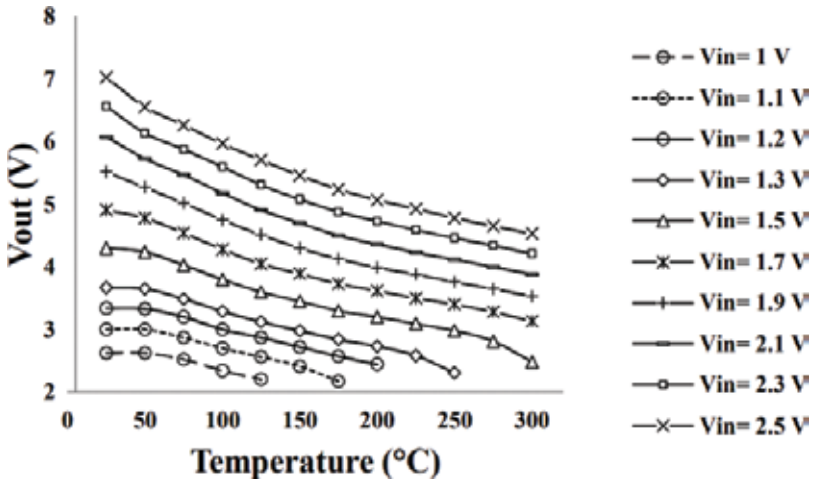

Figure 14. Output voltage as a function of temperature.

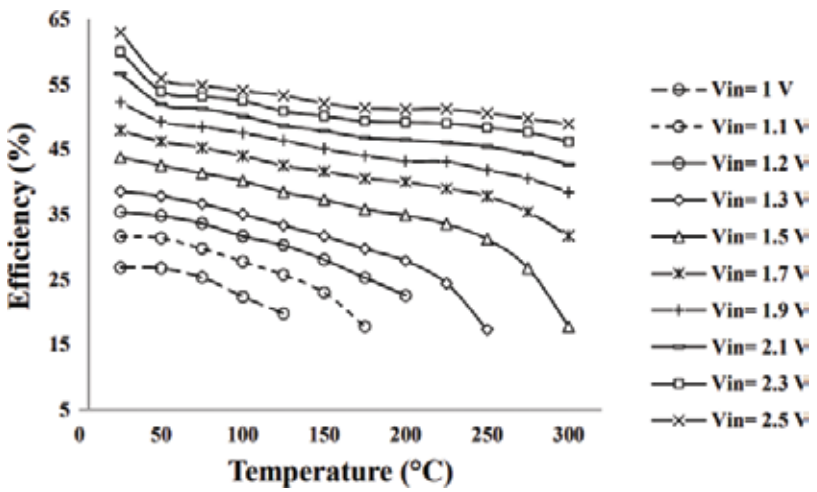

Figure 15. Efficiency of boost converter as a function of temperature.

converter supplying a 100 kΩ load. As described for the 100 kΩ converter, at higher temperatures the increased resistance of both the JFET channel and the windings within the transformer itself result in a reduction in efficiency. The SiC diode voltage drop also increases with temperature, so the overall conduction loss in the circuit increases, resulting in a decrease in the system efficiency. However, it can be seen from the data that the decrease in efficiency with increasing temperature is not as significant for the high output power circuit. As the converter output power is significantly higher, the power losses in the circuit will play a less significant role in the overall efficiency of the converter hence the converter efficiency is higher.

5. Conclusions

A novel self-starting converter technology has been described, which is suitable for powering wireless sensor nodes by means of energy harvesting from a thermal gradient. The converter was constructed from silicon carbide devices and proprietary high temperature passives to enable deployment in hostile environments, such as those found in aerospace, oil and gas and nuclear applications. The self-oscillating nature of the circuit along with high temperature capability result in reduced component count and hence a more reliable approach for powering SiC based WSNs for hostile environments. The self-oscillating nature of the circuit along with high temperature capability result in reduced component count and hence a more reliable approach for powering SiC based WSNs for hostile environments. The operation principle of the self-starting converter was detailed for two configurations which reflect low and high output current. The effect of input voltage and primary inductance on the converter operation and switching frequency was correlated with the characteristics of the components used in the circuit manufacture and the operating conditions for the circuit. Experimental measurements on a converter showed that whilst the performance of the circuit is influenced by the ambient temperature, it is possible to boost the voltage from a thermoelectric generator to a level that is suitable for the operation of high temperature circuits.

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Chapter 2

New Energy Harvesting Systems Based on New Materials

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Lipan Laurențiu Constantin

Additional information is available at the end of the chapter

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Abstract

This study starts with the ZnO nanostructured materials used for improve the efficiency of polycrystalline solar cells operation under low solar radiation conditions. The ZnO nanowires were prepared using the hydrothermal method of deposition on the seed layer by a new and complex process, with controllable morphological and optical properties. The analysis of the XRD patterns, scanning electron microscopy images (SEM) of the ZnO nanowires and a lot of tests made Pasan Meyer Burger HighLight 3 solar simulator, confirm the advantages of using the ZnO nanowires in solar cells applications for antireflection coatings. Then, piezoelectric structures based on new modified PZT zirconate titanate designed for energy harvesting applications is presented. Based on their piezoelectric characteristics, modified PZT zirconate titanate ceramics made of Pb $(Zr_{0.53}Ti_{0.47})_{0.99}Nb_{0.01}O_3$ ceramic have efficient applications in energy harvesting devices. A piezoelectric transducer, consisting of a thin plate of this piezoceramic material, with dimensions (34 mm × 14 mm × 1 mm), is illustrated. A multiphysics numerical simulation further illustrates such piezoelectric transducer operation. Finally, the miniature planar transformer with circular spiral winding and hybrid core—ferrite and magnetic nanofluid, designed for new energy harvesting systems is presented. We purpose now that the magnetic nanofluid be used both as a coolant and as part of the hybrid magnetic core.

Keywords: ZnO nanostructured materials, antireflection coatings, piezoelectric devices, energy harvesting, electric micro-transformer, planar coils, magnetic nanofluid

1. Using the ZnO nanostructured materials in order to improve the efficiency of polycrystalline solar cells operation under low solar radiation conditions

1.1. Current state regarding obtaining of the ZnO nanoparticles

ZnO is a II–VI semiconductor with direct banned band of 3.37 eV. Nanostructured ZnO is used to obtain LED's (light-emitting diode – electroluminescent diode), in the manufacture of gas sensors and photovoltaic cells, both because of its electron transport properties and anti-reflective coatings. In recent years, a number of articles have been reported to present the results obtained from studies to obtain ZnO nanoparticles. The use of the hydrothermal method for obtaining these nanostructures using water as solvent and the $Zn(NO_3)_2$ – HMTA system, at low temperatures (below 100°C), is among the processes that have begun to be used in recent years. ZnO nanoparticles are relatively easy to synthesize due to the hexagonal columnar structure of the unit cell. Once with getting the nanobelts of ZnO in 2001 [1], the research of ZnO nanostructures with different morphologies has seen rapid growth. The different methods of synthesizing these nanoparticles have been developed in recent years; they include vapor–liquid–solid techniques [2, 3], chemical vapor deposition [4], thermal evaporation [5] and hydrothermal method [6, 7]. The hydrothermal method does not involve the use of catalysts and facilitates the growth of nanoparticles on large surfaces. The increase in the gaseous phase can be achieved using one of the following methods: chemical deposition of metal–organic vapors (MOCVD) [8, 9], chemical transport from vapor [10, 11] and deposition by laser ablation [12]. With these methods, high-quality nanoparticles of micron size [13, 14] can be obtained. The process presents a number of disadvantages: it requires a temperature of 450–900°C, a series of limitations related to the substrate are imposed like morphology and its area [15]. In contrast, growth from the solution is a process that takes place at temperatures below 100°C, [16, 17], and the advantage of this process is to obtain nanoparticles with optical and electrical properties necessary for their use in the field of photovoltaic cells (antireflection coatings, electrode transparent, etc.).

1.2. Preparation of antireflective coating based on ZnO nanoparticles for application on the substrate

Anti-reflection technology plays an important role in the fabrication of high-efficiency solar cells by increasing light coupling into the active region of devices. A complex process is used for obtaining ZnO nanostructures for antireflective coatings. The process is suitable to silicone solar cells and can be used in order to increase their efficiency under low solar radiation, allowing the control of the morphological and optical properties of ZnO nanostructures deposited on glass through ZnO seed layer deposition process. The ZnO nanowires were prepared using the hydrothermal method of deposition on the seed layer by a new and complex process, [18]. To obtain the ZnO nanoparticles, two steps are required: obtaining the ZnO seed layer (on which ZnO nanoparticles are formed) and a second stage consisting of the actual growth of ZnO nanoparticles. ZnO seeded layers were prepared using a solution of zinc acetate dissolved in 1-propanol. Zinc decomposition or hydrolysis to obtain ZnO nanocrystals are a method often used [19–21]. Subsequent decomposition of zinc acetate at temperatures between 100°C − 280°C leads to the formation of $Zn_4O(CH_3CO_2)_6$, which eventually breaks

down into ZnO. During the process of obtaining a ZnO by this method a series of gaseous products are released: water (H_2O), carbon dioxide (CO_2), acetone ($(CH_3)_2CO$) and acetic acid (CH_3COOH). These products are eliminated around the temperature of 270°C ((1)–(4)). As the temperature increases, ZnO nanoparticles are formed following chemical reactions:

$$Zn(CH_3COO)_2.2H_2O \rightarrow Zn(CH_3COO)_2 + 2H_2O \quad (1)$$

$$4Zn(CH_3COO)_2 + 2H_2O \rightarrow Zn_4O(CH_3COO)_6 + 2CH_3COOH \quad (2)$$

$$Zn_4O(CH_3COO)_6 + 3H_2O \rightarrow 4ZnO + 6CH_3COOH \quad (3)$$

$$Zn_4O(CH_3COO)_6 \rightarrow 4ZnO + 3CH_3COCH_3 + 3CO_2 \quad (4)$$

Thus, thermal dehydration of zinc acetate can be considered a process of dehydration, vaporization/decomposition and ZnO formation [22]. Synthesis of ZnO nanowires by the hydrothermal method on the deposited substrate by the dehydratated zinc acetate process, involves the reactions:

$$HMTA + 6H_2O \leftrightarrow 4NH_3 + 6HCHO \quad (5)$$

$$NH_3 + H_2O \leftrightarrow NH_4^+ + OH^- \quad (6)$$

$$Zn^{2+} + 4NH_3 \leftrightarrow \left[Zn(HN_3)_4\right]^{2+} \quad (7)$$

$$Zn^{2+} + OH^- \leftrightarrow Zn(OH)_2 \quad (8)$$

$$Zn(OH)_2 \leftrightarrow ZnO + H_2O \quad (9)$$

HMTA hydrolyzes readily in water to form formic aldehyde (HCHO) and ammonia (NH_3), releasing energy, which is associated with its molecular structure, as can be seen in reactions (5) and (7). This stage is critical in the process of increasing ZnO nanowires. If HMTA hydrolyses very quickly, it produces a very large amount of OH^- ions—in a very short time, Zn^{2+} ions from the solution would precipitate quickly due to the basic pH, and this would lead to rapid consumption of precursors and to an inhibition of the growth of ZnO nanoparticles [23]. From reactions (8) and (9), NH_3 which originates from hydrolysis HMTA has two essential roles. Firstly it produces the basic medium required for the formation of $Zn(OH)_2$. Secondly, it coordinates the Zn^{2+} ions and thus stabilizes the aqueous solution. $Zn(OH)_2$ is dehydrated when heated by ultrasonication or even under the sunlight. All five reactions (5), (6), (7), (8) and (9) are in equilibrium and can be controlled by adjusting the reaction parameters: precursor concentration, temperature and growth time, which may have a positive or negative influence on the balance of reactions. Thus, precursor concentration determines the nanoparticle density, temperature and growth time controls. It also controls the morphology and nanoparticle size ratio. In reaction (5) it can be seen that seven moles of reactants produce ten moles of reaction products, which means an increase in entropy during the reaction, resulting an increase of the temperature, and finally the result is the shift of equilibrium to the reaction products. The rate of hydrolysis of HMTA increases with the increase of the basicity of the environment and vice versa. Also, the five reactions continue at room temperature but at a very low speed. For example, the solution with a precursor concentration of less than 10 mmol/L remains transparent and clear at room temperature for several months. If microwaves are used

as a source of heating, the reactions take place at a very high speed, with a nanofire growth rate of up to 100 nm/min [24].

1.3. The analysis of ZnO seed layer and ZnO nanowires growth by the hydrothermal method

The X-ray diffraction analysis was performed for the ZnO seed layer as well as for the ZnO nanowires growth by the hydrothermal method as shown within **Figures 1** and **2** respectively. The structural analysis of the ZnO nanoparticles was performed, by grazing incident X-ray diffraction using an X-ray diffractometer (Bruker AXS D8 Discover) with Cu and Kα irradiation, 40 kV/40 mA, 20–60°, 2 Theta domain, 2 seconds/step scan speed and 0.04° step. In the case of the ZnO seed layer, there were identified only the specific peaks of ZnO, confirming the higher purity of the film. ZnO from seed layer presented *wurtzite* hexagonal structure *P63mc* as well as structure parameters $a = b = 3.242$ nm and $c = 5.176$ nm. The intensity of the diffraction peaks corresponding to (002) and (110) plans displayed low broad peaks in the case of all the analyzed seed layer samples. The *XRD* analysis showed wurtzite hexagonal structure *P63mc* and structure parameters $a = b = 3.242$ nm and $c = 5.176$ nm when also considering the nanowires. The diffraction pattern highlighted peaks associated to (100), (002), (101) and (102) plans and the correspondence of ZnO. The (002) plan displayed a higher intensity peak in comparison to the corresponding plans (100), (101) and (102), indicating that the ZnO nanowires are predominantly c-axis orientated. Other peaks were not observed, leading to the fact that no other structures besides ZnO were formed. It was confirmed that high purity ZnO is obtained.

A different number of depositions (spray pyrolysis and spin coating) were achieved in order to determine the optimal thickness and morphology of the ZnO seed layer. The optimal seed

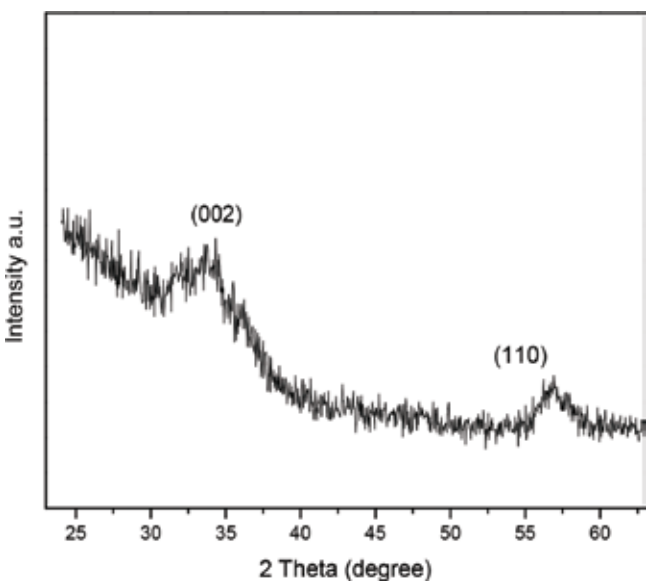

Figure 1. XRD analysis of ZnO seed layer.

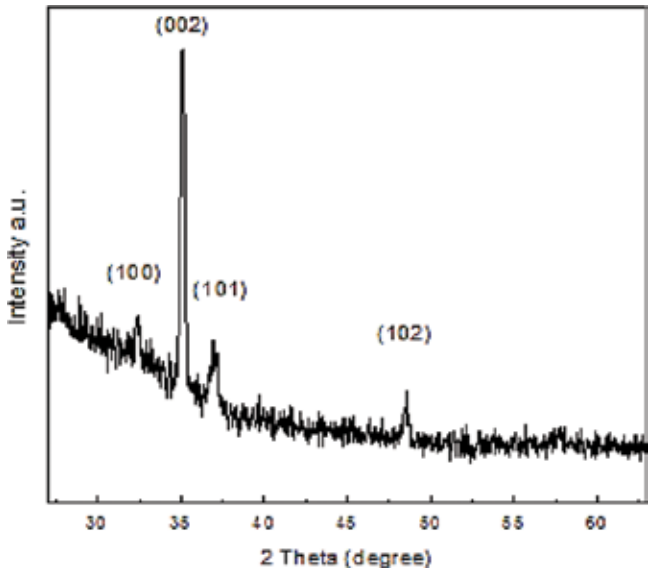

Figure 2. XRD analysis of ZnO nanowires growth by the hydrothermal method [18].

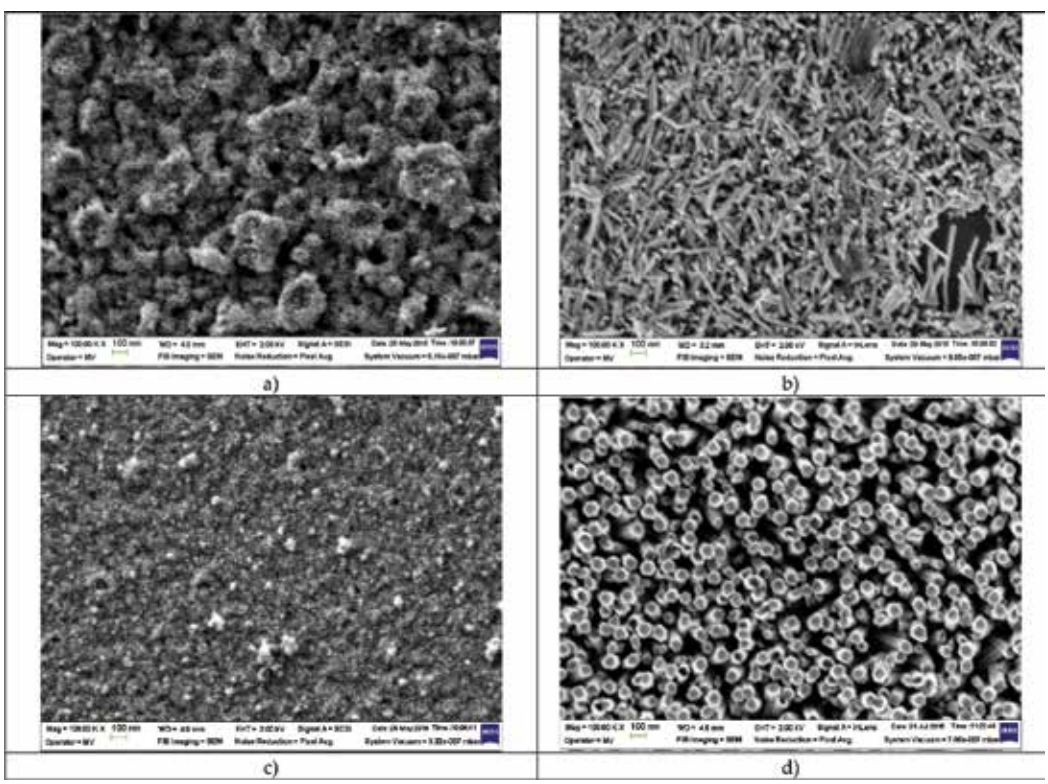

Figure 3. Scanning electron microscopy (SEM) images of the ZnO seed layer (a) and (c) as well as SEM images of ZnO nanowires (b) and (d) respectively [18] (100 kx magnification).

layer was obtained by three application stages of spray pyrolysis at a temperature of 100°C, three stages of spin coating followed by treatment at 300°C for a period of 30 minutes.

The microscopy micrographs shown within **Figure 3** were recorded by using a field scanning electron microscope or by employing the annular in-lens detector for a second set of electron images with magnification of 100.000 X and an accelerating voltage of 2000 V. The surface morphology and structure of the nanoparticles were examined by employing a scanning electron microscope (FESEM, Carl Zeiss Auriga) at an accelerating voltage of 2.00 kV. The imaging was performed at a high magnification of 100 kx while the optical transmission and reflection spectra was recorded in the wavelength range of 400–800 nm by using a double beam UV–Vis–NIR spectrophotometer (UV–VIS Spectrophotometer 570 Jasco). The morphology of the ZnO seed layer surface influences the morphology of the ZnO nanowire. These layers operate as seed crystals in order to ensure the epitaxial growth of ZnO nanowires. In the case of thicker films, ZnO clusters are observed (grains with dimensions larger than 100 nm) consisting of agglomerations that influence the nanowires growth by a reduced order, scattered across the surface and random orientated (**Figure 3a** and **b**). The morphology and growth of the zinc oxide nanowires are influenced by the thickness and geometry of the seed layer (uniform grain, 30–55 nm) (as seen from **Figure 3c** and **d**). In this case, due to the seed layer uniformity and lack of agglomerations, the nanowires growth was orientated, with homogenous dimensions as well as displayed on the entire substrate surface. In this case, there was obtained a perfectly balanced seed layer and also a homogenous nanowire growth with lengths of ~200 nm and 50 nm diameter. Besides the high density of the ZnO nanowire arrays, other nanostructures are not observed.

The resulting seed layer presented suitable growth proprieties by the hydrothermal method of uniform and vertical ZnO nanowires. The variation of the optical transmission is shown within **Figure 4**, with wavelength found in the range of λ = 400–800 nm for glass, ZnO seed layer and ZnO nanowires. The ZnO seed layer has presented a good transparency of approximately 80%, similar to the glass value due to the reduced thickness (50 nm) and surface uniformity. The

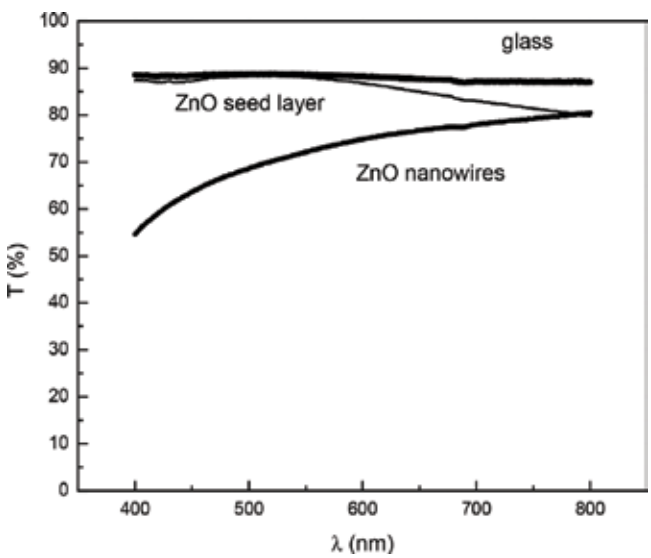

Figure 4. Optical transmission of glass, ZnO seed layer and ZnO nanowires film.

samples of ZnO nanowires present a good transparency in the visible range (400–800 nm), with a lower average value of 76% (approximately 5% lower than in the case of glass). This decrease is due to the fact that the transmitted radiation by light diffusion increases the occurrence of the light scattering phenomenon of the ZnO nanowires.

Following the spectrophotometric analysis, the variation of the optical reflection with wavelength in the range of 400–800 nm is presented in **Figure 5**. The graph confirms that the reflection is reduced in comparison to the values obtained for simple glass. The ZnO seed layer presents an intermediate value between glass and ZnO nanowires, with an average of 11%. The average value of ZnO nanowires sample for the visible optical reflection is equal to 9%, with 5% lower than the simple glass. By summarizing these optical characteristics, it is concluded that the ZnO nanowire films can be considered as a solution to the antireflective coatings in the solar cells field due to the optical proprieties and low-price manufacturing.

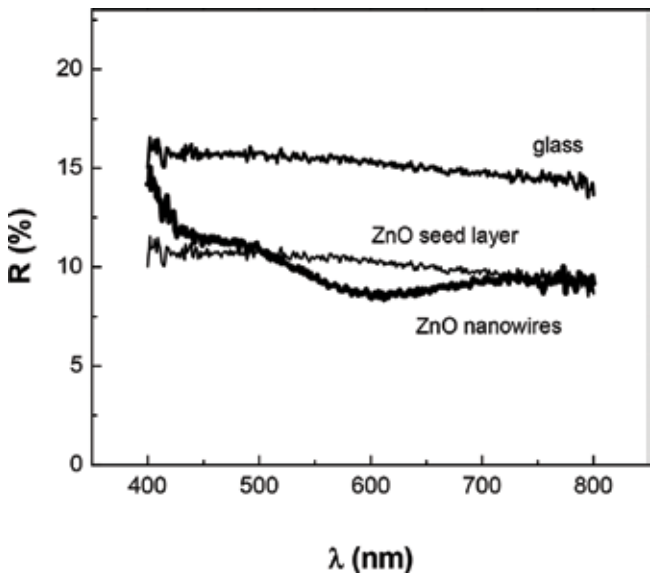

Figure 5. Optical reflection of glass, ZnO seed layer and ZnO nanowires film.

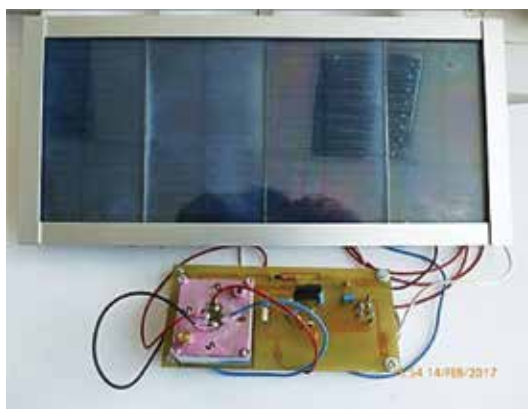

Figure 6. The modular photovoltaic conversion system, connected to the DC/DC converter with isolation.

1.4. Prototyping and testing the modular photovoltaic conversion system

Modular photovoltaic conversion system, designed for energy harvesting applications has been achieved, using four photovoltaic cells, **Figure 6**. A commercial polycrystalline silicone solar cell manufactured by Conrad Electronic SE was selected and covered by a nanostructured ZnO disposed on glass in order to be tested. The technical data related to the considered polycrystalline solar panel (123 cm^2) consist of 1.35 W output power, 9 V nominal voltage, 10.5 V open circuit voltage and 150 mA short-circuit current. The determination of the solar

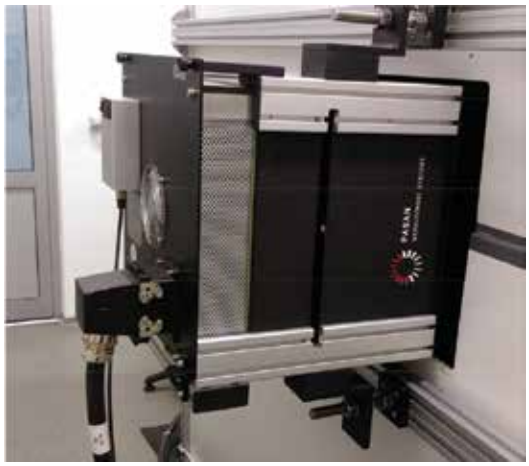

Figure 7. Pasan Meyer Burger HighLight 3 solar simulator, used to test of the modular photovoltaic conversion system, view from flash box.

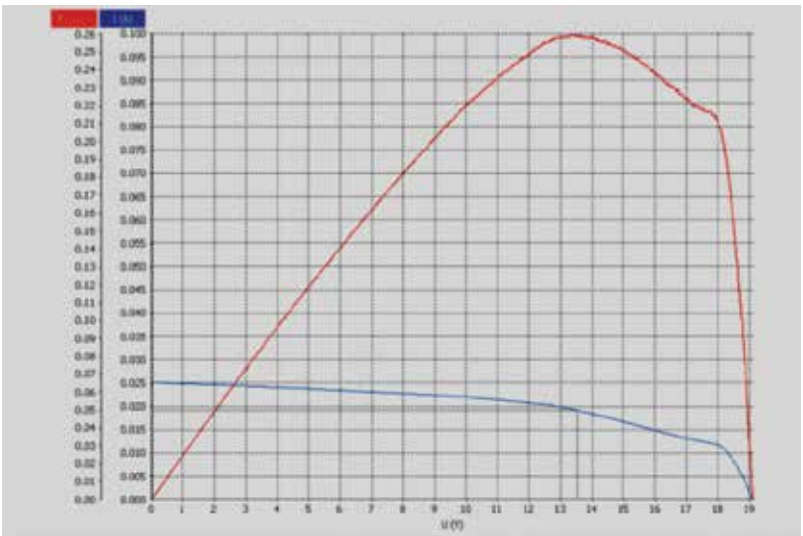

Figure 8. Tested of the photovoltaic module covered by a nanostructured ZnO disposed on glass, for 100 W/m^2 test conditions.

cells functional parameters (efficiency, short circuit current, open circuit voltage and output power) has led to the conclusion that all the values are superior in the case of the solar cells with ZnO nanowires on glass showing that the performance of the solar cell depends on the irradiance and antireflective coating.

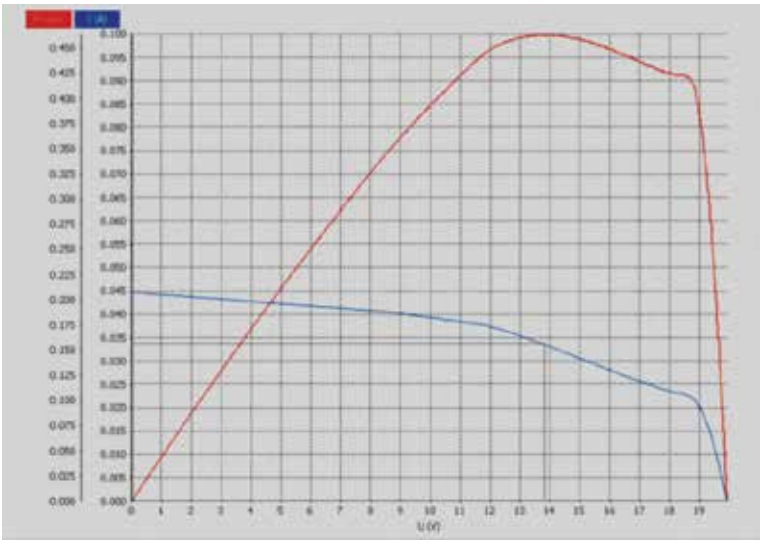

Figure 9. Tested of the photovoltaic module covered by a nanostructured ZnO disposed on glass, for 200 W/m^2 test conditions.

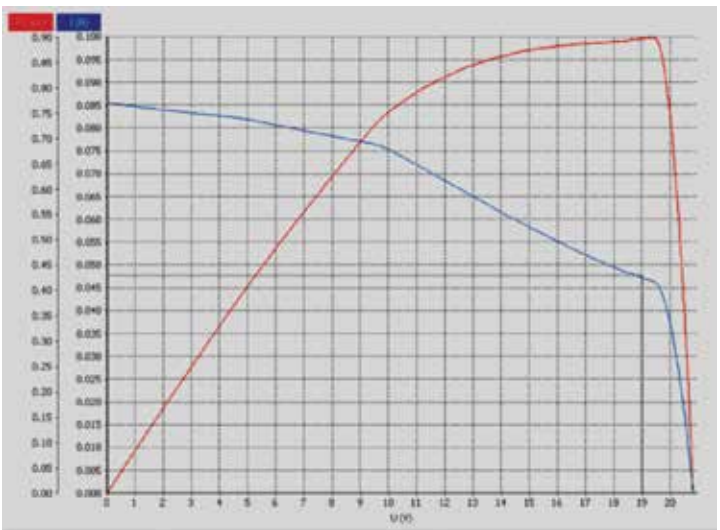

Figure 10. Tested of the photovoltaic module covered by a nanostructured ZnO disposed on glass, for 400 W/m^2 test conditions.

The photovoltaic module was tested for standard test conditions (1000 W/m^2, 25°C, AM 1.5) as well as for reduced solar irradiance by using the Pasan Meyer Burger HighLight 3 solar simulator shown in **Figure 7**. There were used four masks for the solar irradiance attenuation (100 W/m^2, 200 W/m^2, 400 W/m^2 and 700 W/m^2) in order to achieve the comparison between the generated powers along with varying the operation conditions. The used simulator is able

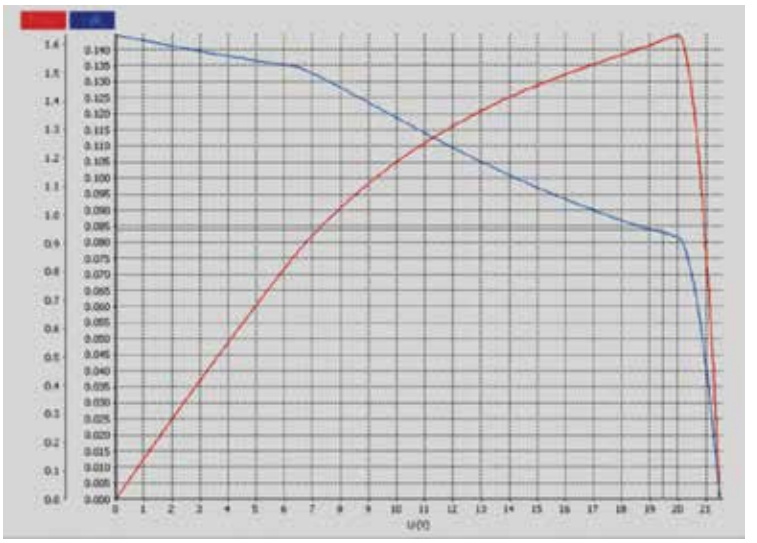

Figure 11. Tested of the photovoltaic module covered by a nanostructured ZnO disposed on glass, for 700 W/m^2 test conditions.

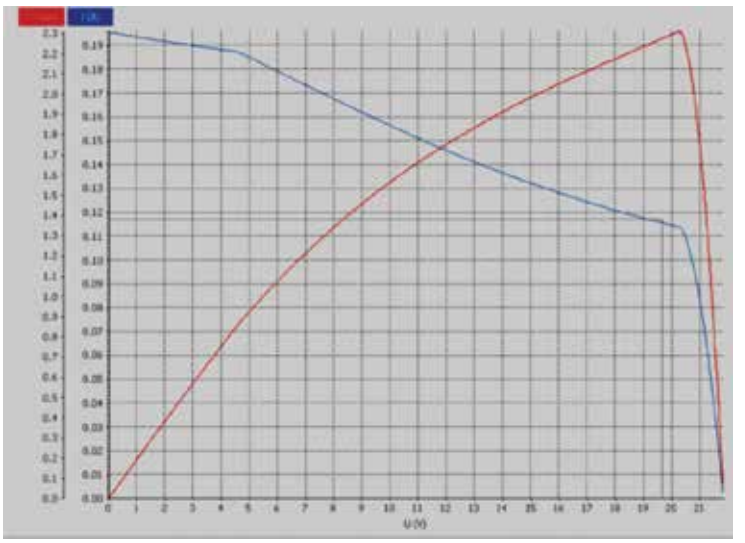

Figure 12. Tested of the photovoltaic module covered by a nanostructured ZnO disposed on glass, for standard test conditions, 1000 W/m^2.

to adjust the irradiance value between 100 W/m^2 and 1000 W/m^2, with both the light uniformity and light stability below 1%. Accordingly, five characteristics resulted for each of the tested modules for these various operating conditions, **Figures 8**, **9**, **10**, **11** and **12**.

The results confirm the advantages of using the ZnO nanowires in solar cells applications for antireflection coatings.

2. Piezoelectric structures based on new modified PZT zirconate titanate designed for energy harvesting applications

We propose a piezoelectric ceramic material what can it be integrated into piezoelectric structures for energy harvesting applications. The piezoceramic element has the shape of a disk with diameter of 12 mm while the width is 0.3 mm. On each of the ceramic disk's sides, silver

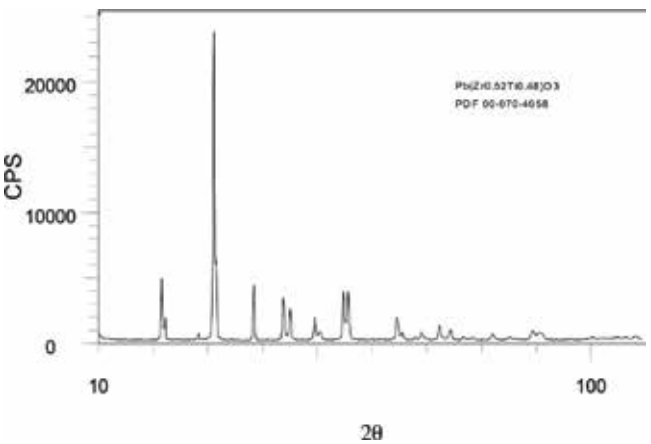

Figure 13. XRD pattern of PZT doped with 1% Nb_2O_5 sintered at 1120°C for 2 hours, [25].

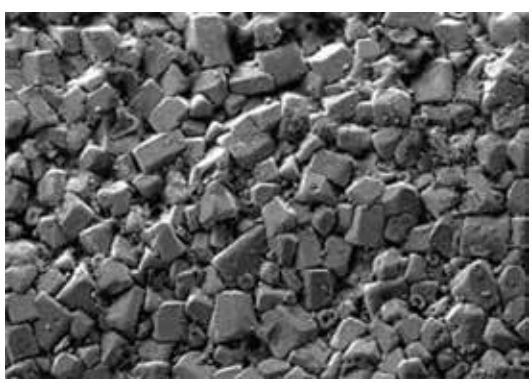

Figure 14. Scanning electron microscopy images (SEM) image of PZT doped with 1% Nb_2O_5. Sintered at 1120°C for 2 hours [25].

electrodes were attached. Perovskite ceramics based on lead zirconate titanate (PZT) modified with niobium (Nb) were used to obtain these active elements. A high temperature solid state reactions technique has been used to prepare the piezoelectric ceramic, [25, 26], described by the general formula $Pb(Zr_{0.53}Ti_{0.47})_{0.99}Nb_{0.01}O_3$. Based on their piezoelectric characteristics, modified PZT zirconate titanate ceramics have efficient applications in energy harvesting devices. The X-ray diffraction patterns of $Pb(Zr_{0.53}Ti_{0.47})_{0.99}Nb_{0.01}O_3$ ceramic are shown in **Figure 13**. The XRD results indicate the rovskite type tetragonal phase free from a pyrochlore phase. The SEM pattern of the same composition sample is shown in **Figure 14** and it shows that the microstructure of our sample is very dense.

Figure 15. The low energy source built with piezoelectric linear transducers system, INCDIE ICPE-CA concept [26].

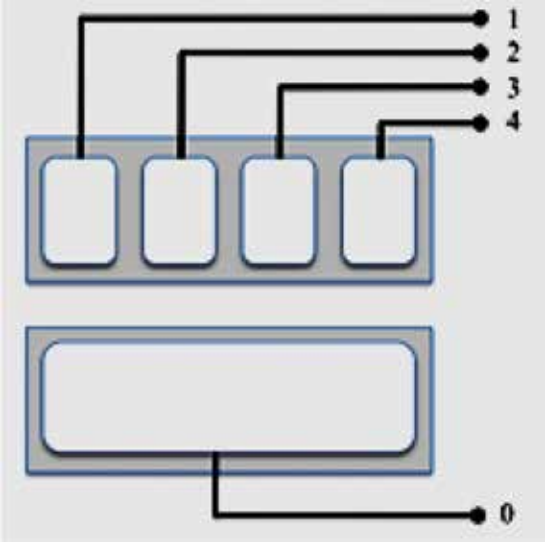

Figure 16. The electrical circuit of the generator [26].

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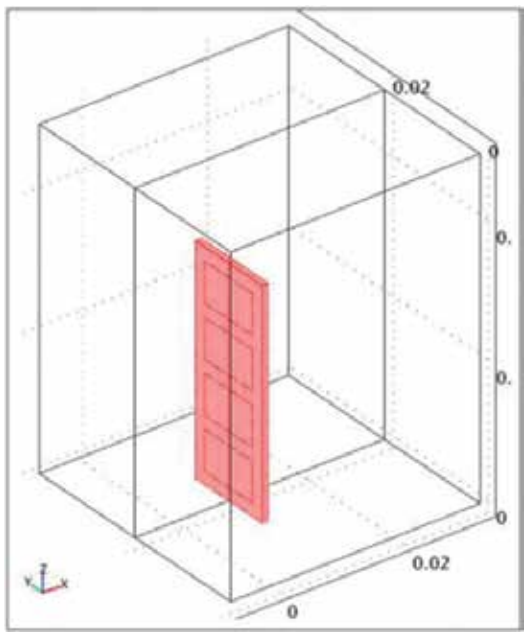

Figure 17. Computational domain for the flow problem (the plate is placed in a flow duct, as in a hydrodynamic test setting) (concept ECEE-UPB) [26].

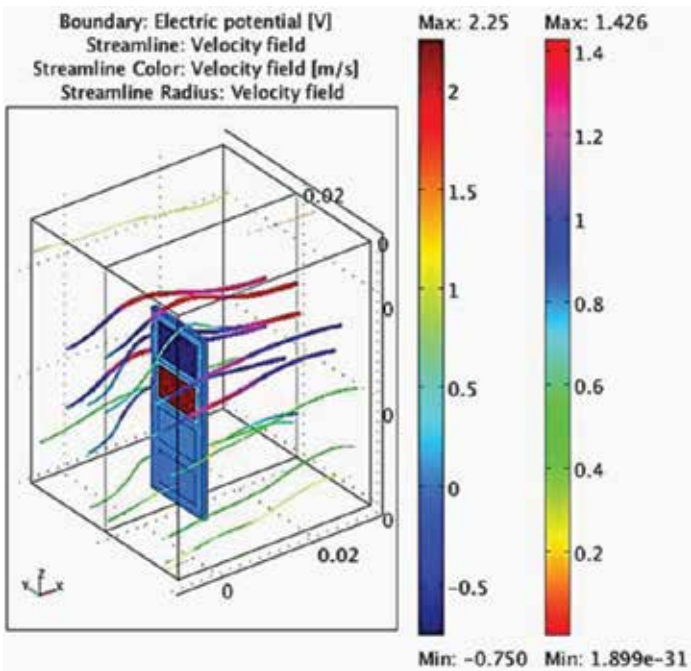

Figure 18. Solutions of the multiphysics problem: Fluid streamlines and electric potential color map on the surface of the plate (concept ECEE-UPB) [26].

A simple structure is analyzed in [25], by numerical simulation for the demonstration of its capacity to generate electric voltage under mechanical stress.

Another piezoelectric transducer, consisting of a thin plate of piezoceramic material with dimensions (34 mm × 14 mm × 1 mm), is illustrated in **Figure 15**. A layer of conductive material is deposited on one side of the plate (see the lower picture in **Figure 15**) and four equal rectangular conductive areas are deposited on the other side (see the upper picture in **Figure 15**), [26]. If the plate is subjected to pressure and mechanical deformation, due to exposure to wind or being placed in a fluid flow, the piezoelectric material will be polarized and a non-uniform electrical potential distribution could be identified on the faces of the plate. Conductive surfaces behave like surface electrodes attached to the plate; they integrate the electric potential on the plate's surface and connect to an electric circuit, transferring the potential value of each plate to an output connector, **Figure 16**. The one face which is uniformly coated can be used for reference terminal (ground), while each of the four rectangular patches can be connected to an individual electrode (1, 2, 3, 4), **Figure 16**. If the deformation of the ceramic plate is not uniform (the case of a flexible material), the electrodes might take different potential values and the piezoceramic plate becomes an electrical generator with four different output voltages: U_{10}, U_{20}, U_{30}, U_{40}, **Figure 16**. If the plate is rigid and the deformations are identical, the four terminals provide equal output voltages, [26].

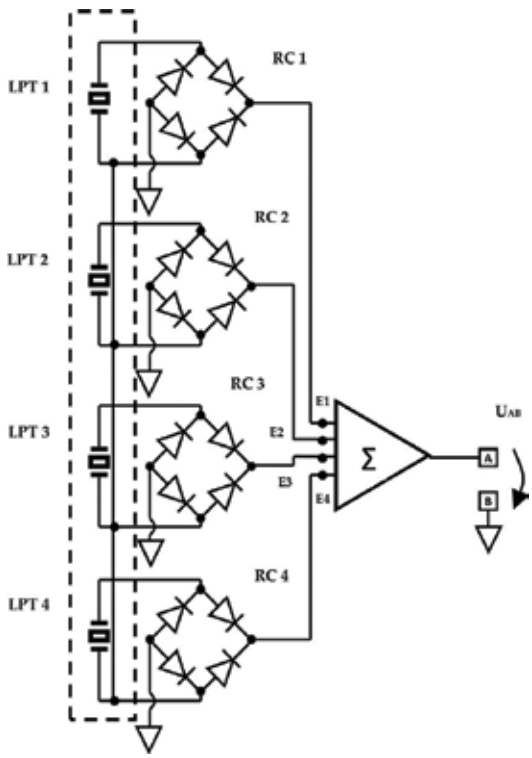

Figure 19. Interfacing of the low energy source built with piezoelectric linear transducers system [26].

A multiphysics numerical simulation further illustrates such piezoelectric transducer operation. The numerical model was built and analyzed with Comsol Multiphysics [38], a technical software package based on the finite element method, which allows the coupling of different software modules specialized in modeling physical problems of different nature. An image of the solution of this analysis is presented in **Figures 17** and **18**.

Often, due to the complexity of the mathematical model, the analytical solutions of the differential equations system are difficult to obtained. Thus, it is necessary to use the numerical simulations method still from the design phase.

Interfacing of the low energy source built with piezoelectric linear transducers system is achieved through four bridges, as shown in **Figure 19**.

3. Miniature planar transformer with circular spiral winding and hybrid core—ferrite and magnetic nanofluid designed for new energy harvesting systems

One of the novelties of the future harvesting devices is regarding the use of a magnetic liquid core micro-transformer for the DC-DC converter of the harvesting device. From the operating point of view, by replacing the solid core with a hybrid core—ferrite and magnetic nanofluid, we estimate to result in a better heat dissipation and a reduction the thermal stresses in the micro-transformer leading to a longer life cycle of the device, maintaining or even improving the electric characteristics. Also, the dielectric properties of the micro-transformer will be improved.

3.1. Making a planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid: V1 by using LIGA technology (Litographie, Galvanoformung, Abformung) and precision micromachining

Energy harvesting is a relatively new research area, seen as a viable and affordable solution for powering small autonomous devices, such as wireless sensor networks. Energy harvesting devices use small scale parts with low power losses. The main components are the electrical transformers that convert the voltage/current parameters from the primary from the energy harvesting stage, to the secondary to energy storage and distribution level stage. Miniature construction of the transformers, whose implementation can benefit from the LIGA manufacturing technology (Litographie, Galvanoformung, Abformung or in English Lithography, Electroplating and Molding), are required for compact, small but energy-efficient solutions. The following steps are performed to manufacture a planar microtransformer with circular spiral windings and with hybrid core—ferrite and colloidal magnetic nanofluid—V1:

A. ***Manufacture of the planar micro-coils***:

- the ceramic substrate preparation, 1, as well as surface preparation, (**Figure 20a**) and depositing conductive uniform submicrometer layer, 3;
- spin deposition (coat) of a uniform layer, 2, SU8 photoresist, (**Figure 20a**). The thickness of this layer will be slightly above the height of turns to be deposited;

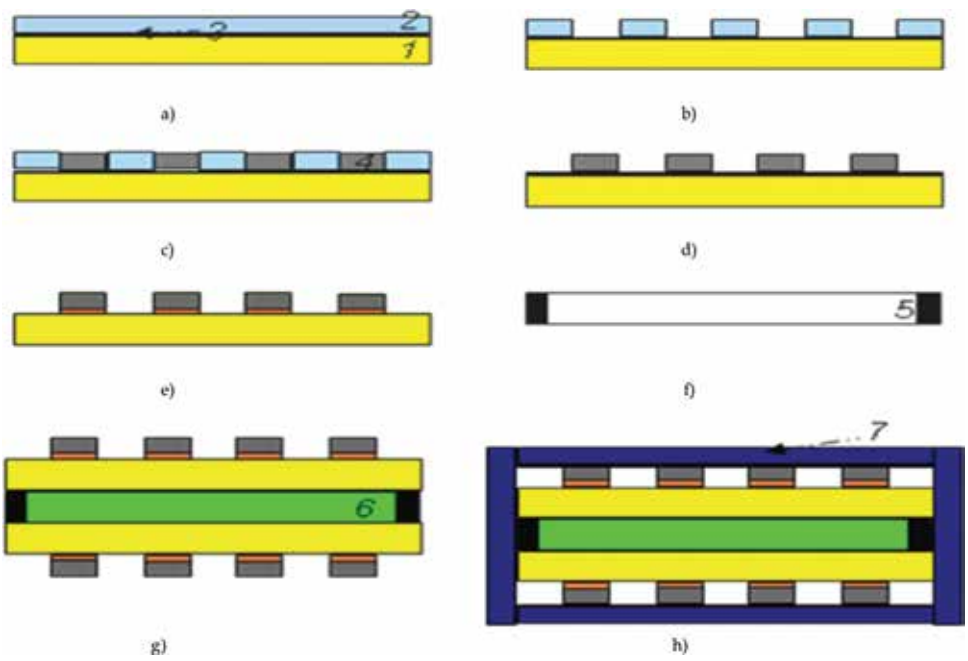

Figure 20. Manufacture of a planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid—V1.

- pre-exposure bake (soft bake) at 95°C;
- exposure to UV radiation by direct writing lithography using DWL66 equipment;
- post-expose bake at 65°C and 95°C, with controlled ramp;
- relax and develop structures using 1-methoxy-2-propyl acetate (mr-DEV600), (**Figure 20b**);
- dry, hard bake;
- high purity copper galvanic deposition, 4, with controlled thickness (**Figure 20c**);
- SU8 photoresist exposed remove using free radical reaction with STP2020/R3T equipment (**Figure 20d**);
- controlled corrosion (remove) submicrometer layer to separate planar microcoils (**Figure 20e**);
- integrity coils checking.

B. *Manufacture of another parts*:

- precision micromachining by CNC machine (KERN Micro) by laser ablation CompexPro/Coherent and by electrodischarge machine on SmartDEM/Kunth: separation and sealing element, 5, (**Figure 20f**) and ferrite clad, 7, (**Figure 20h**).

C. ***The assembling***:

- aligning the plates with micro-coils (two) by means of the separation and seal element, 5, (**Figure 20g**);
- undismantled adhesion assembly (bonding);
- introducing a magnetic nanofluid, 6, (**Figure 20g**), in the cavity and sealing the nozzle access;
- mounting plate ferrite isolated from coils and making of electrical connections.

3.2. Making a miniature planar microtransformer with circular spiral windings obtained by machining, starting from a textolit board double plated with copper and with hybrid core—ferrite and colloidal magnetic nanofluid

3.2.1. Making a miniature planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid: V2

A key component of the devices used for energy harvesting from the environment is the electric transformer. In this case, we proposed a miniature planar transformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid, [27]. The proposed model has two circular spiral-wound, made from copper: 20 turns in primary and 40 turns in secondary. Windings, **Figures 21** and **22**, can be "grown" using LIGA technology on a ceramic substrate (Al_2O_3) as has been shown previously or can be obtained by machining, starting from a textolit board double plated with copper. Housing and central column are made of 3F3 ferrite. The cavity formed in the housing is filled with superparamagnetic colloidal nanofluid, NMF-UTR40-500G, **Figure 21**, having saturation magnetization of 500 Gs, [27]. The applications presented in [28, 29], uses a dilution of magnetic nanofluid acting also as a cooling agent, type NMF-UTR40-50G that having saturation magnetization of 50 Gs.

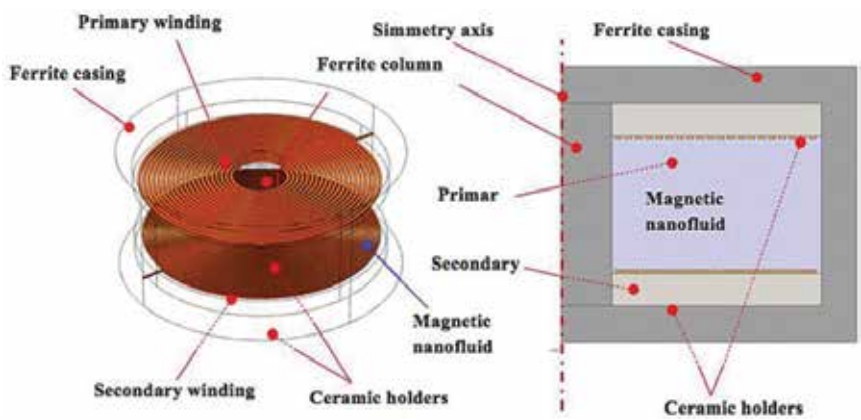

Figure 21. The planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid—V2 and the equivalent simplified 2D axial model [30].

Figure 22. Planar coils corresponding to primary and secondary coils of the microtransformer, INCDIE ICPE-CA concept.

We purpose now that the magnetic nanofluid be used both as a coolant and as part of the hybrid magnetic core, by using of the magnetic nanofluid type NMF-UTR40-500G.

3.2.1.1. The mathematical model

The magnetic field inside the planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid—V2 for steady state conditions is described by the (10), (11), (12) and (13) equations as follows: inside the coils ($\mathbf{J} \neq 0$), the ferrite part of the magnetic core ($\mathbf{J} = 0$), and within the ceramic holders ($\mathbf{J} = 0$).

$$\nabla \times \left(\mu_0^{-1}\mu_r^{-1}\nabla \times \mathbf{A}\right) = \mathbf{J}, \tag{10}$$

inside the magnetic nanofluid (*MNF) core.*

$$\nabla \times \left(\mu_0^{-1}\nabla \times \mathbf{A} - \mathbf{M}\right) = 0, \tag{11}$$

where **A** [T·m] is the magnetic vector potential, **J** [A/m^2] is the electric current density, $\mu_0 = 4\pi \times 10^{-7}$ H/m is the magnetic permeability of the free space, μ_r is the relative magnetic permeability, and **M** [A/m] is the magnetization of the MNF, approximated here through, $\mathbf{M} = \alpha \arctan(\beta \mathbf{H})$, where **H** [A/m] is the magnetic field strength, and α, β are empiric constants selected to accurately fit the magnetization curve. The problem is closed by magnetic insulation boundary conditions, $\mathbf{n} \times \mathbf{A} = 0$, where **n** is the outward pointing normal, [30–32].

The magnetic field, produced by the electric currents, generates magnetic body forces within the MNF, which are responsible for the flow of the fluid part of the core described, in steady state conditions, through.
momentum conservation (*Navier–Stokes*)

$$\rho(\mathbf{u} \cdot \nabla)\mathbf{u} = -\nabla \times \left[p\mathbf{I} + \eta\nabla\mathbf{u} + (\nabla\mathbf{u})^T\right] + \mathbf{f}_{mg}, \tag{12}$$

mass conservation law

$$\nabla \cdot \mathbf{u} = 0, \tag{13}$$

where, $\mathbf{u}$ [m/s^2] is the velocity, p [N/m^2] is the pressure, ρ [kg/m^3] is the mass density, η [N·s/m^2] is the dynamic viscosity, and $\mathbf{f}_{mg} = \mu(\mathbf{M} \cdot \nabla)\mathbf{H}$ [N/m^3] is the magnetization body force. Body forces of thermal nature are not significant here [30–32]. No slip (zero velocity) conditions on the outer boundaries of the MNF core close the flow problem.

3.2.1.2. The practical achievements

In **Figure 23**, the 3F3 ferrite parts of magnetic circuit can be seen and in **Figure 24** the ferrite magnetic circuit and microtransformer housing. Parts of the housing, the ferrite magnetic circuit and the four planar coils which form the primary and the secondary circuit of the microtransformer it can be seen in **Figure 25**. Finally, two assembled planar microtransformers are represented in **Figure 26**.

Figure 23. The 3F3 ferrite parts of magnetic circuit.

Figure 24. The ferrite magnetic circuit and microtransformer housing.

Figure 25. Parts of the housing, the ferrite magnetic circuit and the four planar coils which form the primary and the secondary circuit of the microtransformer, INCDIE ICPE-CA concept [33].

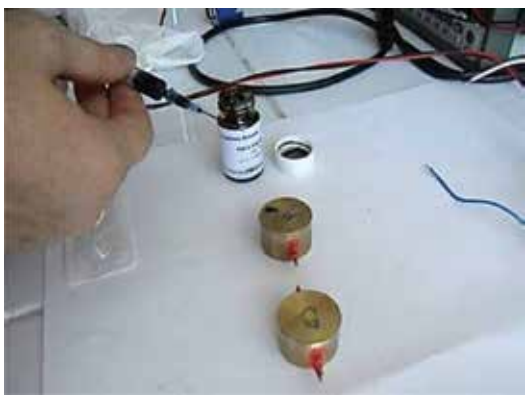

Figure 26. Two assembled planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid—V2, after the magnetic nanofluid loading process.

3.2.1.3. Analysis of 3F3 ferrite as part of magnetic circuit

Analysis of 3F3 ferrite done by scanning electron microscopy (SEM) coupled with energy dispersive micro-probe X-ray under the following conditions:

The two areas of interest were at an increase of 5000× and 2000×, **Figures 27** and **29**;

- Acquisitions have been made with the help of the secondary electron detector in the sample chamber, type "Everhart – Thornley", coupled with "INCA Energy 250" energy dispersive microprobe produced by Oxford Instruments;
- Two categories of spectra were achieved, namely: punctual, with the elemental distribution of the electron beam spot on the surface of the sample and another as micro-area, integrated where the composition of the elements of the microarray was determined quantitatively;

- Spectral analysis is multipoint type because the spectra were superimposed to see the intensity and variation of the elements in the selected points/areas;
- All the spectra were normalized to 100%. The unit was expressed in the concentration of the elements of interest was the percentage by mass (weight percent%).

After analysis, the following features were noted:

- Elements that were highlighted were C, O, Mn, Fe and Zn, **Tables 1** and **2** and **Figure 28** for Spectrum 1;

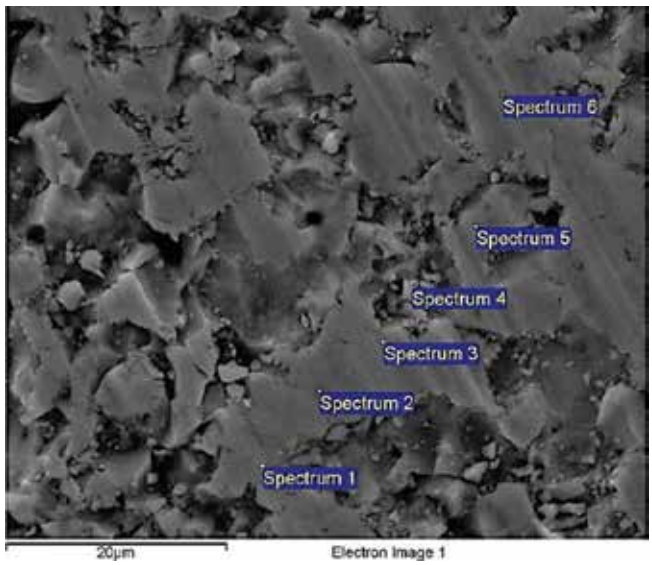

Figure 27. Scanning electron microscopy image (SEM) of the 3F3 ferrite, 5000× magnification.

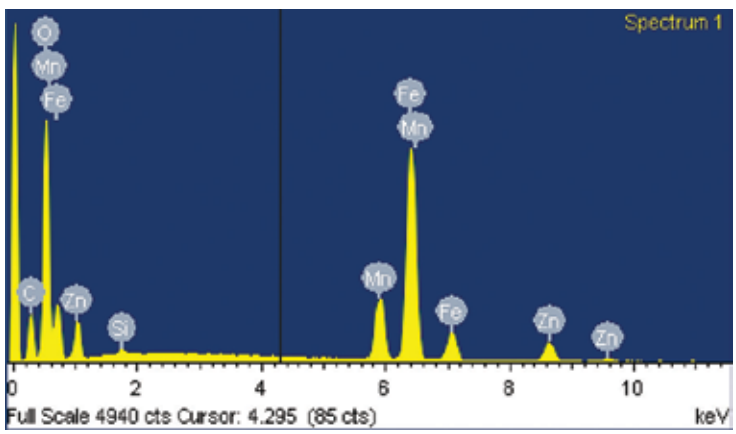

Figure 28. The 3F3 spectra analyze, corresponding to Spectrum 1 and 5000× magnification.

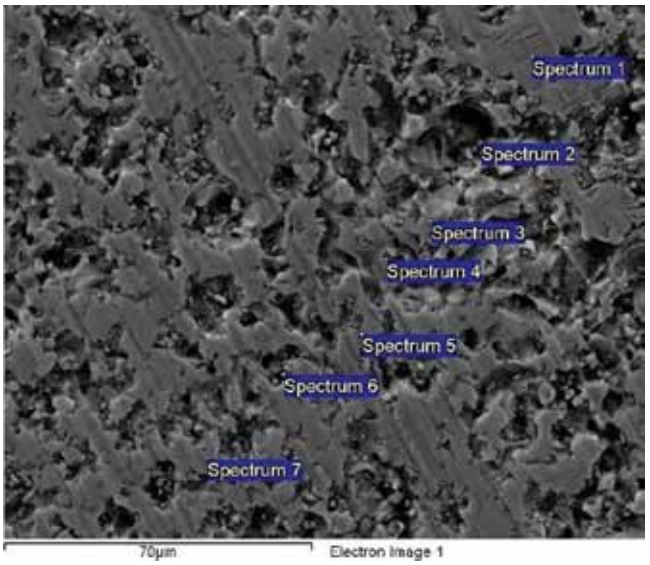

Figure 29. Scanning electron microscopy image (SEM) of the 3F3 ferrite, 2000× magnification.

Processing option: all elements analysed (normalised); all results in weight%							
Spectrum	In stats.	C	O	Mn	Fe	Zn	Total %
Spectrum 1	Yes	25.46	22.63	9.14	35.20	7.57	100.00
Spectrum 2	Yes	21.64	27.47	8.73	35.16	7.00	100.00
Spectrum 3	Yes	12.80	24.98	10.93	42.17	9.13	100.00
Spectrum 4	Yes	19.72	28.91	8.77	34.95	7.65	100.00
Spectrum 5	Yes	16.97	26.78	9.80	37.90	8.55	100.00
Spectrum 6	Yes	15.95	27.84	9.71	38.17	8.33	100.00
Mean		18.76	26.44	9.51	37.26	8.04	100.00
Std. deviation		4.49	2.28	0.83	2.80	0.77	
Max.		25.46	28.91	10.93	42.17	9.13	
Min.		12.80	22.63	8.73	34.95	7.00	

Table 1. Normalized values of elements obtained from spectral analysis of ferrite 3F3, corresponding to Spectrum 1–6, 5000× magnification.

- The presence of oxygen in percent more than 20% indicates that the sample contains oxides with various chemical combinations. The compositional distribution of the highlighted elements is relatively uniform, variations being probably due to the surface geometry of the sample (roughness of hundreds of nm) or to a non-uniform distribution of the carbon matrix (**Figure 29**);
- SEM micrographs have revealed a relatively uniform surface in terms of morphology, but which has a roughness due to the technological methods of obtaining the samples (of the

intrinsic material) or the mechanical processing methods used to obtain the investigated piece;

- It is also observed the presence of some impurities on the surface of investigated samples such as Al, Si and Ca elements, **Table 2** and **Figure 30** for Spectrum 1, but in very small percentages and they are not likely to jeopardize their functional role.

3.2.1.4. Magnetic nanofluids used for planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid

Magnetic nanofluids used as the core liquid in the micro-electric transformer obtained by co-precipitation method [27, 35], is a colloidal suspension of nanoparticles of magnetite (Fe_3O_4), covered with a layer of surfactant oleic acid and dispersed in transformer oil. The main steps in

Processing option: all elements analyzed (normalized); all results in weight%										
Spectrum	In stats.	C	O	Al	Si	Ca	Mn	Fe	Zn	Total %
Spectrum 1	Yes	32.45	27.82	–	0.17		6.99	26.69	5.88	100.00
Spectrum 2	Yes	55.59	21.24	1.18	3.78	2.13	2.92	11.22	1.95	100.00
Spectrum 3	Yes	31.73	28.83	–	0.39	–	6.50	26.67	5.87	100.00
Spectrum 4	Yes	36.77	25.41	–	0.60	–	6.53	25.41	5.28	100.00
Spectrum 5	Yes	33.90	29.16	–	0.60	–	6.19	24.83	5.32	100.00
Spectrum 6	Yes	54.25	10.65	0.16	0.63	0.53	6.15	23.36	4.27	100.00
Spectrum 7	Yes	20.86	28.69	–	0.28	–	8.87	34.09	7.21	100.00
Max.		55.59	29.16	1.18	3.78	2.13	8.87	34.09	7.21	
Min.		20.86	10.65	0.16	0.17	0.53	2.92	11.22	1.95	

Table 2. Normalized values of elements obtained from spectral analysis of ferrite 3F3, corresponding to Spectrum 1–7, 2000× magnification.

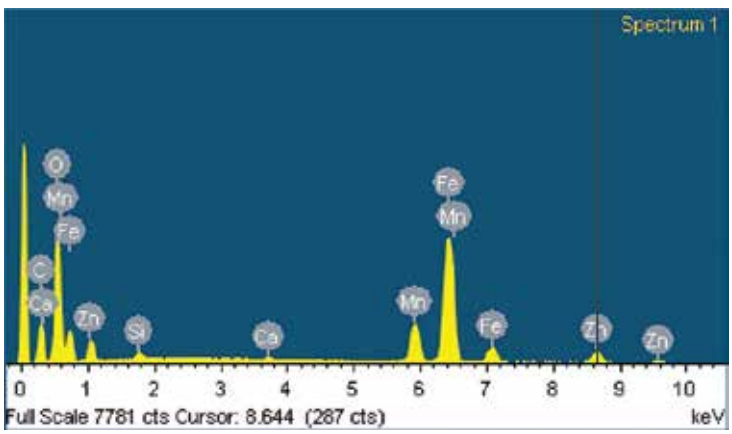

Figure 30. The 3F3 spectra analyze, corresponding to Spectrum 1 and 2000× magnification.

the synthesis procedure for obtaining magnetic nanofluids based on non-polar organic liquids are indicated in [28–30, 35]. To be used as a transformer fluid core, magnetic nanofluid requires good colloidal stability and features adapted to the operating conditions and materials it is in contact with. The magnetic feature is the most important for this application that requires a high saturation magnetization, **Figure 31**.

The maximum volume fraction was set around 23% and the recommended saturation magnetization values ranging between 500 Gs and 1000 Gs. The quality of magnetic nanofluids (NFM) is related to many details of the synthesis process and their stabilization/dispersion in the base fluid (in our case the UTR40 transformer oil). Among these we mention the coprecipitation temperature, Fe^{2+} molar ratio to Fe^{3+}, agitation rate, chemisorption temperature, reaction time, and so on. An essential aspect is the complete coverage of NFM with stabilizer and the elimination of the primary non-adsorbed primary surfactant. Repeated flocculation/redispersing NFM's remain coated with the optimal amount of surfactant [34, 35].

3.2.2. Making a miniature planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid: V3

Planar microtransformers with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid is used in electronic circuits as a separator transformer in the DC/DC converter in harvesting energy applications. The use of a specific colloidal magnetic nanofluid with high saturation magnetization between 500 Gs and 1000 Gs, as a liquid core as part of the magnetic circuit eliminates all air gaps and also the magnetic field of dispersion. Achieving an improved magnetic coupling is obtained by constructive form of planar coils. Use of symmetrically overlayed ferrite cores, **Figure 32**, in conjunction with the magnetic nanofluid to the magnetic circuit assembly, determines the extension of the frequency range up to 1000 Mhz, **Figure 38**. This planar microtransformer, **Figures 32** and **36**, is made up of a planar coils assembly, a magnetic circuit assembly and a housing assembly. Regarding the planar coils, these respect the same manufacturing technology (**Figure 33** and **34**).

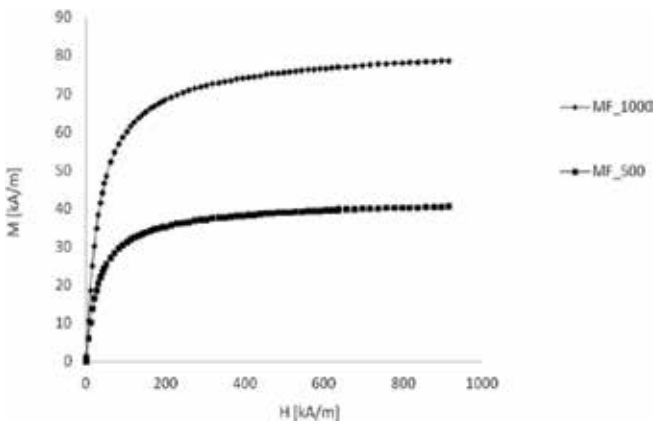

Figure 31. The first magnetization curve for analyzed NMF-UTR40-1000G and NMF-UTR40-500G samples (NMF-UTR40-1000G with Ms. = 78.61 kA/m and NMF-UTR40-500G with Ms. = 40.51 kA/m) [34].

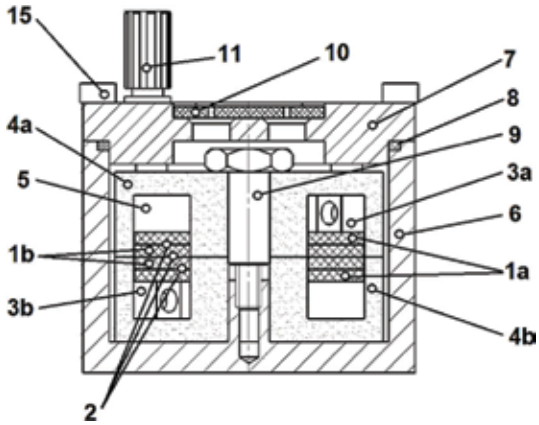

Figure 32. The section through a planar microtransformer with circular spiral windings **1a** and **1b**, with hybrid core—ferrite **4a** and **4b** and colloidal magnetic nanofluid **5**.

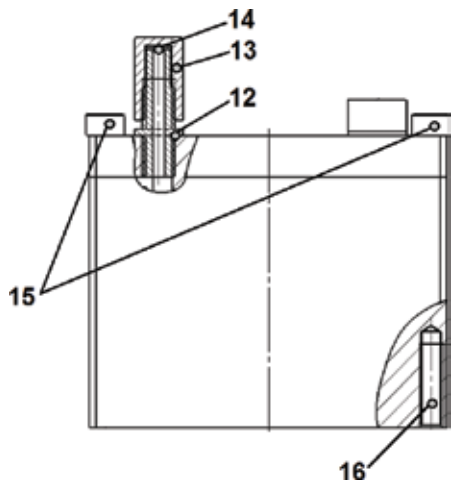

Figure 33. The section through a casing assembly.

A. *The planar coils assembly*

The planar coils assembly consists of four planar coils, **Figures 32** and **34a** and **Figure 34c**, respectively two identical planar coils, **1a** and two identical planar coils **1b**, each disposed on a glass-textolite plate of 1 mm thickness and diameter in the range 35–45 mm, covered on both sides with a copper layer thickness 35 μm and made by milling with a gap between 0.2–0.5 mm, dimensioned according to the current flow through the planar coils. Each primary planar coil, **1a**, is formed of two semi-windings connected in series, double-sided disposed on the same glass-textolite plate. The two semi-windings each have 20 turns made by milling on the glass-textolite plate. Then the two semi-windings are inserted between them resulting in a primary coil **1a**. Each secundary planar coil, **Figures 34a** and **34c**, **1b**, is formed of two semi-windings connected in series, double-sided disposed on the same glass-textolite plate. Also,

Figure 34. (a) Planar coil, (b) magnetic ferrite cores and (c) arrangement of planar coils in ferrite cores, practical achievements.

the two semi-windings each have 20 turns made by milling on the glass-textolite plate. Then the two semi-windings are inserted between them resulting in a secundary coil **1b**. All coils are isolated from each other by three insulation, **2**, of 0.1 mm thick made of "hostaphan" (polyethylene terephthalate), **Figure 12**. The planar coils assembly are fixed relative to the two upper **4a** and lower **4b** magnetic cores by means of two spacers **3a** and **3b** made of glass-textolite, **Figure 32**.

B. *The magnetic circuit assembly*

The magnetic circuit assembly consists of: two magnetic cores, top **4a** and bottom **4b**, 3F3 of the „pot" type, identical from ferrite, symmetrically overlapping according to **Figures 32** and **34b**; a liquid core consisting of a magnetic nanofluid, **5**, **Figure 32** in which are immersed the planar coil assembly and the two magnetic cores **4a** and **4b Figure 34** C, placed in the casing assembly. The role of a liquid core made of a magnetic nanofluid as part of the magnetic circuit, eliminates all air gaps and also the magnetic field of dispersion. The most important magnetic feature for this usage is high saturation magnetization, between 500 Gs and 1000 Gs, **Figure 31**. Volume fraction (the ratio between the volume of magnetite nanoparticles and the volume of the entire magnetic nanofluid) corresponding to this saturation magnetization is in the range of 22–24%.

C. *The casing assembly*

The casing assembly, **Figure 35**, in which are immersed in magnetic nanofluid both the planar coils assembly and the magnetic circuit assembly. **Figure 36** shows a planar microtransformer

Figure 35. Parts of the casing assembly.

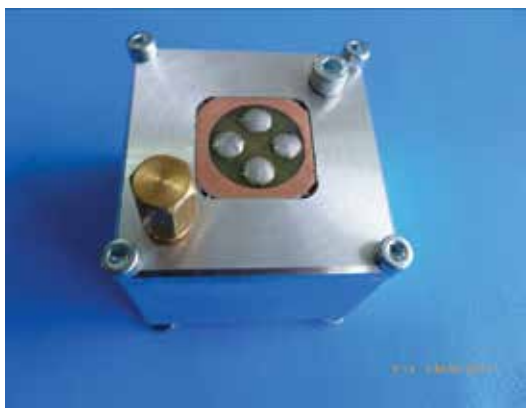

Figure 36. The planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid, practical achievements.

with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid, practical achievements. The casing assembly, **Figures 32** and **33** consists of the box **6** and the lid **7**, both made by duralumin, the gasket **8** and the central screw **9**, which is fixing the magnetic circuit and the planar coils with the box **6**. The lid **7** contains the plate with terminals **10**, the system of the magnetic nanofluid supply **11** (made by a supply nozzle **12**, by a nozzle lid **13** and a nozzle gasket **14**), fixing screws **15** and four location screws **16**.

As I have shown, by using a specific magnetic nanofluid with high saturation magnetization, ranging between 500 Gs and 1000 Gs, as a liquid core of a magnetic circuit, the air gaps and the dispersive magnetic field lines are removed. Thus, magnetic nanofluid is used both as a coolant and as part of the hybrid magnetic core. Also, an improved magnetic coupling by up to 10% is noticed, together with an increase of the overall efficiency by up to 5%. As we will see below, experimental measurements in dinamic mode proves extension of the frequency range up to 1000 MHz, by symmetrical superposition of the ferrite magnetic cores in conjunction with the specific magnetic nanofluid.

3.2.2.1. Experimental measurements on the planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid

A. Experimental measurements performed in static mode

Static mode measurements have been made with the bridge "Precision LCR Agilent E 4980A" for the microtransformer without magnetic nanofluid as well as for the microtransformer with hybrid core—ferrite and colloidal magnetic nanofluid with 500 Gs saturation magnetization, for a frequency variation in the range of 100–300 kHz (**Figure 36**).

Number of turns of the primary coil are N1 = 80 turns and number of turns of the secondary coil are N2 = 80 turns, (separator transformer). The bridge "Precision LCR Agilent E 4980A" it is used with option LEVEL = 2 V.

Analyzing the results obtained, synthesized in **Tables 3** and **4**, following conclusions are resulted:

- in the presence of magnetic nanofluid, the quality factor for the primary planar coil as well as the quality factor for the secondary planar coil increases significantly;
- there is a better frequency behavior in the presence of magnetic nanofluid.
- Experimental measurements performed on dynamic mode

In order to perform experimental measurements in dynamic mode, the transformer is connected in an electronic circuit diagram as shown in **Figure 37**. The Arbitrary Waveform Generator FLUKE PM 5138A was set to provide an excitation signal with a rectangular

Measured parameters for primary coil in the case if not magnetic nanofluid					
Frequency	100 kHz	150 kHz	200 kHz	250 kHz	300 kHz
L_{p1} [mH]	3.672	2.129	1.378	0.981	0.75
D_1 [−]	4.45	3.743	3.117	2.647	2.3
Q_1 [−]	0.23	0.27	0.32	0.38	0.44
G_1 [mS]	1.92	1.865	1.793	1.712	1.624
Rp_1 [Ω]	520	536.32	557.58	584.25	615.78
Rdc_1 [Ω]	10.64	10.64	10.64	10.64	10.64
Measured parameters for secondary coil in the case if not magnetic nanofluid					
L_{p2} [mH]	2.89	1.615	1.051	0.764	0.600
D_2 [−]	3.292	2.6	2.091	1.739	1.488
Q_2 [−]	0.3	0.38	0.48	0.57	0.67
G_2 [mS]	1.8	1.705	1.581	1.448	1.314
Rp_2 [Ω]	553.5	586.64	632.47	690.75	761
Rdc_2 [Ω]	10.8	10.8	10.8	10.8	10.8

Table 3. Measured parameters for primary and secondary coil in the case if not magnetic nanofluid.

Measured parameters for primary coil in the case with presence of magnetic nanofluid					
Frequency	100 kHz	150 kHz	200 kHz	250 kHz	300 kHz
L_{p1} [mH]	3.23	1.725	1.1	0.79	0.614
D_1 [−]	4.34	3.30	2.64	2.21	1.92
Q_1 [−]	0.23	0.3	0.38	0.45	0.52
G_1 [mS]	2.13	2.03	1.91	1.78	1.65
Rp_1 [Ω]	470	492	522	560	602
Rdc_1 [Ω]	10.62	10.62	10.62	10.62	10.62
Measured parameters for secondary coil in the case with presence of magnetic nanofluid					
L_{p2} [mH]	1.9	1.09	0.782	0.635	0.555
D_2 [−]	2.143	1.54	1.22	1.024	0.89
Q_2 [−]	0.46	0.64	0.81	0.97	1.11
G_2 [mS]	1.788	1.5	1.246	1.029	0.859
Rp_2 [Ω]	559	664	802.54	971	1160
Rdc_2 [Ω]	10.8	10.8	10.8	10.8	10.8

Table 4. Measured parameters for primary and secondary coil in the case with presence of the magnetic nanofluid, NMF-UTR40-500G type.

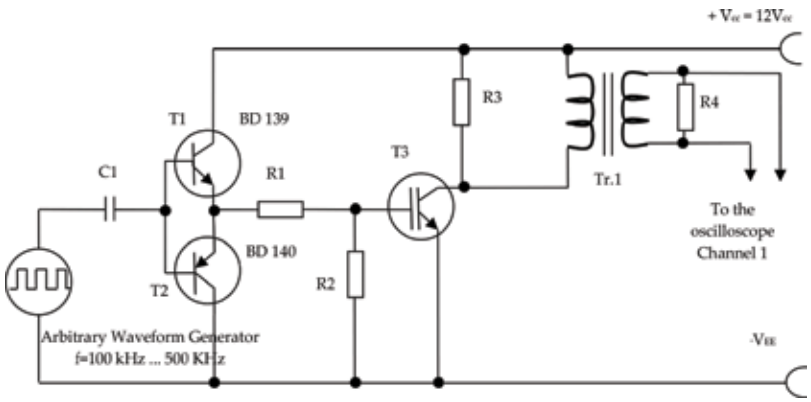

Figure 37. Electronic circuit diagram for testing the planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid, on dynamic mode.

waveform, with features: the amplitude 10 V peak-to-peak, duty cycle k = 50% and frequency in the range of f = 100 to 1000 kHz. In Blue, at the bottom, **Figure 18**, the waveform capture of the arbitrary function generator is highlighted. Also, the output (secondary winding) waveforms capture in yellow, at the top is highlighted, **Figure 38**. Both waveforms captures are achieved with a digital oscilloscope Tektronix TDS 2014B.

The waveforms capture results for the frequency in the range of f = 100 to 1000 kHz can be concluded as shown in **Figure 38a–h**. These shows a good behavior of the planar microtransformer

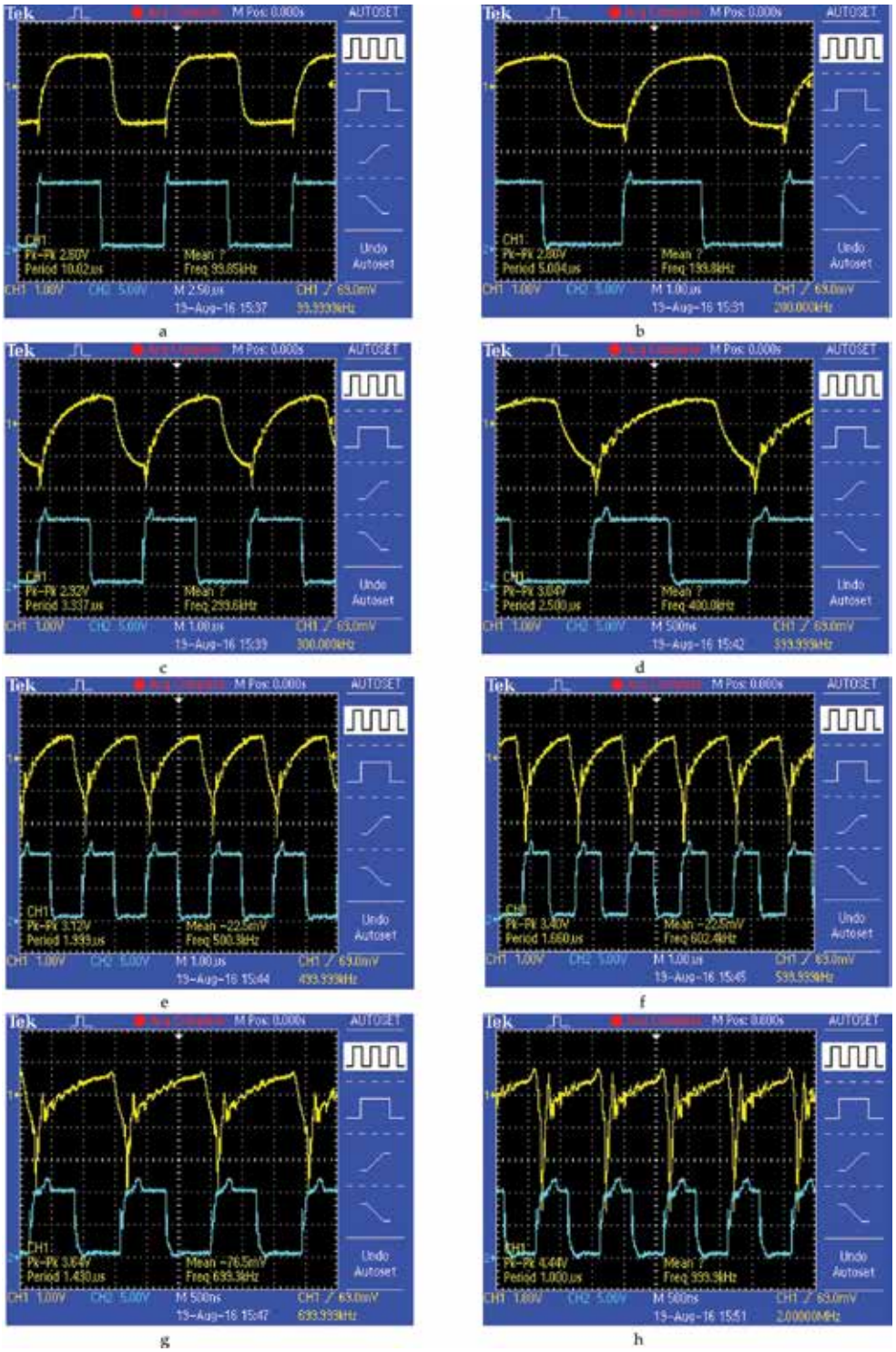

Figure 38. The waveform capture of the arbitrary function generator at the bottom and the output (secondary winding) waveforms capture at the top is highlighted, for the frequency in the range of f = 100–1000 kHz, from a. to h.

http://dx.doi.org/10.5772/intechopen.72613

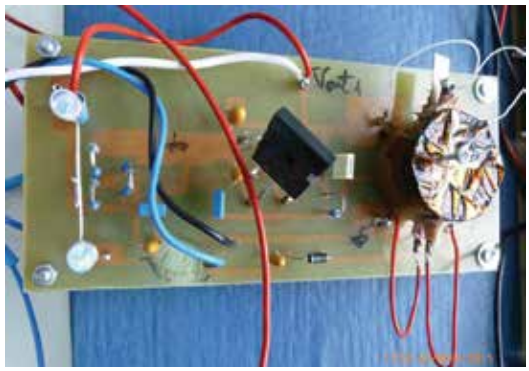

Figure 39. DC/DC converters, practical achievements for applications such as energy harvesting, made with the planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid –V2.

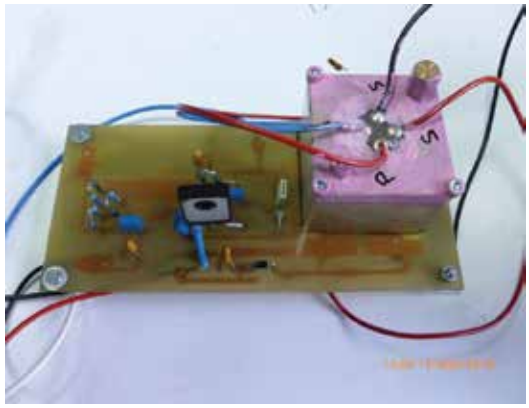

Figure 40. DC/DC converters, practical achievements for applications such as energy harvesting made with the planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid –V3.

with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid. Thereby, it results in the possibility of using this type of transformer in DC/DC converters, for applications such as energy harvesting.

As shown in **Figures 39** and **40**, the planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid –V2 and V3 is used in applications of energy harvesting. **Figure 41**, the electronic circuit diagram of DC/DC converter, designed for energy harvesting applications is shown.

3.2.3. Numerical simulation of the planar transformer with circular spiral windings with hybrid core-Ferrite and colloidal magnetic nanofluid-V4

3.2.3.1. CAD design

Variant V4 of the planar transformer corresponds to the DC/DC converters of high active power, that exceeding 100 watts. Choosing a particular type of magnetic nanofluid for a given application is an essential stage in design and can be facilitated by numerical modeling that

uses quantitative estimates of material properties (magnetoreological, thermal, magnetic, electrical, etc.) for the validation of numerical models used in designing and evaluating the behavior of the planar transformer. The evaluation of the magnetic flux inside the planar transformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid is done for two propose magnetic nanofluid, NMF-UTR40-50G and NMF-UTR40-500G, whose magnetization at saturation is of 50 Gs and 500 Gs respectively. Mathematical

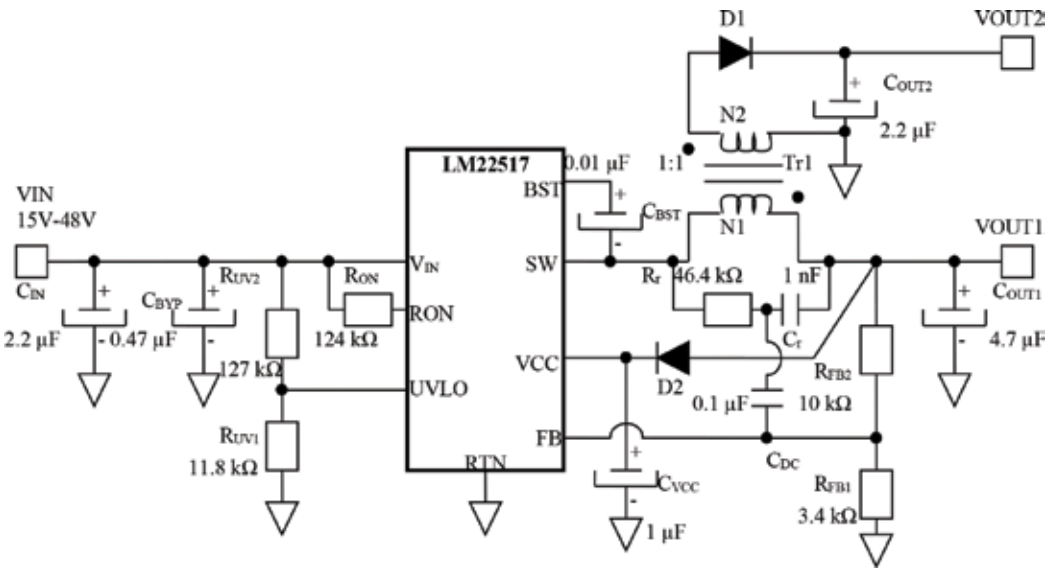

Figure 41. Electronic circuit diagram of DC/DC converter, designed for energy harvesting applications, made of LM22517 Texas Instruments and planar microtransformer with circular spiral windings with hybrid core—ferrite and colloidal magnetic nanofluid [33, 36, 37].

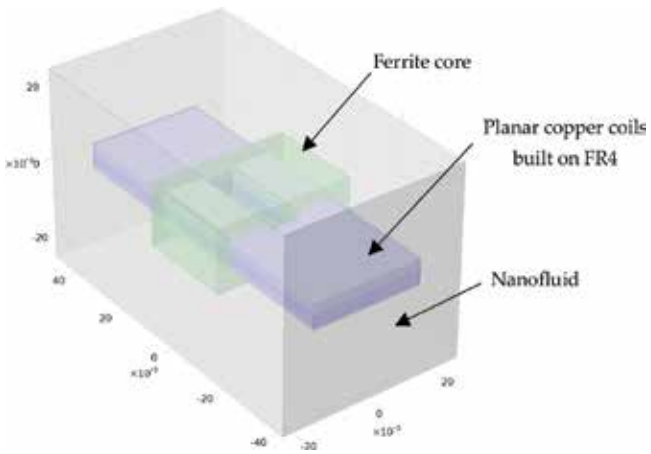

Figure 42. The CAD design and computational domain of the transformer submerged in magnetic nanofluid NMF-UTR40-50G or NMF-UTR40-500G.

models and numerical simulation are defined, under stationary hypothesis, by the finite element (FEM) technique [38, 39]. The computational domain was constructed by CAD methods, based on the design dimensions of the transformer, **Figure 42**.

Also, the details of the primary and secondary windings profiles are shows in **Figures 43** and **44**. To reduce the complexity of the model and the computational efforts, some elements (e.g. between layers, supports, etc.) have been excluded from the computational domain.

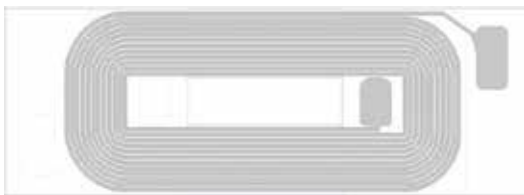

Figure 43. Details of the primary windings profiles.

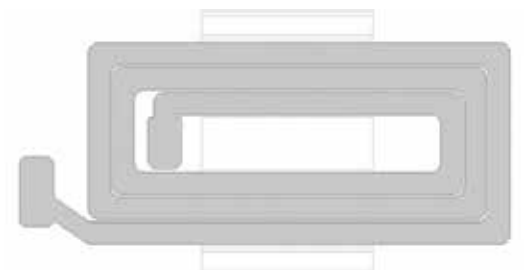

Figure 44. Details of the secondary winding profiles.

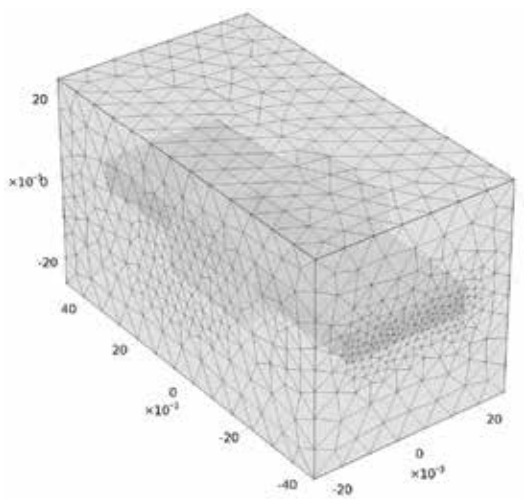

Figure 45. The discretization network (mesh) of the transformer, numerical model.

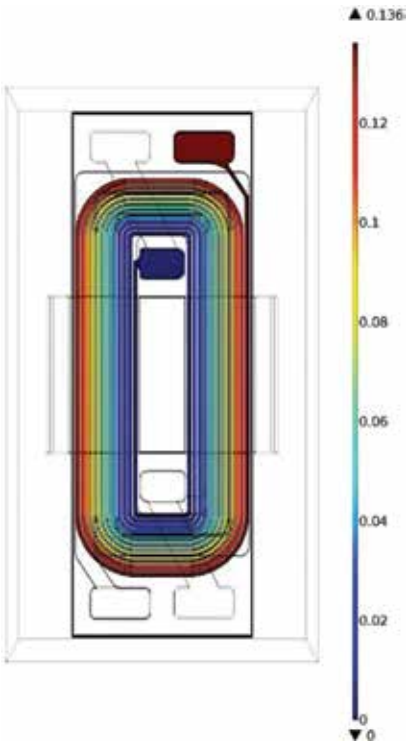

Figure 46. The spectra of electric field in the primary planar copper winding by colored boundary map in volts.

The problem is solved by the Galerkin finite element (FEM) technique. A discretization network consisting of 850,000, tetrahedral, quadratic Lagrange elements was generated automatically to model the field, **Figure 45**.

3.2.3.2. Mathematical model

The magnetic field source, the electrical currents in the windings, must be known. Therefore, an electrokinetic field analysis is defined by the partial differential equation (PDE). Firstly, the magnetic field source as well as the electrical currents in the windings must be known. Therefore, an electrokinetic field analysis is defined by the partial differential equation, (14), (15), (16) and (17),

$$\nabla_t \cdot d(\sigma \nabla_t V) = dQ_j \tag{14}$$

where σ [S/m] is the electrical conductivity, Q_j [W/m^3] is an external current source and d [m] is the thickness of the shell. The operator ∇_t represents the tangential derivative along the shell [40]. The stationary magnetic field is computed by solving [38–40],
for the copper windings and free space

$$\nabla \times \left(\mu_0^{-1}\mu_r^{-1}\nabla \times \mathbf{A}\right) = \mathbf{J_s}^e, \tag{15}$$

for the magnetic fluid

$$\nabla \times \left(\mu_0^{-1}\mu_r^{-1}\nabla \times \mathbf{A} - \mathbf{M}\right) = 0, \tag{16}$$

where **A** [T·m] is the magnetic vector potential, $\mathbf{J_s}^e$ [A/m^2] is the external electric current density of the shell ($\mathbf{J_s}^e \neq 0$ inside the planar coils), $\mu_0 = 4\pi \times 10^{-7}$ [H/m] is the magnetic permeability of free space, and μ_r is the relative permeability. For the 3CP90 ferrite core μ_r = 1720 and for the copper windings and the free space μ_r = 1. Also, **M** [A/m] is the magnetization in the magnetic nanofluid, approximated by the analytic formula [40],

$$M = \alpha \arctan(\beta H), \tag{17}$$

here H [A/m] is the magnetic field strength, and α, β are empiric constants selected to fit the experimental magnetization characteristic of the magnetic nanofluid (α = 3050 A/m and $\beta = 1.5\times10^{-5}$m/A for the NMF-UTR40-50G, respectively, $\alpha = 4.85 \times 10^4$A/m and $\beta = 2.5 \times 10^{-5}$m/A for NMF-UTR40-500G).

3.2.3.3. Numerical simulation results

An iterative flexible generalized minimum residual solver (FGREMS) was used to solve the mathematical model (5), (6), (7) and (8). **Figures 46** and **47** present the electric field in the windings by voltage boundary color map, boundary conditions were chosen for nominal working conditions of the transformer are considered.

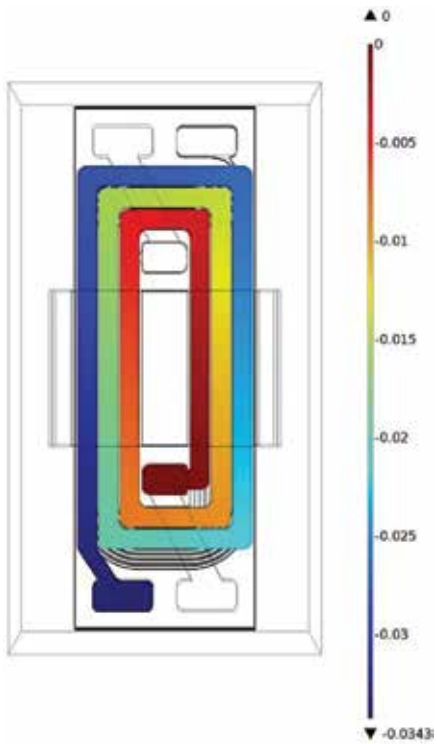

Figure 47. The spectra of electric field in the secondary planar copper winding by colored boundary map in volts.

The current shell density resulting from the electric field problem is used to solve the magnetic field problem in the transformer. **Figure 48** shows the magnetic field in the transformer submerged in the magnetic nanofluid NMF-UTR40-50G through field lines for different

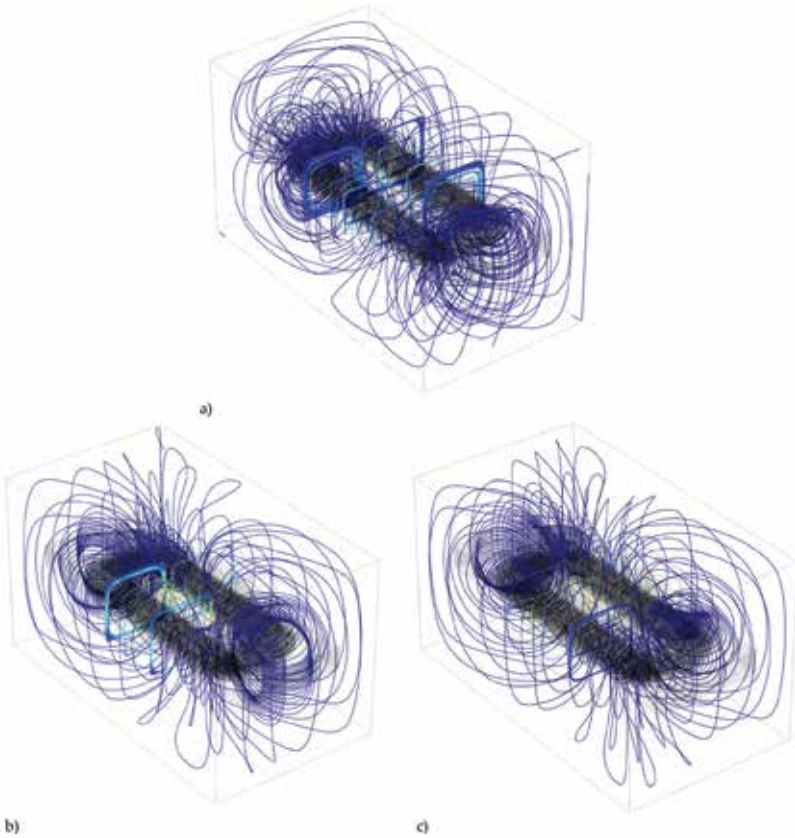

Figure 48. Magnetic flux density (tubes) for different powering schemes (NMF-UTR40-50G magnetic nanofluid).

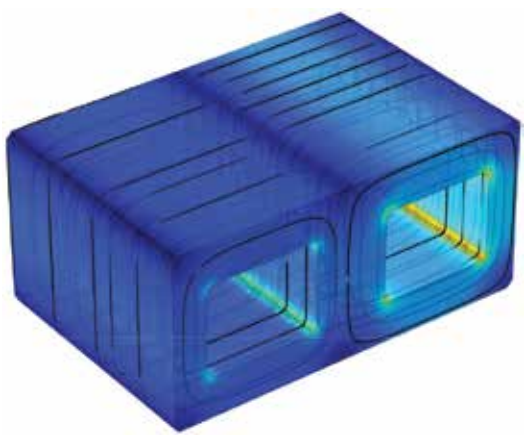

Figure 49. Normalized magnetic induction, by boundary color map, and tubes of magnetic flux density.

powering alternatives: (a) both windings are "ON", the currents are in opposite directions – differential magnetic fluxes, (b) primary winding is "ON" and secondary winding is "OFF" and (c) primary winding is "OFF" and secondary winding is "ON".

The magnetic field simulation result indicates that the fascicular magnetic field lines close mainly through the ferrite core, which offers a lower reluctance path than the magnetic nanofluid. In **Figure 49** the flux inside the solid ferrite core is presented by color map of normalized magnetic induction, *B*, as well as the lines of magnetic field density.

The magnetic field problem was solved also for the NMF-UTR40-500G magnetic nanofluid which has higher saturation limit, **Figure 50** shows the magnetic flux density (tubes) for different powering schemes.

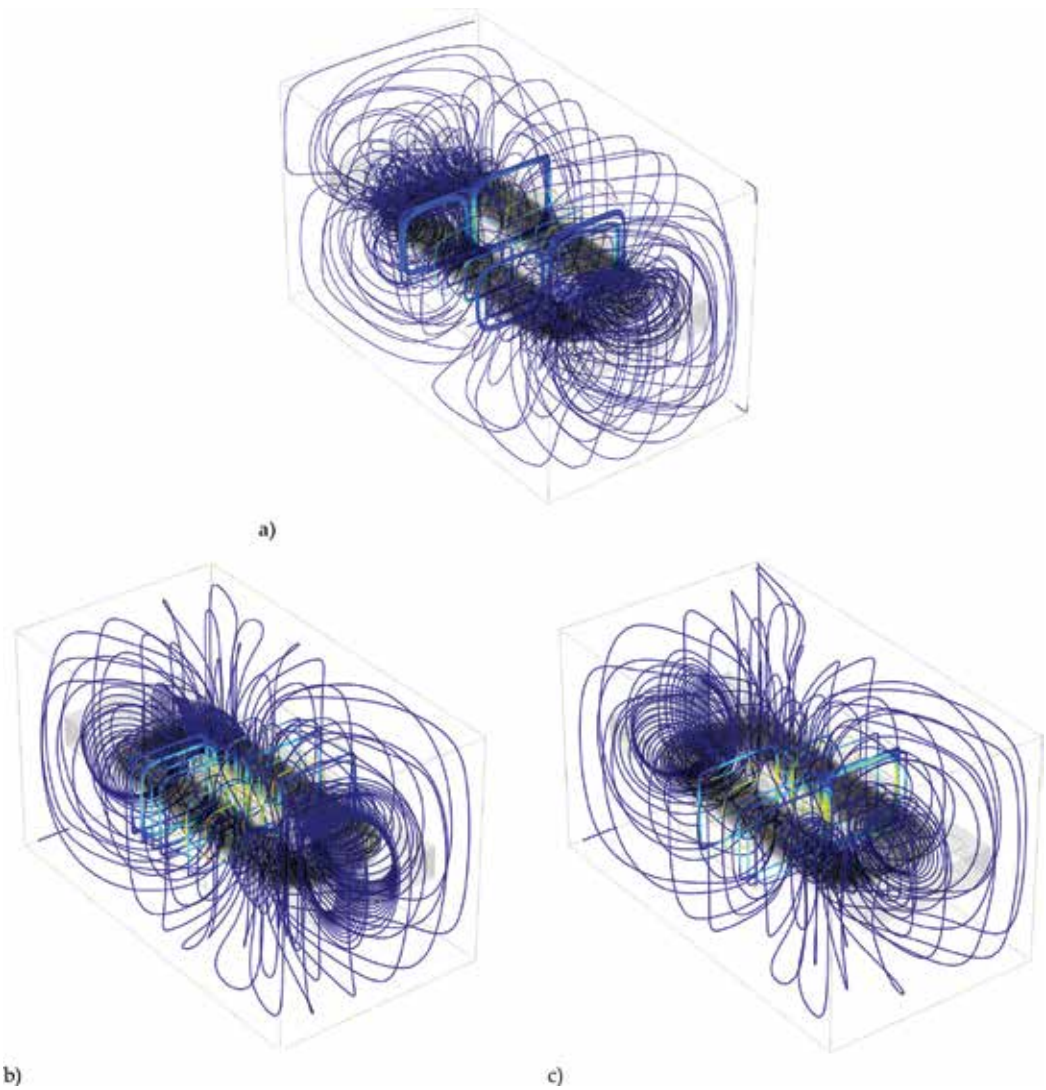

Figure 50. Magnetic flux density (tubes) for different powering schemes (NMF-UTR40-500G magnetic nanofluid).

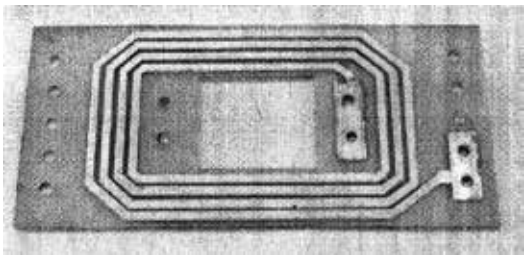

Figure 51. Planar coil corresponding to primary and secondary coils, practical achievements.

Figure 52. Planar transformer with planar windings with hybrid core—ferrite and colloidal magnetic nanofluid—V4, practical achievements.

The result indicates insignificant differences between the two types of magnetic nonfluids in terms of the magnetic flux distribution inside the fluid part of the magnetic core. However, because of the higher saturation limit, the NMF-UTR40-500G it is expected to perform better in higher power applications. For different models, the numerical investigations was performed under steady state conditions, to estimate the lumped parameters of the transformer and to evaluate the thermal behavior [41].

Figure 51 shows the planar coil corresponding to primary and secondary coils, practical achievements, for V4 variant of planar transformer. Also, **Figure 52** shows the practical achievement of the planar transformer with planar windings with hybrid core—ferrite and colloidal magnetic nanofluid—V4 variant.

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Nomenclature

Lp_1 inductance of the primary coil, corresponding to an equivalent $Lp_1 – Rp_1$ pattern disposed in parallel;

Lp_2 inductance of the secondary coil, corresponding to an equivalent $Lp_2 – Rp_2$ pattern disposed in parallel;

D_1 tangent of the loss angle for the primary coil;

D_2 tangent of the loss angle for the secondary coil;

Q_1 Quality factor for the primary coil;

Q_2 Quality factor for the secondary coil;

G_1 conductivity ($1/Rp_1$) of the primary coil, corresponding to an equivalent $Lp_1 – Rp_1$ pattern disposed in parallel;

G_2 conductivity ($1/Rp_2$) of the secondary coil, corresponding to an equivalent $Lp_2 – Rp_2$ pattern disposed in parallel;

Rp_1 the resistance of the primary coil, corresponding to an equivalent $Lp_1 – Rp_1$ pattern disposed in parallel;

Rp_2 the resistance of the secondary coil, corresponding to an equivalent $Lp_2 – Rp_2$ pattern disposed in parallel;

Rdc_1 the resistance of the primary coil measured in DC;

Rdc_2 the resistance of the secondary coil measured in DC.

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Section 2

Circuit Design and Architectures

Chapter 3

Nanoarchitecture of Quantum-Dot Cellular Automata (QCA) Using Small Area for Digital Circuits

Radhouane Laajimi

Additional information is available at the end of the chapter

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Abstract

Novel digital technologies always lead to high density and very low power consumption. One of these concepts—quantum-dot cellular automata (QCA), which is one of the new emerging nanotechnologies, is based on Coulomb repulsion. This chapter presents a novel design of 2-input Exclusive-NOR (XNOR)/Exclusive-OR (XOR) gates with 3-input Exclusive-NOR (XNOR) gates which are composed of 10 cells on 0.006 μm^2 of area. A novel architecture of 3-input Exclusive-OR (XOR) gate is defined by 12 cells on 0.008 μm^2 of area. The proposed design of 2-input XOR/XNOR gate structures provide less area and low complexity than the best reported design. The simulation results of proposed designs have been achieved using QCA Designer tool version 2.0.3.

Keywords: quantum-dot cellular automata (QCA), nanoelectronic, QCA technology, majority voter, Exclusive OR (XOR) gate, QCA Designer

1. Introduction

In recent years, the use of CMOS technology is limited by high consumption, low speed, and density beyond 10 nm. To overcome these problems, a number of researchers have been ascertained to find the solution for this classical CMOS technology which is quantum-dot cellular automata (QCA) used for high-speed application.

Nowadays, QCA transistor-less technology, single electron transistor (SET), and carbon nanotube (CNT) are being used as an alternative to CMOS technology. The use of QCA on the nanoscale has a promising future because of its ability to achieve high performance in terms of clock frequency, device density, and power consumption [1–4] if it is compared to similar implementations with conventional VLSI technology. These advantages make the proposed QCA technology useful for high-performance electronic applications applied on mobile or autonomous devices where power consumption and real-time processing low are needed.

Recently, using QCA technology for electronic modules design has become widely used [5–7]. In [8–10], memory circuits have been proposed. In [11–13], reversible full adder/subtractor and multiplier has been designed. In [14], a sequential circuits based on QCA technology has been proposed. In [15], a decoder circuit based on QCA technology has been developed.

In this chapter, we will describe the background of QCA technology. This new concept will take the great advantage of a physical effect called the Coulomb force. In the next, we will describe how the information can be propagated through QCA cell by clicking. Then, we will introduce the basic elements and gates used for QCA circuits. The proposed 2-input "XOR" circuit occupies small area of 0.006 μm^2, low complexity of 10 cells as compared to previous best designs. Besides, the proposed 3-input "XOR" design occupies only 0.008 μm^2 whereas the previous best reported design occupies 0.0116 μm^2 area. On the other hand, the proposed 3-input "XOR" gate has 32% less area than best reported design.

2. Background of QCA

In 1993, Craig Lent [16] proposed a new concept called quantum-dot cellular automata (QCA). This emerging technology has made a direct deviation to replace conventional CMOS technology based on silicon [17]. QCA generally uses arrays of coupled quantum dots in order to implement different Boolean logic functions. QCA or quantum-dot cellular automata as its name is pronounced uses the quantum mechanical phenomena for the physical implementation of cellular automata. In the general case, conventional digital technologies require a range of voltages or currents to have logical values, whereas in QCA technology, the position of the electrons gives an idea of the binary values [18]. The advantages of this technology are [19] especially given in terms of speed (range of terahertz), density (50 Gbits/cm^2) [20] and in terms of energy or power dissipation (100 W/cm^2).

QCA is based essentially on a cell. Each cell represents a bit by a suitable charge configuration as shown in **Figure 1**. It consists of four quantum dots and two electrons charge. Under the effect of the force of Colombian repulsion, the two electrons can be placed only in two quantum sites diametrically opposite.

A QCA cell is composed of four points with one electron each in two of the four points occupying diametrically opposite locations. The question that arises in this case is why do electrons occupy quantum dots of opposite or diagonal corner To answer this question, it is enough to have an idea about the principle of the repulsion of Coulomb, which is less effective with respect to the electrons when they are in adjacent quantum dots. The points are coupled to one another by tunnel junctions.

Thus, the internal effect of the cell highlights two configurations possible; each one will be used to represent a binary state "0" or "1." A topology of QCA is a paving of cells QCA. The interaction between the cells makes it possible to transmit information which gives the possibility of replacing physical interconnection of the devices. The information (logic 0 or logic 1) can propagate from input to the output of the QCA cell only by taking advantage of the force of repulsion as shown in **Figure 2**.

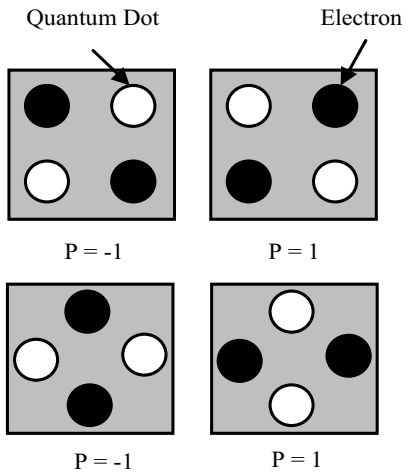

Figure 1. Basic QCA cell.

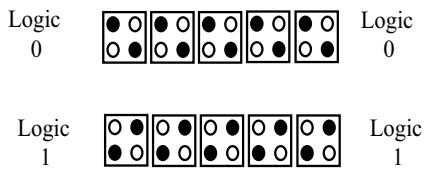

Figure 2. Operations of a QCA wire propagation by application of logic 0 and logic 1 1 to a QCA cell at the input.

3. Clocking in QCA

Clocking is an important term in QCA design. In order to propagate the information through QCA without any random adjustments of QCA cells, it is necessary to make a clock to guarantee the same data putting from input to the output. According to **Figure 3**, timing in QCA is obtained by clocking in four distinct periodic phases [21, 22] namely Switch, Release, Relax, and Hold.

Based on the position of the potential barrier, the arrays of QCA cells in each phase have different polarizations. There are four phases, and every phase has its own polarizations as shown in **Table 1**.

From **Table 1**, during the "Switch" phase of the clock, the QCA cell begins without polarization and switches to polarized state while the potential barrier has been raised from low to high. In the "'Hold" phase, the polarization state is preserved as the preceding phase and the potential barrier is high. From the "'Release" phase, the potential barrier is lowered and the cells become unpolarized. In "Relax" phase, the potential barrier remains lowered and the cells keep at nonpolarized state. This phase, the cells are ready to switch again. This way information is propagated in QCA circuits by keeping the ground-state polarization all the time. **Figure 4** illustrates the polarizations and interdot barriers of the QCA cells in each of the QCA clock zones.

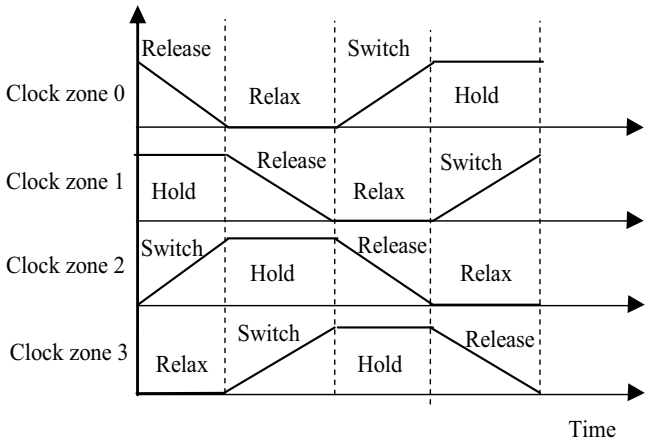

Figure 3. Four phases of QCA clock zones.

Clock phase	Potential barrier	Polarization state of the cells
Hold	Held high	Polarized
Switch	Low to high	Polarized
Relax	Low	Unpolarized
Release	Lowered	Unpolarized

Table 1. Operation of QCA clock phases.

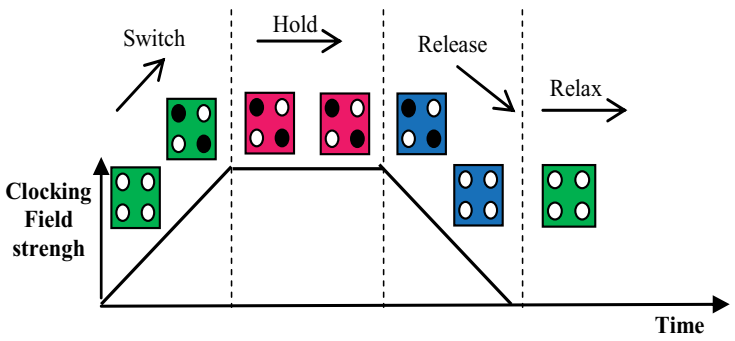

Figure 4. Schematic of interdot barriers in QCA clock.

4. Basic QCA elements and gates

Many architectures of logic devices can be designed by using adequate arranging of QCA cells. The biggest advantage of this wireless technology is that the logic is carried by the cells

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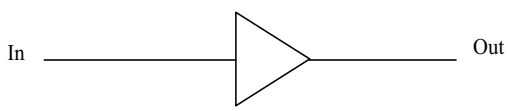
themselves. The fundamental QCA logic is binary wire, inverter, and majority voter. These QCA logic gates are evaluated and simulated using the QCA Designer tool version 2.0.3.

4.1. Noninverter gate or binary wire

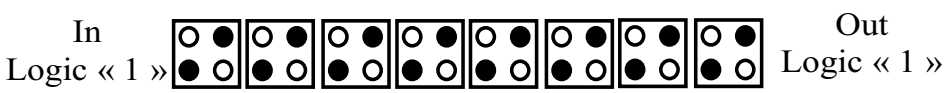
The great advantage of cell QCA is that all the close cells are aligned on a specific polarization, which depends on the input cell or the driver cell. Hence, by arranging the cells side-by-side according to the type "0" or "1" applied to the input cell, any logic can be transferred. Consequently, this gate can play the role of a wire or binary interconnection or noninverter gate as shown in **Figure 5(a)**. The layout of each cell given by binary wire is represented in **Figure 5(b)**.

The simulation results of the noninverter gate are presented in **Figure 5(c)**. One waveform with one frequency is applied to the input (In), one waveform for the first clock (Clk 0), and one waveform for the binary wire outputs (Out). From simulation results of binary wire given by **Figure 5(c)**, the expression from the output pulses of the noninverter gate can be deduced, which is given by Eq. (1):

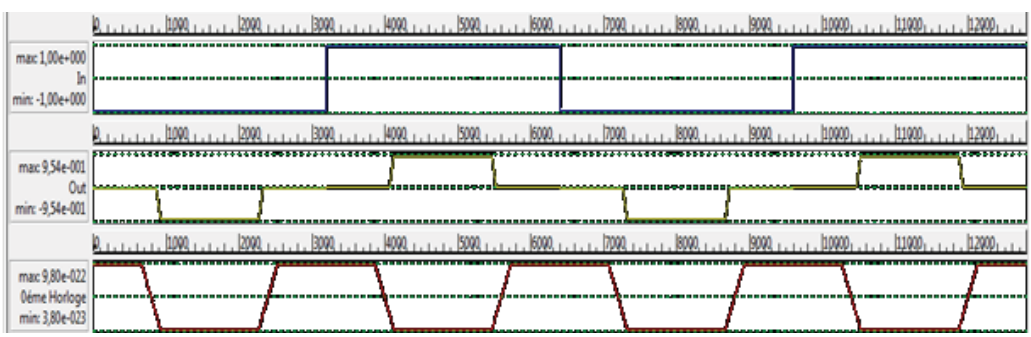
$$Out = In \ . \overline{Clk\ 0} \tag{1}$$



(a)



(b)



(c)

Figure 5. Binary wire, (a) representation, (b) QCA layout, and (c) simulation results.

4.2. Inverter gate

Thanks to the columbic interaction between electrons in neighboring cells, different types of the inverter gates in QCA were proposed [23–26]. The principle operation of this gate is to invert the input signal applied. If the applied input is low then the output becomes high and vice versa, as shown in **Figure 6(a)** and **6(b)**. The input "In" is given to one of the ends and the output reversed will be obtained at the output "Out." The position of the electrons and the layout of each cell are represented in **Figure 6(b)**. The principle of operation of this gate is based on the wire of input, which will be prolonged in two parallel wires and will polarize the cell placed at the end of these two wires, which implies the opposite polarization of this cell due to the Coulomb repulsion.

According to **Figure 6(c)**, the simulation results of the inverter gate are presented. One waveform with one frequency is applied to the input (In), one waveform for the clock 0 (Clk 0), and one waveform for the inverter gate outputs (Out).

From simulation results of the output pulses inverter gate (Out) given by **Figure 6(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (2):

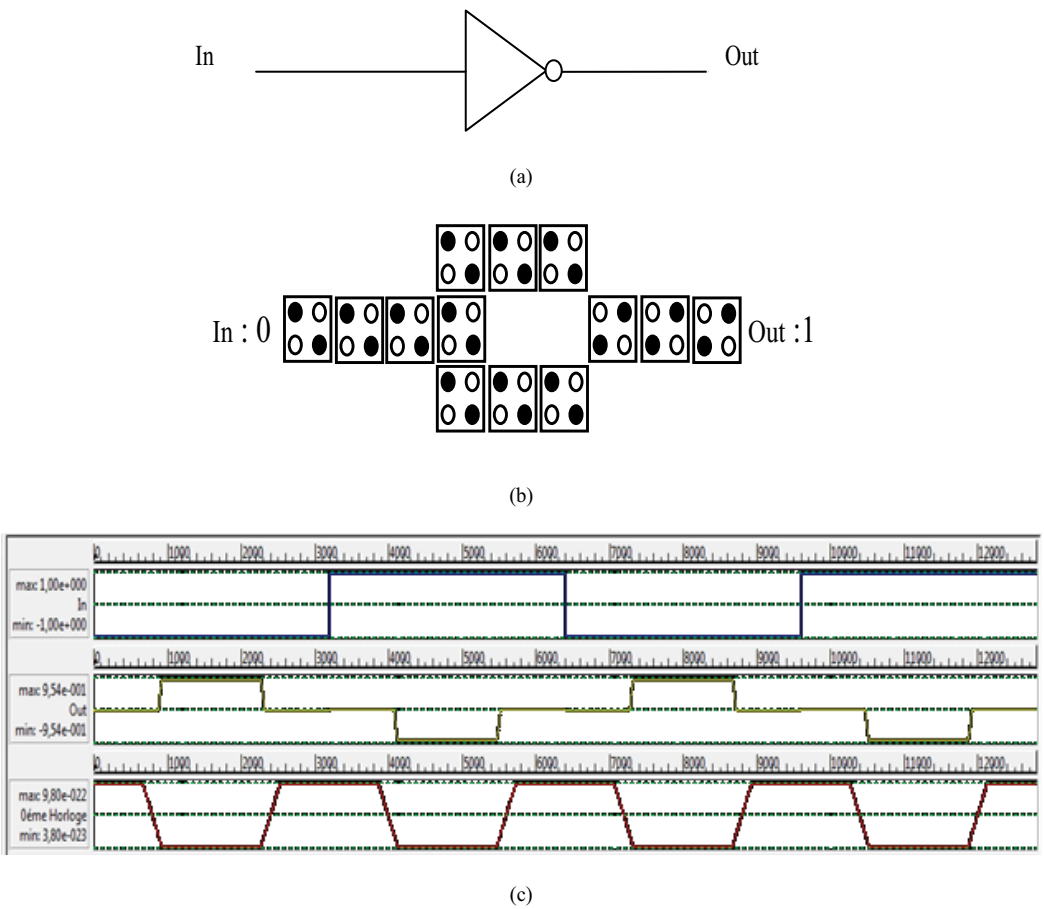


Figure 6. Inverter gate, (a) representation, (b) QCA layout, and (c) simulation results.

$$Out = \overline{In} \ . \overline{Clk}\ 0 \tag{2}$$

4.3. QCA majority voter

In QCA circuits, the majority voter (MV) plays an important role for logic gates. It is only composed of five cells: three input cell, one output cell, and a center cell, which is the decision-making cell. These cells are arranged like a cross with three inputs (a, b, and c) and one output (Out). This gate is based on the majority logic value given at its input as shown in **Figure 7(a)**. The layout of each cell given by MV is represented in **Figure 7(b)**.

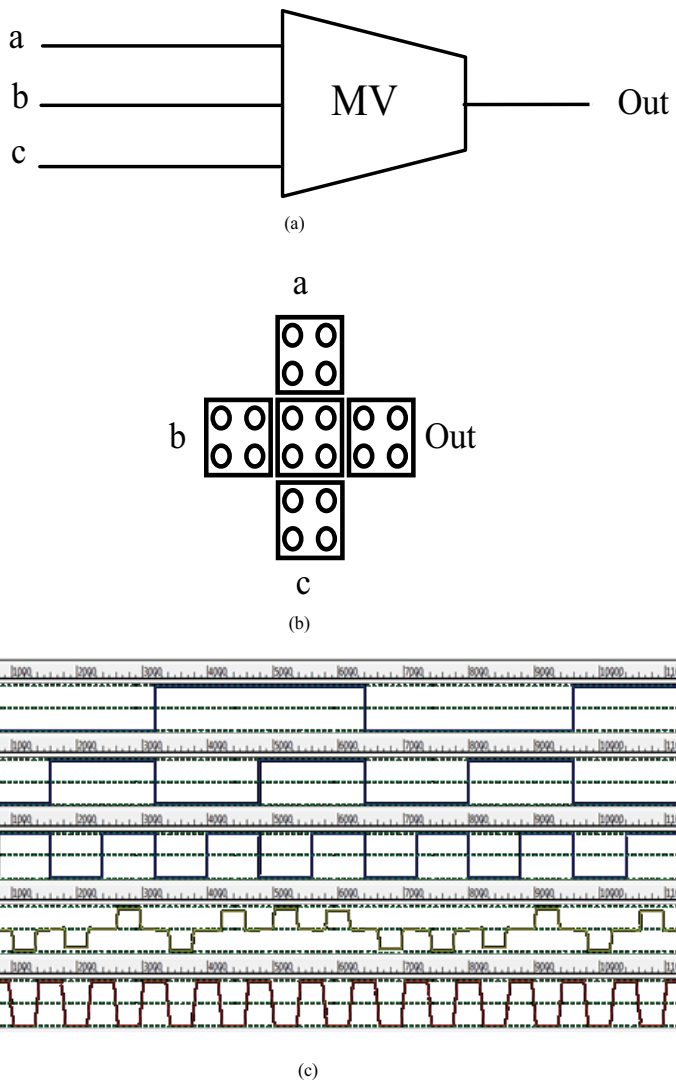


Figure 7. Majority voter (MV) gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

According to **Figure 7(c)**, the simulation results of the majority voter (MV) gate are presented. Three waveforms with different frequencies are applied to the inputs (a, b, and c), one waveform for the clock 0 (Clk 0), and one waveform for the MV outputs (Out). From simulation results of the output pulses of MV gate given by **Figure 7(c)**, the expression of the MV gate can be given by Eq. (3):

$$Out = a \,.\, b + b \,.\, c + c \,.\, a \tag{3}$$

From the majority voter gate, depending on the input fixed to 0 or 1, other logical gates can be deduced such as AND/OR gates.

- On the one hand, when one of the inputs of MV is fixed to 1, the logical function of OR gate is obtained and can be expressed in Eq. (4):

$$Out = a + b \quad when \quad c = 1 \tag{4}$$

Figure 8 shows the representation, QCA layout, and simulation of OR gate.

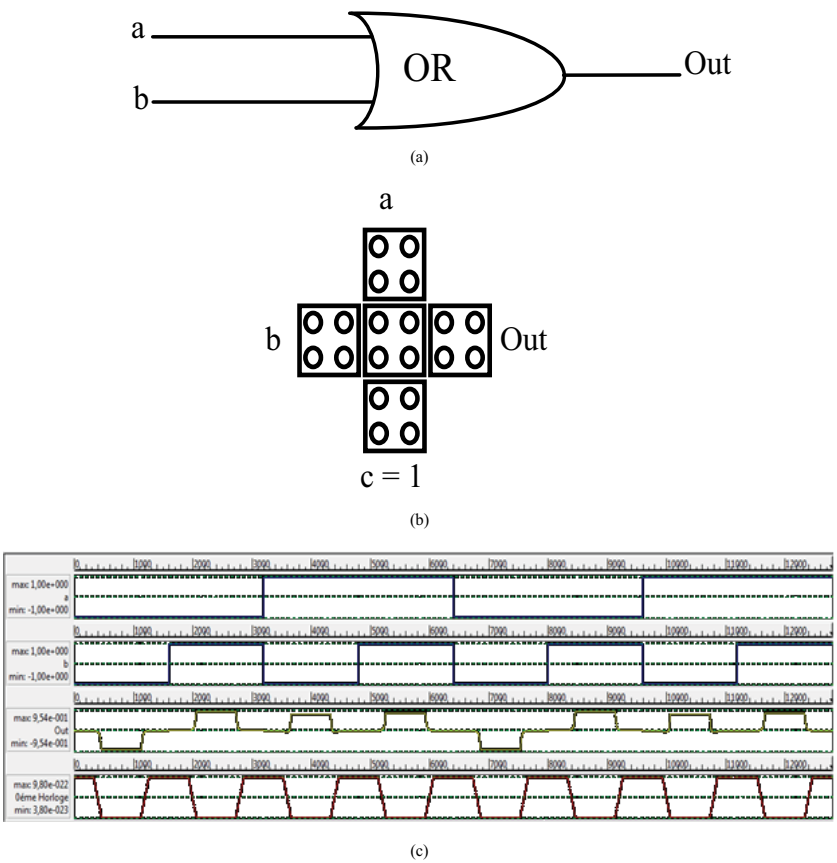


Figure 8. OR gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

According to **Figure 8(c)**, the simulation results of the OR gate are presented. Two waveforms with one frequency are applied to the inputs (a and b), one waveform for the clock 0 (Clk 0), and one waveform for the OR gate outputs (Out).

From simulation results of the output pulses OR gate (yellow) given by **Figure 8(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (5):

$$Out = (a + b).\overline{Clk}\ 0 \tag{5}$$

- On the other hand, when one of the inputs of MV is fixed to 0, the logical function of AND gate is obtained (**Figure 9**) and can be expressed in Eq. (6):

$$Out = a\ .\ b \quad when \quad c = 0 \tag{6}$$

Figure 9 shows the representation, QCA layout, and simulation of AND gate.

According to **Figure 9(c)**, the simulation results of the AND gate are presented. When there are two waveforms, with one frequency is applied to the inputs (a and b), one waveform given for the clock 0 (Clk 0), and one waveform for the AND gate outputs (Out).

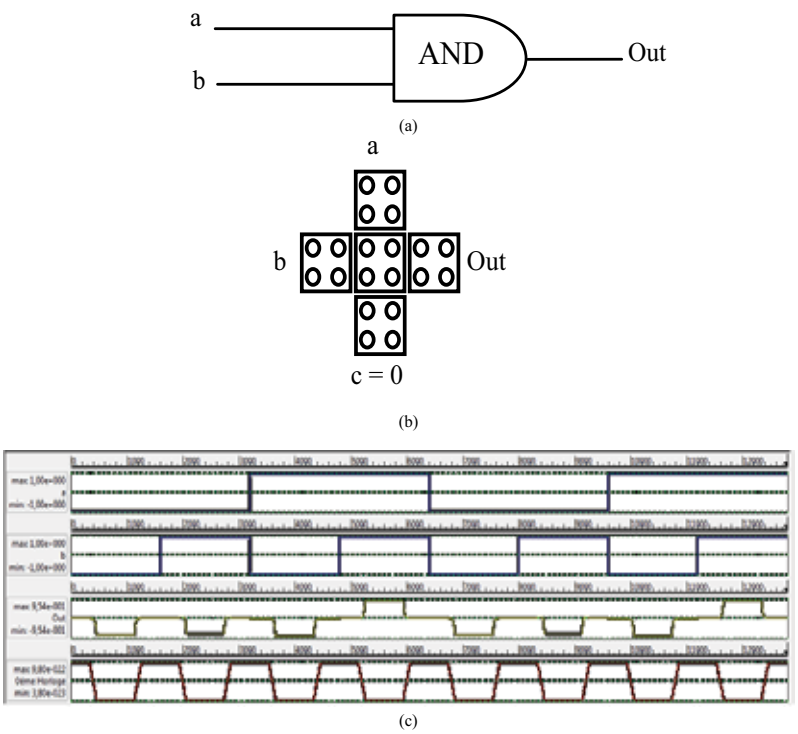


Figure 9. AND gate, (a) QCA representation, (b) QCA layout, and (c) simulation results.

From simulation results of the output pulses AND gate (yellow) given by **Figure 9(c)**, the expression of the inverter gate can be deduced as expressed in Eq. (7):

$$Out = \quad (a \;.\; b).\overline{Clk}\; 0 \tag{7}$$

5. Novel proposed QCA elements and gates

5.1. Proposed structure of 2-input digital "XNOR" gate

The 2-input logical "XNOR" gate is a hybrid circuit based on Inverter gate and "Exclusive-OR" gate. The schematic of a simple digital "XNOR" gate is presented in **Figure 10**. This circuit has two inputs: "c" and "d," and one output "K."

The truth table of this "XNOR" gate is shown in **Table 2**.

From **Table 2**, it can be deduced that when "c" and "d" are equal, the output "K" is equal to "1," and when "c" and "d" are different, the output "K" is equal to "0." Hence, the output "K" of the "Non-Exclusive-OR" ("XNOR") gate performs the following logic operation in Eq. (8):

$$K = \overline{c \oplus d} = \quad \overline{\overline{c}.d + c.\overline{d}} \tag{8}$$

In this chapter, a novel architecture of two-input "non-Exclusive-OR" gate using QCA implementation is proposed. It is defined by a higher density and a small number of cells.

This novel structure of 2-input "XNOR" gate is composed of two inputs "c," "d," and one fixed logic "0," with one output "K." The structure and the QCA layout of the proposed design are shown in **Figure 11**.

The simulation results of the proposed 2-input logical "XNOR" gate are shown in **Figure 12**. Four waveforms are applied to the inputs: c, d, Clk 0 and Clk 1. One waveform for the digital "XNOR" gate outputs (K). It can be deduced that there is 0.5 clock delay of latency on the novel proposed 2-input "XNOR" gate constituted only by 10 cells with an area of 0.006 μm^2.

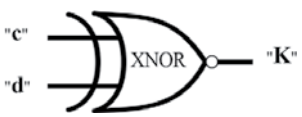


Figure 10. Schematic of 2-input "XNOR" gate.

c	d	K
0	0	1
0	1	0
1	0	0
1	1	1

Table 2. Truth table of 2-input "XNOR" gate.

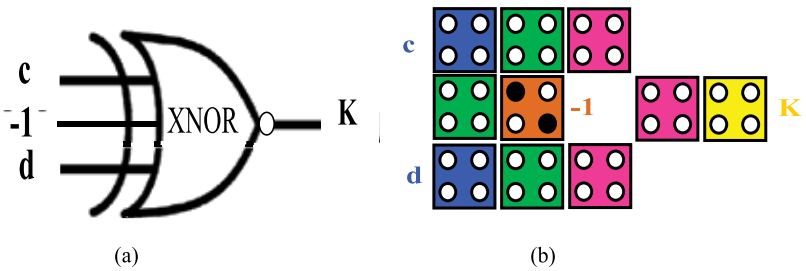


Figure 11. The novel architecture of 2-input "XNOR" gate structure, (a) schematic of "XNOR" gate and (b) QCA layout of proposed "XNOR" gate.

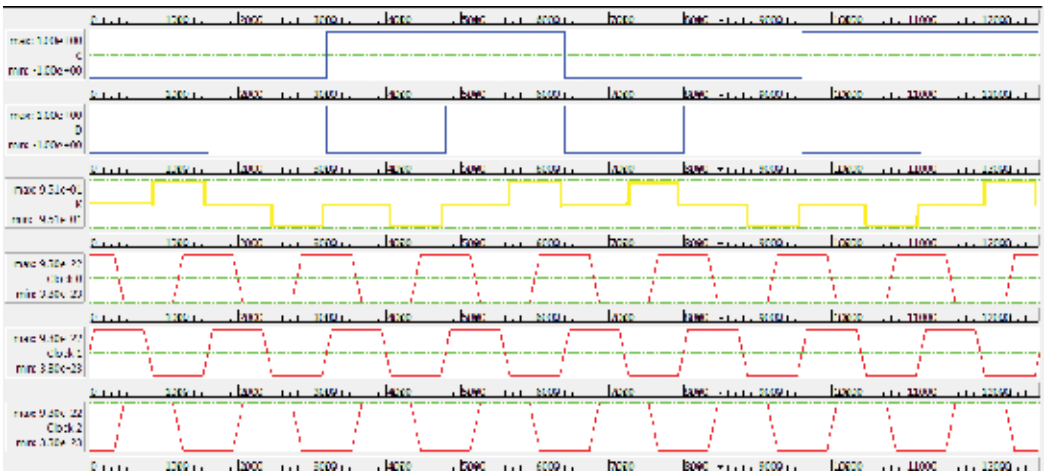


Figure 12. The simulation result of the novel design of 2-input logical "XNOR" gate.

5.2. Proposed structure of 3-input digital "XNOR" gate

The 3-input logical "XNOR" gate is adapted of 2-input logical "XNOR" gate. The schematic of this digital "XNOR" gate is presented in **Figure 13**. This circuit has four inputs: "c," "d," "e," and one output "K."

The truth table of this 3-input "non-Exclusive-OR" gate is shown in **Table 3**.

From **Table 3**, it can be deduced that when the number of the input "1" is odd, the output "K" is equal to "0." In the case of the number of the input "1" is even, the output "K" is equal to "1." Hence, the output "K" of the XNOR gate can determine the parity and is given by the following logic operation in Eq. (9):

$$K = \overline{c \oplus d \oplus e} \tag{9}$$

The simulation results of the proposed 3-input logical "XNOR" gate are shown in **Figure 14**. Three waveforms are applied to the inputs (c, d, and e) with the clock 0, clock 1, and one

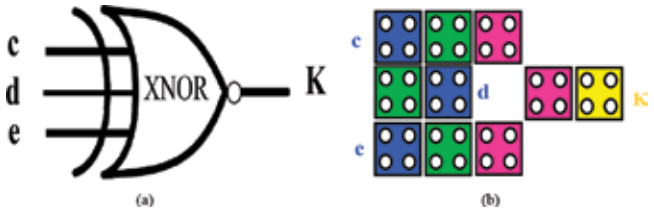


Figure 13. Schematic of 3-input "XNOR" gate. (a) Schematic of "XNOR" gate and (b) QCA layout of proposed "XNOR" gate.

c	d	e	k
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	

Table 3. Truth table of 3-input "XNOR" gate.

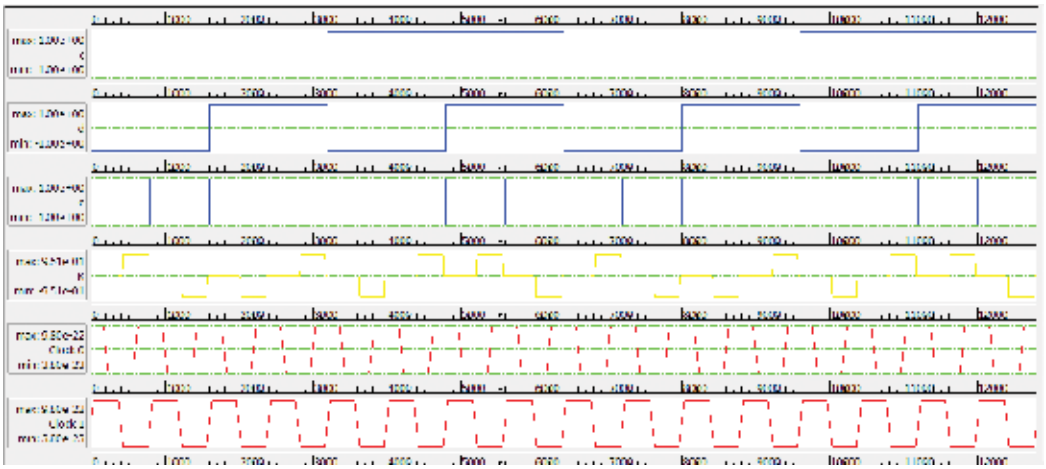


Figure 14. The simulation result of the novel architecture of 3-input logical "XNOR" gate.

waveform for the digital 3-input "XNOR" gate outputs (K). It can be deduced that there is 0.5 clock of latency on this novel proposed architecture 3-input "XNOR" gate constituted by 10 cells and with an area of 0.006 μm^2.

5.3. Proposed architecture of 2-input "XOR" gate

The 2-input logical "XOR" gate is a hybrid circuit, which is designed from 2-input logical "XNOR" gate. The schematic of "XOR" gate is presented in **Figure 15**. This circuit has two inputs: "c" and "d," and one output "K."

The truth table of this 2-input "Exclusive-OR" gate is shown in **Table 4**.

From **Table 4**, it can be deduced that when "c" and "d" are different, the output "K" is equal to "1," and when "c" and "d" are equal, the output "K" is equal to "0." Hence, the output "K" of the "Exclusive-OR" ("XOR") gate performs the following logic operation in Eq. (10):

$$K = c \oplus d = \ \bar{c} \ . \ d + c \ . \ \bar{d} \tag{10}$$

This novel design of 2-input "XOR" gate is composed of two inputs "c" and "d," and one fixed logic "0," with one output "K." The structure and the QCA layout of the proposed 2-input "XOR" gate are shown in **Figure 16**.

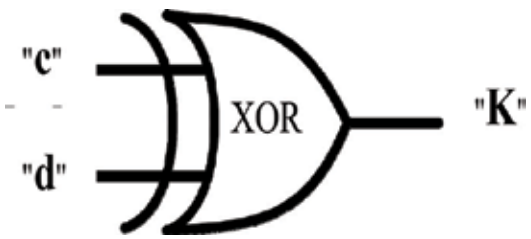


Figure 15. Schematic of 2-input "XOR" gate.

c	d	K
0	0	0
0	1	1
1	0	1
1	1	0

Table 4. Truth table of 2-input "XOR" gate.

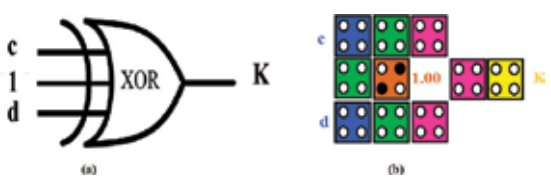


Figure 16. The architecture of novel design 2-input "XOR" gate structures: (a) schematic of 2-input "XOR" gate and (b) QCA layout of proposed 2-input "XOR" gate.

The simulation results of the proposed architecture of 2-input "XOR" gate are presented in **Figure 17**. Two waveforms are applied to the inputs (c and d), the clock 0, clock 1 and one waveform for "XOR" gate output (K). From **Figure 11**, it can be deduced that there is 0.5 clock of latency on this novel 2-input "XOR" gate, which is constituted by 10 cells with an area of 0.006 μm^2.

The proposed 2-input XOR circuit has lower computational complexity and better performances compared to the existing ones [27–31]. **Table 5** shows the comparison results of the proposed design for the XOR with the existing designs.

5.4. Proposed structure of 3-input "XOR" gate

The 3-input logical "XOR" gate is an adapted form of 3-input logical "XNOR" gate. The schematic of this digital "XOR" gate is presented in **Figure 18**. This circuit has only four inputs: "c," "d," "e," and one output "K."

The truth table of this 3-input "Exclusive-OR" gate is shown in **Table 6**.

From **Table 6**, it can be deduced that when the number of the input "1" is even, the output "K" is equal to "0". When the number of the input "1" is odd, the output "K" is equal to "1." Hence, the output "K" of the XNOR gate can determine the parity and is given by the following logic operation in Eq. (11):

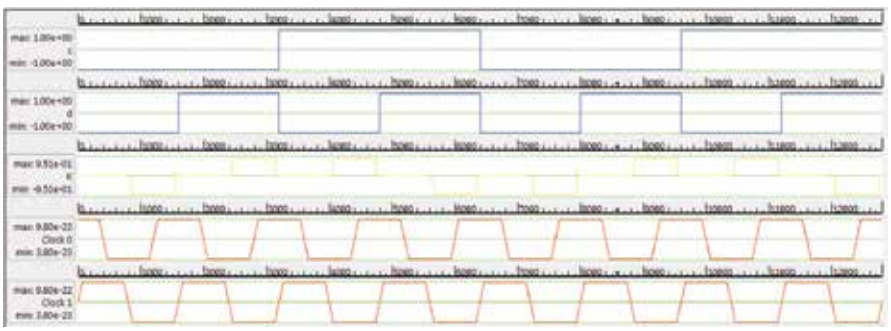


Figure 17. The simulation result of the novel structure of 2-input "XOR" gate.

Design	Cell count	Area (μm^2)	Latency
2-input XOR gate [27]	67	0.06	1.25
2-input XOR gate [28]	32	0.02	1
2-input XOR gate [29]	28	0.02	0.75
2-input XOR gate [30]	30	0.0233	0.75
2-input XOR gate [31]	12	0.0116	0.5
Proposed 2-input XOR	12	0.006	0.5

Table 5. Comparison results of single layer 2-input XOR gates.

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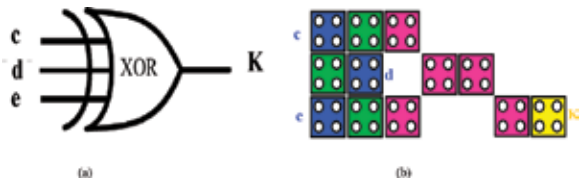

Figure 18. The architecture of novel design 2-input "XOR" gate structures: (a) schematic of 2-input "XOR" gate and (b) QCA layout of proposed 2-input "XOR" gate.

c	d	e	k
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Table 6. Truth table of 3-input "XOR" gate.

$$K = c \oplus \quad d \oplus e \tag{11}$$

The simulation results of the proposed 3-input logical "XOR" gate are shown in **Figure 19**. Three different waveforms are applied to the inputs (c, d, and e), the clock 0 and clock 1 and one waveform for the digital 3-input "XNOR" gate outputs (K). It can be interpreted that there

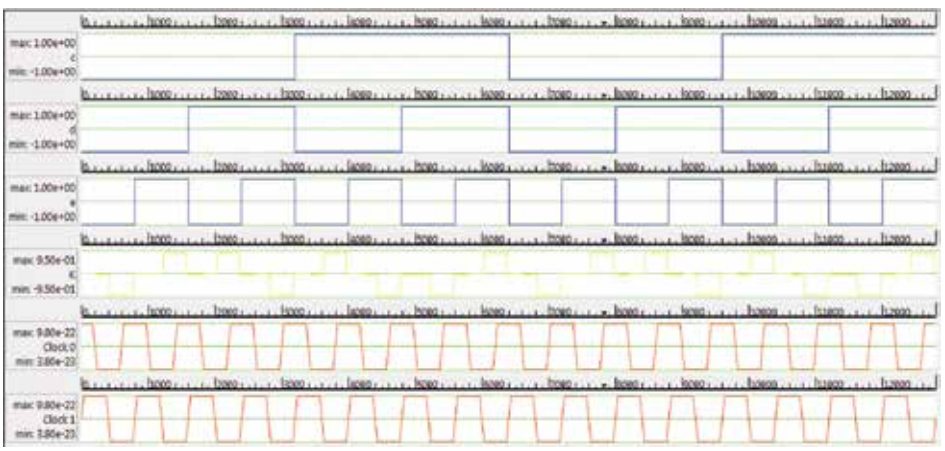

Figure 19. The simulation result of the novel architecture of 3-input "XOR" gate.

Design	Cell count	Area (μm^2)	Latency
3-input XOR gate [31]	12	0.0116	0.5
3-input XOR gate [27]	93	0.07	11.25
Proposed 3-input XOR gate	12	0.008	0.5

Table 7. Comparison results of single layer 3-input XOR gates.

is 0.5 clock of latency on this novel proposed structure of 3-input "XOR" gate, which is composed of 12 cells with an area of 0.008 μm^2.

Table 7 shows the comparison results of the proposed design for the 3-input XOR with the exist designs.

6. Conclusion

In this chapter, we have presented a QCA implementation of several fundamental basic elements and logic gates. Architectures and simulation results are also proposed. An important step in designing QCA circuits is reducing the number of required cells. The proposed method for the reduction of the number of cells in the QCA structure is based on the position of the electrons and the interaction forces between them. In the current proposed work, we have optimized the number of QCA cellule and reduced the wire crossings. Furthermore, this work may be extended to design other reversible QCA gates.

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Chapter 4

Millimeter-Wave Multi-Port Front-End Receivers: Design Considerations and Implementation

Chaouki Hannachi and Serioja Ovidiu Tatu

Additional information is available at the end of the chapter

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Abstract

This chapter covers recent achievements on the integrated 60 GHz millimeter-wave front-end receiver based on the multi-port (six-port) concept. For this purpose, the design procedure of a fully integrated 60 GHz multi-port (six-port) front-end receiver implemented on a thin ceramic substrate (ε_r = 9.9, h = 127 μm) using an miniature hybrid microwave integrated circuit (MHMIC) fabrication process is presented in detail. All components constituting the proposed front-end receiver including an 8 × 2 antenna array, a low-noise amplifier (LNA), a six-port circuit, and the RF power detectors are presented and characterized separately before they are integrated into the final front-end receiver prototype. The performance of the latter has been experimentally evaluated in terms of various M-PSK/M-QAM demodulations. The obtained demodulation results are very satisfactory (the constellation points for all considered M-PSK/M-QAM schemes are very close to the ideal locations), demonstrating and confirming the high ability of the proposed 60 GHz millimeter-wave six-port front-end receiver to operate as a high-performance quadrature demodulator, without any calibration, for modulation schemes up to 32 symbols.

Keywords: demodulation, front-end, low power, MHMIC, millimeter-wave, receiver, six-port, 60 GHz

1. Introduction

In 2001, the Federal Communications Commission (FCC) allocated several GHz in the frequency band around 60 GHz for unlicensed use. In fact, this unlicensed millimeter-wave frequency band is available in North America and Korea (57–64 GHz), as well as in Europe and Japan (59–66 GHz) [1, 2]. The main characteristic of this frequency band is the very high level of attenuation due to the extremely high atmospheric absorption (17 dB/Km), in addition

to higher loss in common building materials, which make 60 GHz communication most suitable for short-range wireless applications, several meters for low power to max 1 km for backhaul solutions. However, to operate reliably at even short ranges, 60 GHz communication systems must also employ a highly focused, narrow-beam antenna to increase the level of signal available to the target receiver.

Today, the demand for high-data-rate wireless communications and broadband transceiver/receiver systems with reduced hardware requirements and high flexibility is highly increased. However, the existing hardware architectures for radio communication systems suffer from a number of limitations including high cost, design complexity, as well as high power consumption. For instance, for most mixers in conventional receivers, to obtain a good conversion gain, the power of the local oscillator must be more than 10 dBm, which is a relatively high power level compared to other alternatives reported in literature [3]. Moreover, in conventional receiver systems, the phase noise of the local oscillator (LO) is transformed directly into the phase noise in the baseband. This results in neighbor channel interference, usually caused by reciprocal mixing, consequently decreasing the selectivity of the receiver [1].

Radio architectures having a potential to get beyond the previously mentioned limitations include radio communication systems based on multi-port architectures. The design simplicity combined with the wideband characteristics of multi-port receiver structures may provide RF receiver architectures, which can solve many of the current challenges of receiver systems. It provides a straightforward approach for broadband operations, low power consumption, and low manufacturing costs, making it a serious candidate for various indoor millimeter-wave wireless applications [4, 5].

In the recent years, several designs of multi-port (six-port) circuits have been investigated and presented in literature. They range from microstrips to LC lumped element designs, for different microwave and millimeter-wave frequency bands [6]. The first reported multi-port circuit was employed in the 1970s by Glenn F. Engen and Cletus A. Hoer as an alternative solution to network analyzers for the measurement of complex scattering parameters [7, 8]. A couple of years later, it was used in radar applications and has recently been proposed as an alternative to the conventional receiver architectures such as the homodyne and heterodyne receivers.

In this chapter, a fully integrated 60 GHz front-end receiver based on the multi-port (six-port) technique is presented and analyzed. All parts composing the proposed front-end receiver such as an 8×2 antenna array, a low-noise amplifier (LNA), a six-port circuit, and the power detectors are presented and characterized separately. This chapter is therefore organized as follows. First, Section 2 gives a comprehensive overview on the MHMIC fabrication process used to manufacture the proposed 60 GHz front-end receiver prototype. Next, Section 3 shows the theoretical concept of the six-port circuit and how it operates as an amplitude/phase discriminator; moreover, it describes in detail the basic building blocks of the designed 60 GHz front-end receiver. The experimental characterization procedure and the obtained measurement results, as well as the final fabricated front-end receiver prototype with the experimental M-PSK/M-QAM demodulation results are also discussed in the same section. Finally, a conclusion is drawn.

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2. MHMIC fabrication process

Today, there are few promising high-quality fabrication processes, offering potentially low-cost and highly integrated millimeter-wave components, such as the monolithic microwave integrated circuit (MMIC) based on GaAs, silicon, or SiGe technology for large-scale production and the miniature hybrid microwave integrated circuit (MHMIC) for prototyping or small-scale production [9]. The latter adopts a thin-film process in which a wide range of passive components are fabricated on an alumina substrate having typically a high dielectric constant. These components are not limited only to the basic lumped passive components such as thin-film resistors, spiral inductors, and overlay capacitors, but they also include a large number of RF passive circuits including power dividers, directional couplers, printed antennas, and filters. The active devices such as diodes, power amplifiers (PAs), and low-noise amplifiers (LNAs) are implemented at the end of the process, using gold wire bonding technology.

The most frequently used materials for the substrate metallization are gold, copper, or copper-gold. High-precision thin-film resistors are typically implemented using nichrome or tantalum nitride films on a thin-film ceramic substrate. However, various processing techniques are usually used, such as photolithography techniques, e-beam, and, more recently, the excimer laser micromachining [10].

It is to be noted that the choice of a thin substrate is due to the reduced guided wavelength in high-permittivity ceramic substrates. In order to keep the required circuit aspect ratio (the guided wavelength versus the line width), the substrate thickness has to be as thin as possible. The optimal choice for frequencies higher than 60 GHz is the 127-μm-thick alumina substrate that is commercially available. This substrate is also easily compatible with the regular 100-μm-thick MMIC active components, to be integrated with planar passive MHMICs. MMIC chips are implemented in rectangular cuts on ceramics, on the top of the same metallic fixture, allowing thermal dissipation and easy wire bonding with MHMIC components, which are typically at the same height.

The MHMIC technology represents today an excellent alternative for low-cost and rapid prototyping of highly miniaturized circuits with improved performances at millimeter-wave frequencies up to 86 GHz [6].

3. Multi-port (six-port) circuit-based front-end receivers

The six-port (multi-port) quadrature down-conversion is an innovative approach in millimeter-wave technology. A comprehensive theory, validated by various simulations and measurements of 60 GHz (V-band) direct conversion receivers, has been presented in literature over the recent years [11, 12].

The block diagram in **Figure 1** highlights the operation principle of a front-end receiver based on a six-port circuit to demodulate RF signals. This structure is composed of three 90° hybrid

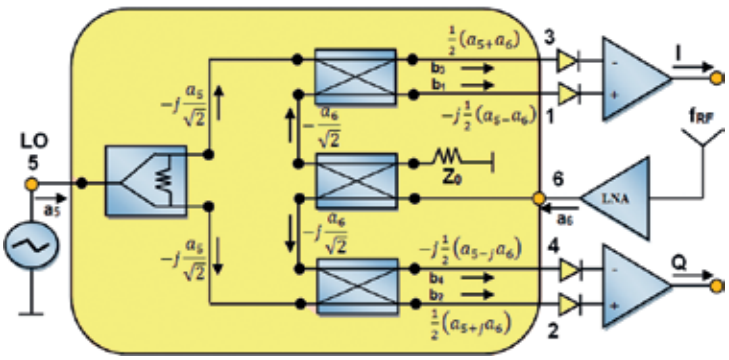

Figure 1. Block diagram of a six-port circuit-based front-end receiver.

couplers and a Wilkinson power divider. The proposed architecture makes possible to obtain, from output power measurements, the phase difference and the amplitude ratio between an unknown signal from the antenna (a_6) and the reference signal coming from a local oscillator (a_5).

The output signals b_i can be expressed as a function of the signals a_i and the S-parameter S_{ij} by the following linear relationship:

$$b_i = \sum_{j=1}^{6} S_{ij} a_j, \qquad i = 1, \ldots, 6 \tag{1}$$

The S_{ij} parameters of the six-port circuit can be obtained directly from **Figure 1**. For that purpose, the S-parameter matrices [S] of the 90° hybrid coupler and the Wilkinson power divider are employed. The corresponding matrices are given in Eqs. (2) and (3):

$$[S] = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{2}$$

$$[S] = -j\frac{1}{\sqrt{2}} \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{3}$$

Thus, the global S-parameter matrix [S] of the six-port circuit in **Figure 1** is obtained by Eq. (4):

$$[S] = \frac{1}{2} \begin{bmatrix} 0 & 0 & 0 & 0 & -j & j \\ 0 & 0 & 0 & 0 & 1 & j \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & -j & -1 \\ -j & 1 & 1 & -j & 0 & 0 \\ j & j & 1 & -1 & 0 & 0 \end{bmatrix} \tag{4}$$

Using Eq. (4), we may obtain the formulas of the four waveforms, b_1, b_2, b_3, and b_4, as a function of the two incident waves a_5 and a_6, as described in Eq. (5):

$$\begin{cases} b_1 = -j\dfrac{a_5}{2} + j\dfrac{a_6}{2} \\ b_2 = \dfrac{a_5}{2} + j\dfrac{a_6}{2} \\ b_3 = \dfrac{a_5}{2} + \dfrac{a_6}{2} \\ b_4 = -j\dfrac{a_5}{2} - \dfrac{a_6}{2} \end{cases} \tag{5}$$

In order to simplify calculations, we assume that the RF signals resulting from the antenna a_6 and the local oscillator (LO) a_5 have an amplitude ratio α, a phase difference $\Delta\varphi(t) = \varphi_6(t) - \varphi_5$, and a frequency difference $\Delta\omega = \omega - \omega_0$ ($\omega = 2\pi f$). Therefore, these signals can be expressed by the following equations [11]:

$$a_5 = a \cdot e^{j\left(\omega_0 \cdot t + \varphi_5\right)} \tag{6}$$

$$a_6 = \alpha \cdot a \cdot e^{j\left(\omega_0 \cdot t + \varphi_6(t)\right)} = \alpha \cdot a_5 \cdot e^{j(\Delta\omega \cdot t + \Delta\varphi(t))}. \tag{7}$$

By replacing the expressions of signals a_5 and a_6 in the system of Eq. (5), we obtain

$$b_1(t) = -j\frac{a}{2} \cdot e^{j\left(\omega_0 t + \varphi_5\right)} \cdot \left[1 + \alpha \cdot e^{j(\Delta\omega \cdot t + \Delta\varphi(t) + \pi)}\right] \tag{8}$$

$$b_2(t) = \frac{a}{2} \cdot e^{j\left(\omega_0 t + \varphi_5\right)} \cdot \left[1 + \alpha \cdot e^{j\left(\Delta\omega \cdot t + \Delta\varphi(t) + \frac{\pi}{2}\right)}\right] \tag{9}$$

$$b_3(t) = \frac{a}{2} \cdot e^{j\left(\omega_0 t + \varphi_5\right)} \cdot \left[1 + \alpha \cdot e^{j(\Delta\omega \cdot t + \Delta\varphi(t))}\right] \tag{10}$$

$$b_4(t) = -j\frac{a}{2} \cdot e^{j\left(\omega_0 t + \varphi_5\right)} \cdot \left[1 + \alpha \cdot e^{j\left(\Delta\omega \cdot t + \Delta\varphi(t) - \frac{\pi}{2}\right)}\right] \tag{11}$$

It should be noted that the signals at the intermediate frequency (IF) band are the results of connecting the four six-port circuit outputs to the power detectors (see **Figure 1**). We consider that the power delivered at the output of each ideal power detector is proportional to the square of the RF signal magnitude [11, 13]. Under these conditions

$$v_i = K_i \cdot |b_i|^2 = K_i \cdot b_i \cdot b_i^*, \qquad i = 1, \ldots, 4 \tag{12}$$

Given that the power detectors are identical ($K_i = K$), then

$$v_1(t) = K\frac{a^2}{4} \cdot \left\{1 + \alpha^2 - 2 \cdot \alpha \cdot \cos\left[\Delta\omega \cdot t + \Delta\varphi(t)\right]\right\} \tag{13}$$

$$v_2(t) = K\frac{a^2}{4}\cdot\left\{1 + \alpha^2 - 2\cdot\alpha\cdot\sin\left[\Delta\omega\cdot t + \Delta\varphi(t)\right]\right\} \tag{14}$$

$$v_3(t) = K\frac{a^2}{4}\cdot\left\{1 + \alpha^2 + 2\cdot\alpha\cdot\cos\left[\Delta\omega\cdot t + \Delta\varphi(t)\right]\right\} \tag{15}$$

$$v_4(t) = K\frac{a^2}{4}\cdot\left\{1 + \alpha^2 + 2\cdot\alpha\cdot\sin\left[\Delta\omega\cdot t + \Delta\varphi(t)\right]\right\} \tag{16}$$

In order to generate quadrature signals IF/IQ, we use differential amplifiers in the intermediate frequency band, at outputs 1, 3, and 2, 4 (see **Figure 1**):

$$v_{IF}^{I}(t) = A_{IF}\cdot[v_3(t) - v_1(t)] = \alpha\cdot K\cdot a^2\cdot A_{IF}\cdot\cos\left[\Delta\omega\cdot t + \Delta\varphi(t)\right] \tag{17}$$

$$v_{IF}^{Q}(t) = A_{IF}\cdot[v_4(t) - v_2(t)] = \alpha\cdot K\cdot a^2\cdot A_{IF}\cdot\sin\left[\Delta\omega\cdot t + \Delta\varphi(t)\right] \tag{18}$$

A second frequency conversion followed by low-frequency filtering is performed. The I/Q baseband signal formulas are thus obtained:

$$I(t) = \frac{1}{2}\cdot\alpha\cdot K\cdot a^2\cdot A_{IF}\cdot A_{BB}\cdot\cos\left[\Delta\varphi(t)\right] \tag{19}$$

$$Q(t) = \frac{1}{2}\cdot\alpha\cdot K\cdot a^2\cdot A_{IF}\cdot A_{BB}\cdot\sin\left[\Delta\varphi(t)\right] \tag{20}$$

In fact, the baseband I/Q signal can be expressed in the complex plane by the following equation:

$$\Gamma(t) = I(t) + Q(t) = \frac{1}{2}\cdot\alpha\cdot K\cdot a^2\cdot A_{IF}\cdot A_{BB}\cdot e^{j\Delta\varphi(t)} \tag{21}$$

This expression shows that the terms A_{IF} and A_{BB} are related to the intermediate frequency (IF) band and baseband (BB) amplification. The receiver works in both architectures: heterodyne, according to Eqs. (17) and (18), and homodyne, according to Eqs. (19) and (20). The amplitude ratio α and the phase difference, $\Delta\varphi(t) = \varphi_6(t) - \varphi_5$, can be obtained in baseband. This relationship between the RF domains and the intermediate (IF) band as well as the baseband has highlighted the role of the six-port circuit (reflectometer) as a phase, frequency, and amplitude discriminator [11].

3.1. Multi-port (six-port) circuit design and characterization

A broadband six-port circuit with an improved symmetry and rounded shapes has been designed on a thin alumina substrate (ε_r = 9.9 and h = 127 μm) using the novel Wilkinson power divider/combiner and the three rounded 90° hybrid couplers [9]. The central design frequency is 60.5 GHz, in the center of an unlicensed frequency band (57 to 64 GHz).

It should be noted that all measurements are performed from 60 GHz, due to the available measurement setup capabilities (WR-12 rectangular waveguide modules for the 60–90 GHz

millimeter-wave extension of the VNA). However, extrapolation of measurements and comparison with simulations allow assessing the circuit behavior from 57 to 60 GHz. The microphotograph in **Figure 2(a)** shows the fabricated six-port circuit ready for port 4 to port 5 measurements using a coplanar line to microstrip transition and a precise on-wafer measurement structure equipped with ground-signal-ground (GSG)-150 μm coplanar probes, as shown in **Figure 2(b)**.

As can be seen in **Figure 2(a)**, all remaining ports are terminated by matched loads (50 Ω), integrated on the same substrate using a 100 Ω per square titanium oxide thin layer. In order to avoid the metalized via holes that are complicated to achieve with accuracy and repeatability at millimeter-wave frequencies, the 50 Ω loads use a quarter wavelength open stubs as millimeter-wave RF short circuits (see ports 1, 2, 3, and 4). The outer six-port dimensions are more or less 6.5 mm by 6.5 mm.

In order to ensure the accuracy of S-parameter measurements, the on-wafer through-reflect-line (TRL) calibration technique is employed, using the calibration kits on the same ceramic alumina substrate as the devices under test (DUT) [9]. Its standards are shown in **Figure 3**. It consists of a thru line (T), two open circuits as reflect (R), and a short line (L). Due to the fragility of the very thin gold layer metallization (1 μm), multiple identical standards are designed on the same ceramic substrate to ensure repeatability and success of on-wafer calibrations and S-parameter measurements.

Figure 4 shows the typical return loss measurement at port 6 (RF input) and port 5 (LO input), as well as the isolation between them. As can be seen, at the center operating frequency, around 60 GHz, all values are better than 20 dB. Moreover, the measured values are better than 15 dB at the highest frequency (64 GHz) of the unlicensed frequency band. In fact, the achieved high isolation level is a result of employing a highly isolated round-shaped Wilkinson power divider with a high-precision integrated resistor, which has been implemented with accuracy on the 100 Ω per square titanium oxide thin layer, using MHMIC technology [14], as described earlier.

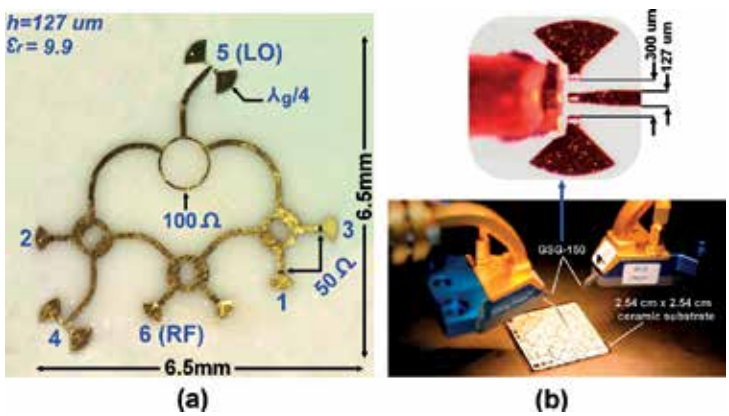

Figure 2. Microphotograph of the fabricated millimeter-wave six-port circuit: (**a**) the on-wafer S-parameter measurement configuration and (**b**) the on-wafer S-parameter measurement process using GSG-150 μm coplanar probes.

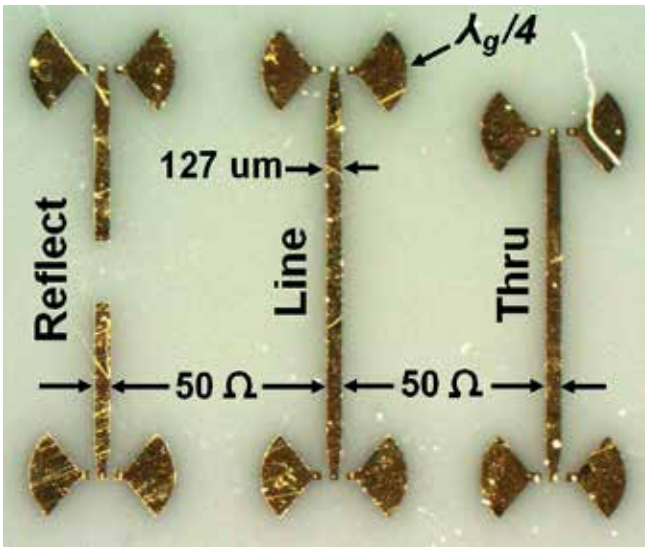

Figure 3. Microphotograph of TRL calibration kit.

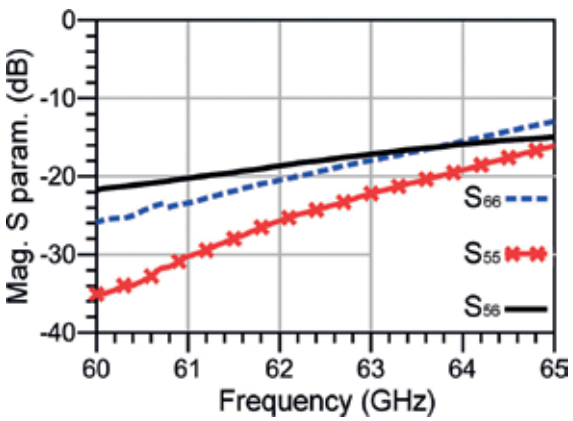

Figure 4. Measured RF inputs return loss and isolation for the fabricated six-port circuit.

The measured return losses at output ports (1, 2, 3, and 4) are illustrated in **Figure 5**. These results exhibit a good matching at all ports, with better than 25 dB around the operating frequency of 60 GHz while keeping a good matching level for the rest of the band (better than 15 dB at the highest frequency (64 GHz)).

Figure 6 shows the measured transmission coefficient results, commonly known as the power splitting between the LO port 5 and two adjacent outputs (ports 2 and 4), as well as between the RF port 6 and two other adjacent outputs (ports 1 and 3). As can be seen, the measured transmission coefficients are close to the value of −6 dB over the considered frequency band, according to the six-port theory. However, around the center frequency of 60 GHz, the

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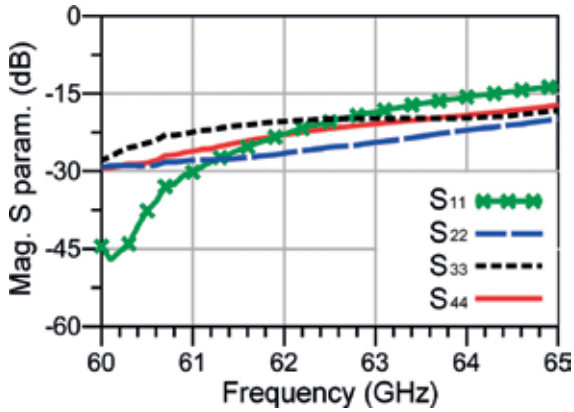

Figure 5. Measured RF outputs return loss (ports 1, 2, 3, and 4) for the fabricated six-port circuit.

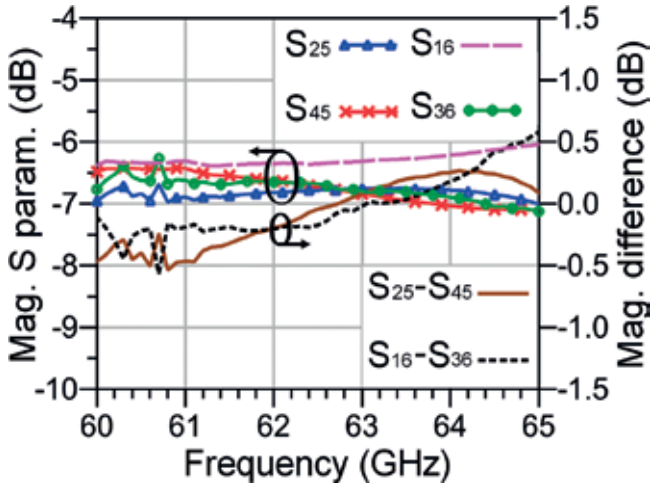

Figure 6. Typical transmission magnitude measurements for the fabricated six-port circuits.

maximum supplementary insertion loss does not exceed 0.6 dB, reaching approximately 1.2 dB at the upper edge. The magnitude unbalance between two pairs of outputs is close to 0 dB at 62.5 GHz and is less than 0.5 dB over the frequency band of interest. It should be noted that due to the high symmetry of the designed circuit, similar results are obtained between port 5 and the other two six-port outputs (1, 3). The same is valid for the transmission coefficient results between RF port 6 and outputs (2, 4).

Figure 7 shows the phase difference between the two typical transmission S-parameters, S_{52} and S_{54}, as well as S_{61} and S_{63}. The obtained results show two quasi-parallel characteristics. The measured phase difference between each two adjacent ports is close to the quadratic reference of 90°. However, the observed phase difference error is less than ±2° up to 64 GHz.

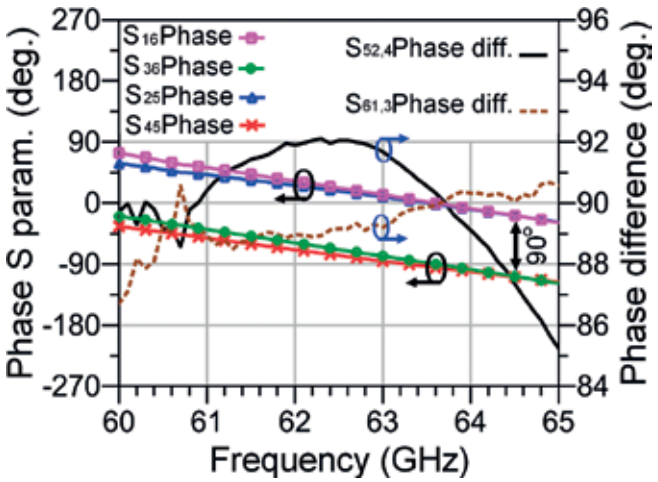

Figure 7. Typical transmission phase measurements for the fabricated six-port circuits.

The plot of the q_i points using the S-parameter measurement results of the proposed six-port circuits is shown in **Figure 8**. As can be seen, the q_i points are positioned equidistantly from the origin and angularly spaced by 360° divided their number (i = 4 in this case). These results underline the performance of the fabricated six-port circuit and prove the high accuracy location of the q_i points over the considered 60 GHz frequency band. Consequently, the magnitudes of the q_i points are equal and closer to 1, while the argument difference is closer to 90° between two corresponding q_i points.

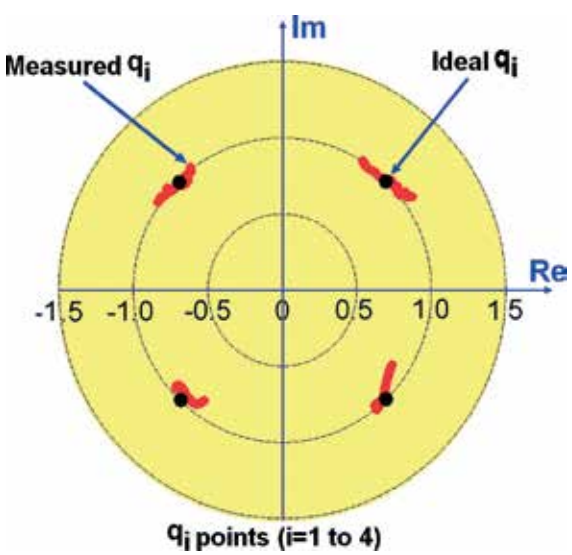

Figure 8. The q_i points of the fabricated six-port circuit for the considered frequency band 60–65 GHz.

3.2. Millimeter-wave power detector design and characterization

As we have seen in the previous section, to recover the low IF or the baseband signals, the implementation of power detectors at the four outputs of the six-port circuit is required. For that purpose, the HSCH-9161 millimeter-wave zero-bias GaAs Schottky diode of Keysight Technologies is selected for power detection, due to its broadband and high-speed properties [15, 16]. The typical configuration of the power detector usually includes the Schottky diode followed by a low-pass filter to extract the DC component, as illustrated in **Figure 9**.

The nonlinear characteristic between the current $i(t)$ that passes through the diode and the input RF voltage $V_{RF}(t)$ is generally described by the Schottky law. By neglecting the parasitic resistance of the diode, this characteristic will be expressed by

$$i(t) = I_s\left[\exp\left(\frac{q_o v_{RF}(t)}{nKT}\right) - 1\right] \tag{22}$$

where I_s is the saturation current, q_o is the charge of the electron, n is the coefficient of ideality, K is the Boltzmann constant, and T is the temperature.

Knowing that the voltage V_{RF} (t) can be expressed by

$$v_{RF}(t) = A\cdot\cos(\omega_{RF}t), \quad \omega_{RF} = 2\pi f_{RF} \tag{23}$$

On the other hand, considering that the input signal V_{RF} (t) has a low power and that it satisfies the condition, $A < V_T$, then we can reexpress Eq. (22) by using the limited development of the exponential function to obtain

$$i(t) = I_s\left[\left(\frac{v_{RF}(t)}{nV_T}\right) + \frac{1}{2}\left(\frac{v_{RF}(t)}{nV_T}\right)^2 + \ldots\right] \tag{24}$$

Moreover, the low-frequency equivalent circuit at the output of the power detector may be presented as follows (**Figure 10**) [16]:

The dynamic resistance of the diode R_V represents the video resistance [16]. The latter with the resistor R and the capacitor C forms a first-order low-pass filter having a cutoff frequency f_c:

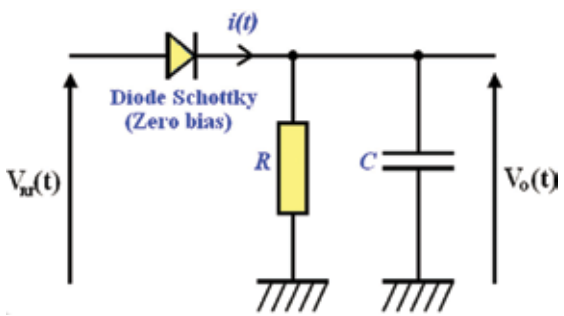

Figure 9. Typical configuration of a zero-bias Schottky diode-based power detector.

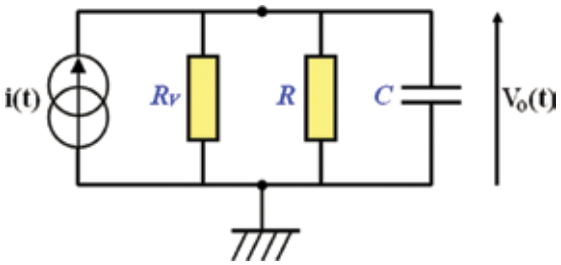

Figure 10. Equivalent circuit for the output of the Schottky diode-based power detector.

$$f_c = \frac{R_v + R}{2\pi R_v RC} \tag{25}$$

By choosing a low-frequency cutoff f_c compared to the RF input frequency of the power detector, the output voltage V_o(t) will therefore be proportional to the low-frequency or baseband (BB) components of the current *i(t)*, particularly to the quadratic term of Eq. (24).

Then, by replacing the expression of the input RF voltage given by Eq. (23) in Eq. (24) and taking into account only the quadratic term of the equation, we obtain

$$i(t) = \frac{I_S}{2}\left(\frac{A\cdot\cos\left(2\pi f_{RF}t\right)}{V_T}\right)^2 \tag{26}$$

After a low-pass filtering operation, the output voltage will be expressed as follows:

$$v_o(t) = \frac{R\cdot R_V}{R + R_V}\left(\frac{I_S}{4{V_T}^2}\right)^2\cdot A^2 = \alpha\cdot P_{RF} \tag{27}$$

The coefficient α represents the sensitivity of the power detector, usually expressed in volts/watt. According to the formula, it can be seen that for the low power levels, the detector can perform power detection because the output voltage of the detector is proportional to the square of the input signal amplitude or, in other words, to the power of the RF signal.

The photograph of the fabricated millimeter-wave power detector circuit used in the proposed front-end receiver architecture is shown in **Figure 11**. It comprises three main parts: the input impedance matching circuit, an HSCH-9161 millimeter-wave GaAs Schottky diode (zero bias), and the detected DC voltage output circuit. Obviously, all parts are designed and implemented on a thin ceramic substrate (ε_r = 9.9, h = 127 μm), using an MHMIC fabrication process. The input of the diode is well matched to 50 Ω using an accurate impedance matching stage to achieve the maximum transmission of the RF signal to diode input. The proposed impedance matching networks include an open-circuit stub of 0.16λ in parallel with the main 50 Ω microstrip line for matching purposes, as well as quarter-wave length-paralleled radial stubs attached to a metalized via-hole through a high-impedance quarter-wave length microstrip line, to prevent the RF signal leakage, providing DC ground. The integrated high-precision resistors of 100 Ω (parallel) are implemented on a 100 Ω per square titanium oxide thin layer

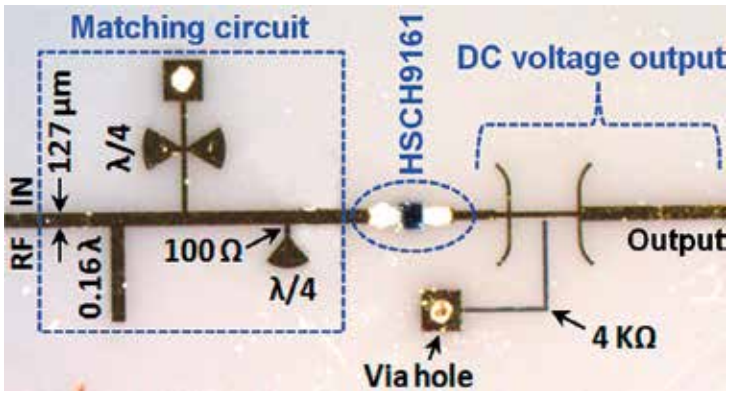

Figure 11. Photograph of the fabricated power detector prototype.

and have the role of providing resistive input impedance that enables broadband operation [15]. The quarter-wave length radial stub provides RF ground.

At the diode output, a broadband low-pass filtering made from two pairs of quarter-wave reflectors has been performed. This operation allows extraction of the DC voltage signals while suppressing all undesired higher-frequency components. In order to maximize the output detection voltage, a high-impedance integrated grounded resistor of 4 KΩ has also been added at the diode detector output. It uses the same 100 Ω per square titanium oxide thin layer.

The simulated and measured return loss at the RF input of the fabricated power detector circuit is compared, with good agreement, in **Figure 12**. As can be observed, the measured impedance bandwidth at −10 dB covers the frequency range of 3.8 GHz, from 60 to 63.8 GHz, which represents a bandwidth of 6.13%, at the center frequency of 61.9 GHz.

The simulated and the measured results of output power versus input power, at 61.9 GHz, are shown in **Figure 13**. As can be seen, a good concordance is achieved between measurement and simulation based on the diode model using the Keysight's Advanced Design System

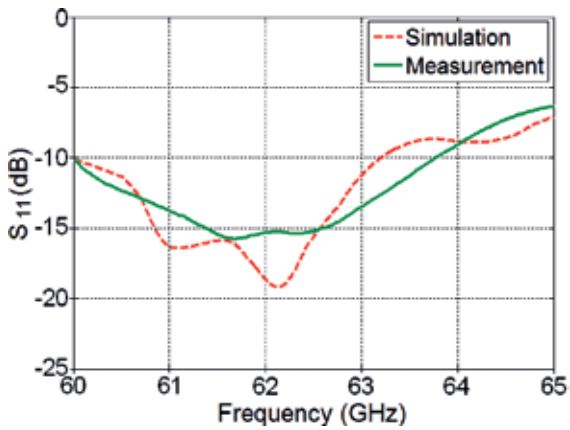

Figure 12. Simulated and measured return loss of the fabricated millimeter-wave power detector.

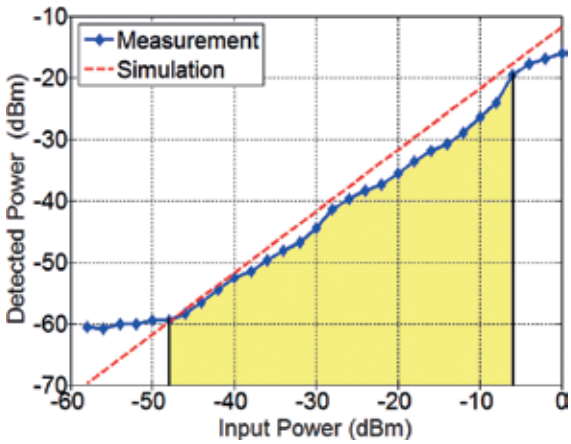

Figure 13. Simulated and measured detected power versus input power at 61 GHz.

(ADS) software. The proposed power detector shows a measured dynamic range (detection range) in the linear region of more than 42 dB. A high sensitivity is also achieved; the minimum detectable input power level using digital voltmeter is approximately −48 dBm.

3.3. V-band low-noise amplifier (LNA) implementation

A low-noise amplifier (LNA) represents the head amplifier of the receiving chain. It is often mounted as close as practical to the antenna, in order to amplify signals having a very low power level. However, the amplification of the signal received by the amplifier must meet two important criteria: maintain a stable and appropriate gain and control the noise figure (NF) of the receiver. In other words, a trade-off between the noise factor and the gain is therefore necessary in the LNA design. Generally, the noise factor F describes the signal-to-noise ratio degradation caused by the RF chain components. It is defined as the ratio of the input SNR (signal-to-noise ratio) to the output SNR of the receiver system:

$$SNR = \frac{SNR_{IN}}{SNR_{OUT}} \tag{28}$$

In the designed front-end receiver prototype, the low-noise amplifier TGA4600 from TriQuint Semiconductor company has been selected. The latter has a reasonable noise factor, NF = 4 dB, allowing to significantly limit the noise contribution of the reception chain. The typical implementation of the employed low-noise amplifier with gold bonding wires and ribbons on a ceramic substrate is illustrated in a photograph of **Figure 14**. Typical characteristics at 60 GHz are also presented in **Table 1**.

3.4. Millimeter-wave microstrip antenna array design

Millimeter-wave microstrip patch antennas are a promising alternative to the future wireless communication technologies in various fields including military, industrial, and commercial [17]. This is primarily due to their small size, low cost, and light weight, as well as the ease of

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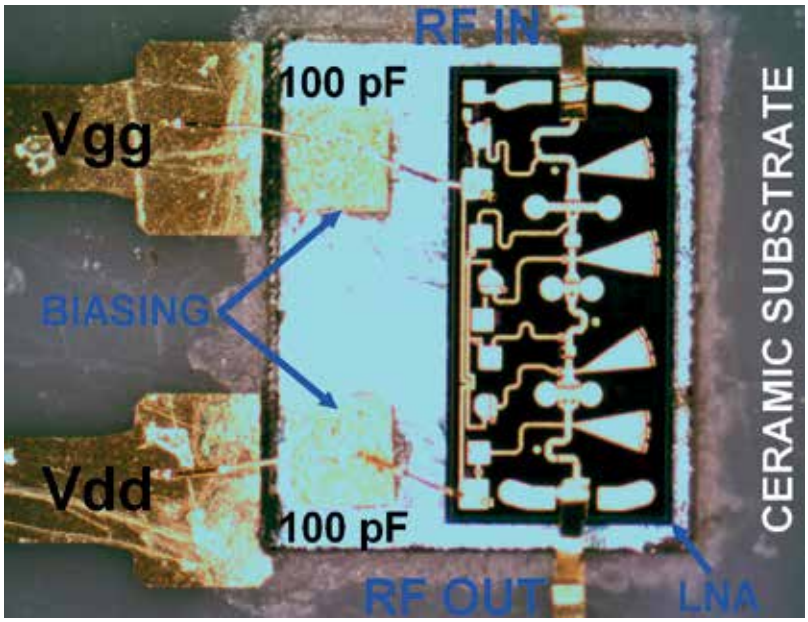

Figure 14. Photograph of typical low-noise amplifier TGA4600 implementation on a thin ceramic substrate.

Technology	0.15 μm 3MI pHEMT
NF	4 dB
Gain	13 dB
Typical frequency range	57–65 GHz
Input/output impedance	50 Ω
Input/output return loss	26 dB/6 dB
Reverse isolation	20 dB
Stability factor	>1

Table 1. Typical characteristics of TGA4600 low-noise amplifier at 60 GHz.

fabrication and integration with any planar fabrication technology, such as the miniature hybrid microwave integrated circuit (MHMIC) or the monolithic microwave integrated circuit (MMIC) [18].

In this section, a high-gain 8 × 2 element microstrip patch antenna array has been designed to be integrated in the proposed 60 GHz millimeter-wave RF front-end receiver prototype, for high-data-rate indoor wireless applications. The proposed array configuration was simulated using the Advanced Design System (ADS) software from Keysight Technologies and tested using the vector network analyzer (E8362B) with millimeter-wave extension modules of the same company.

The geometry of the fabricated microstrip 8 × 2 antenna array, including its single patch element, is shown in the photograph at **Figure 15**. The proposed array architecture adopts a corporate feed network connected to a 50 Ω coplanar feed line to carry out on-wafer measurements through ground-signal-ground (GSG)-150 μm coplanar probes. The employed corporate microstrip feed network includes a Wilkinson power divider/combiner and multiple tee junctions, which are interconnected by microstrip lines of 50 Ω and 70.7 Ω characteristic impedances to allow impedance matching, as well as better control over the phase and amplitude of each single patch element. This approach provides high directivity, improves radiation efficiency, and reduces beam fluctuations, over the suggested frequency range, compared to other array configurations [17]. The geometrical parameters of the proposed antennas are Wa = 18.56 mm, La = 5.01 mm, W = 1.07 mm, L = 0.74 mm, d = 1.43 mm, and d_1 = 1.60 mm.

The simulated and measured return losses of the single patch antenna, as well as the 8 × 2 microstrip array, are compared in **Figure 16**. As can be seen, good concordances are achieved

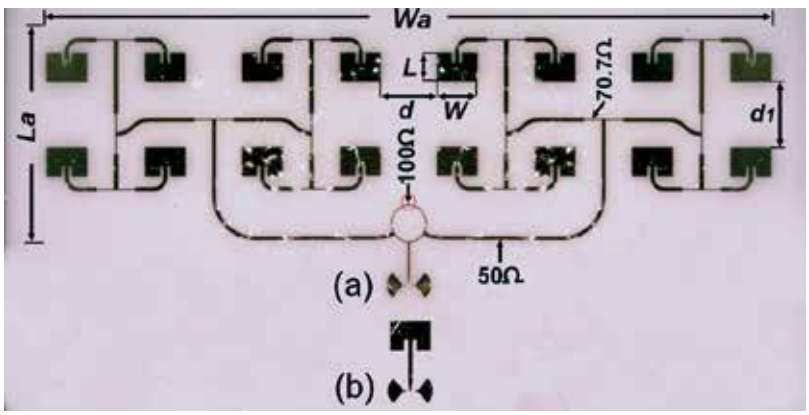

Figure 15. Photograph of the fabricated prototype with the geometrical parameters of (**a**) the 8 × 2 microstrip array antenna and (**b**) the single patch.

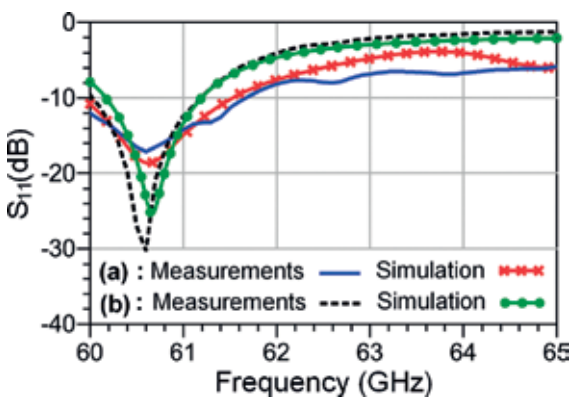

Figure 16. Measured and simulated return loss of (**a**) the 8 × 2 microstrip array antenna and (**b**) the single patch.

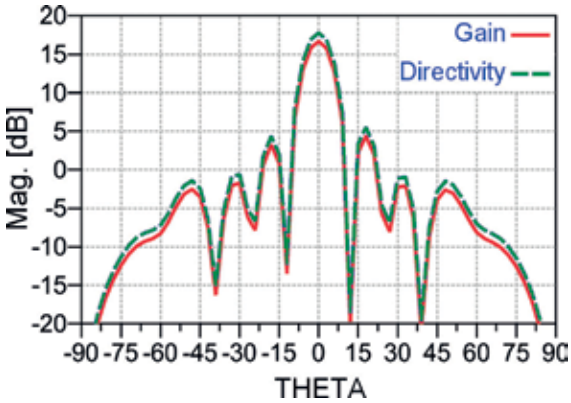

Figure 17. 2D simulated radiation pattern of the proposed 8 × 2 microstrip antenna array at 60.5 GHz.

over the considered frequency range (60–65 GHz). However, the −10 dB antenna bandwidths cover from 60 GHz to 61.2 GHz for the single patch and from 60 GHz to 61.7 GHz for the 8 × 2 microstrip array, which represent, respectively, bandwidths of 1.2 GHz (2%) and 1.7 GHz (2.83%), respectively.

The simulated 2D radiation pattern in E-plane at 60.5 GHz is illustrated at **Figure 17**. As can be observed, the simulated radiation pattern maintains a high symmetry and a good broadside radiation pattern. The maximum gain and directivity are 16.8 dB and 17.9 dB, respectively. The simulated antenna efficiency is around 77.43%. The half-power beamwidth (HPBW) is about 12°, and the first-side lobe is about 12.8 dB below the main lobe.

3.5. Millimeter-wave multi-port (six-port) front-end receiver implementation

In this section, we assemble all the components detailed above to form the final prototype of the fully integrated 60 GHz front-end receiver. The latter is shown in photograph at **Figure 18**. It therefore includes an 8 × 2 antenna array, a low-noise amplifier (LNA), a six-port circuit, and power detectors, integrated on a same 2.54 cm × 2.54 cm ceramic substrate. In summary, its function and principle of operation are as follows: the RF signal enters at port 6, after being received by a 16-element patch antenna array (16.8 dB Gain) and amplified by the TGA4600 LNA from TriQuint Semiconductor (57–65 GHz, 13 dB Gain, and 4 dB noise figure). The reference signal from the local oscillator (LO) enters at port 5 through a microstrip to WR12 rectangular waveguide (RW) transition. In order to recover the low IF or the baseband signals, the four six-port outputs are connected to the RF power detectors.

The fabricated 60 GHz six-port front-end receiver has been tested using the test bench illustrated in the block diagram of **Figure 19** and the corresponding photograph at **Figure 20**. In the transmitting part, the HP 8360 Series Synthesized Sweeper output is connected to a commercial K-Band power amplifier with a gain of around 10 dB. Limited by the upper output frequency range of the frequency synthesizer (40 GHz), an additional millimeter-wave frequency multiplier module (x3), model SFP-123KF-S1, from SAGE Millimeter, Inc., is then used to achieve a frequency around 61.71 GHz (20.57 GHz × 3). The obtained signal is combined

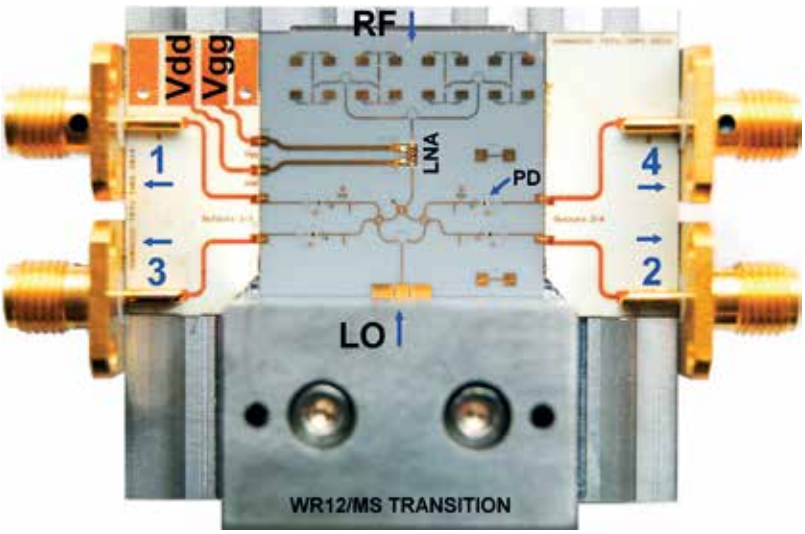

Figure 18. The fabricated six-port front-end receiver prototype.

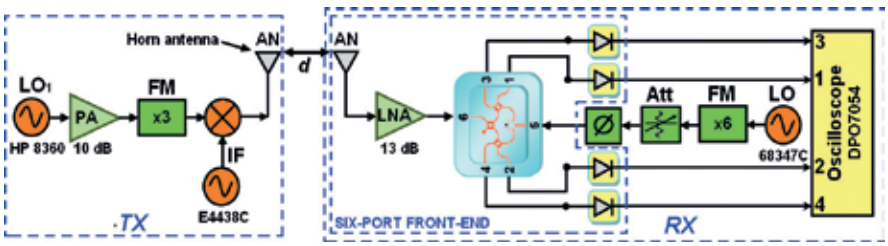

Figure 19. Block diagram of the test bench for the fabricated six-port front-end receiver prototype.

with the 600 MHz intermediate frequency (IF) signal from Agilent E4438 source, through a balanced RF mixer. In order to transmit the modulated signal, a horn antenna operating at the 60 GHz band, with a gain of about 22 dBi, is also employed.

In the receiving part, a frequency multiplier (x6) is used to generate the LO signal having the frequency of 62.19 GHz, at port 5 of the fabricated 60 GHz front-end receiver prototype (signal coming from Anritsu 68347C Synthesized Signal Generator at 10.38 GHz (6×10.38 GHz)). An attenuator and phase shifter are also used to control the power level and phase of the LO signal in millimeter-wave band (V-band), respectively. The four output signals, from the 60 GHz front-end receiver prototype, are displayed and recorded using a Tektronix digital phosphor oscilloscope (DPO7054), with 1 MΩ input impedance.

The demodulation results of various signals, from 4 to 32 symbols, are therefore obtained as shown in **Figure 21**. As can be observed in these captures, the symbols of BPSK, 8PSK, and 16PSK demodulations are distributed evenly around the circle. Likewise, for the QPSK constellation diagram, a quasi-perfectly square shape is achieved, whereas for the 16QAM and

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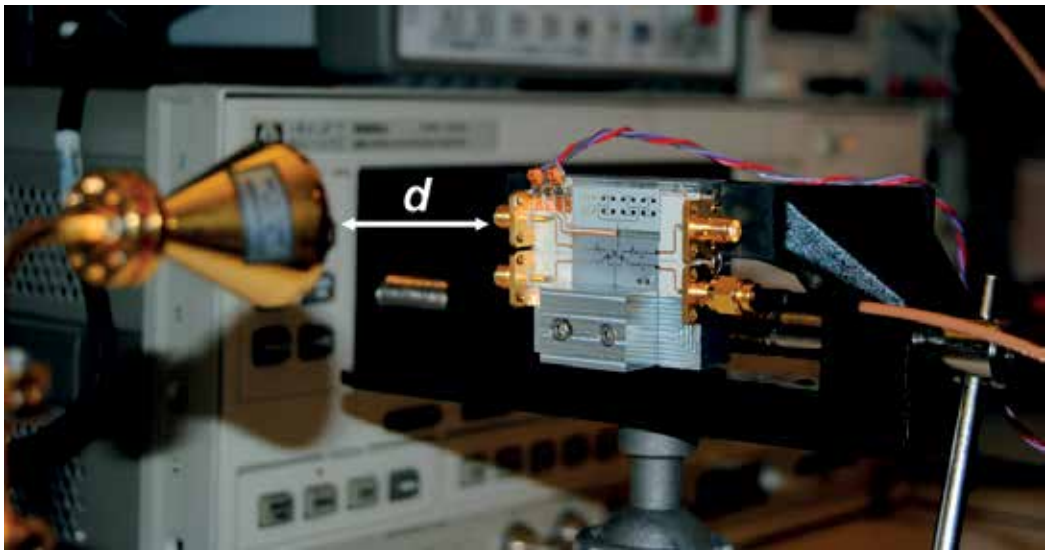

Figure 20. Photograph of the test bench for the fabricated 60 GHz six-port front-end receiver.

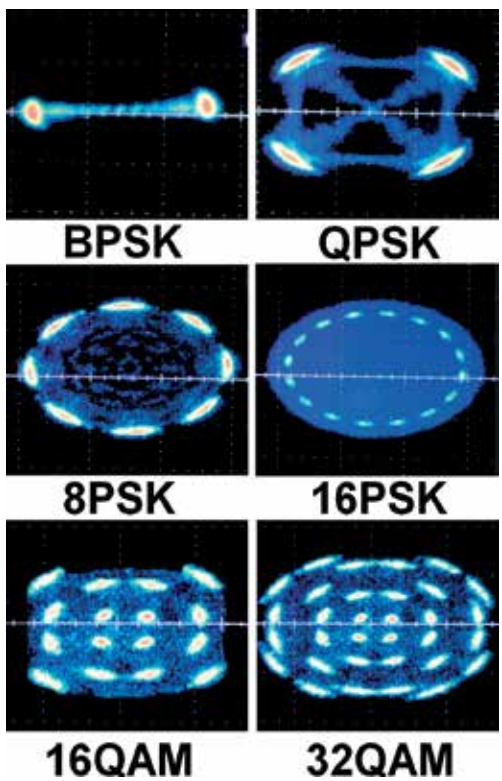

Figure 21. Experimental constellation results of the demodulated MPSK/MQAM signals.

32QAM, the points are almost equidistant, proving the front-end discrimination's qualities in both amplitude and phase, according to the six-port demodulation theory [12]. As can be seen, the phase and amplitude errors are minimal, not exceeding a few percent for each constellation point. It should be pointed out that those errors are mainly due to synchronization of transmitting and receiving equipment (phase noise), as well as the fabrication tolerances (symmetry of the constellation points).

4. Conclusion

The research on the front-end receiver designs in the unlicensed 60 GHz frequency band has been going on for several years now. Although a multitude of 60 GHz front-end configurations have been published in literature, they are not consequently optimized for low power consumption. In this context, the multi-port technique has been proposed as an attractive solution enabling the design of low-cost and compact wireless communication receivers at microwave and millimeter-wave frequency bands.

This chapter describes in detail the design of a low-power 60 GHz direct conversion front-end receiver based on the multi-port (six-port) concept, using a less costly MHMIC fabrication process. The demodulation performances of the proposed front-end receiver structure have been experimentally proven through various M-PSK/M-QAM demodulated signals. The obtained demodulation results, demonstrating the ability of the proposed 60 GHz six-port front-end receiver to directly demodulate PSK or QAM millimeter-wave signals to baseband, or even to down-convert them in quadrature to a given intermediate frequency (IF), create a real expansion opportunity to the future compact, low-power, and low-cost 60 GHz wireless communication systems.

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Section 3

Applications on Emerging Technologies

Chapter 5

Applications of Compressive Sampling Technique to Radar and Localization

Soheil Salari, Francois Chan and Yiu-Tong Chan

Additional information is available at the end of the chapter

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Abstract

During the last decade, the emerging technique of compressive sampling (CS) has become a popular subject in signal processing and sensor systems. In particular, CS breaks through the limits imposed by the Nyquist sampling theory and is able to substantially reduce the huge amount of data generated by different sources. The technique of CS has been successfully applied in signal acquisition, image compression, and data reduction. Although the theory of CS has been investigated for some radar and localization problems, several important questions have not been answered yet. For example, the performance of CS radar in a cluttered environment has not been comprehensively studied. Applying CS to passive radars and electronic warfare receivers is another concern that needs more attention. Also, it is well known that applying this strategy leads to extra computational costs which might be prohibitive in large-sized localization networks. In this chapter, we first discuss the practical issues in the process of implementing CS radars and localization systems. Then, we present some promising and efficient solutions to overcome the arising problems.

Keywords: analog-to-digital converter (ADC), blind detection, clutter, compressive sampling (CS), compressive sensing (CS), localization, radar, time-difference of arrival (TDOA)

1. Introduction

The well-known Nyquist sampling theorem, which has served as a starting point for development of traditional analog-to-digital converters (ADCs), states that the sampling rate needs to be at least twice as high as the bandwidth of the input signal to achieve aliasing-free sampling. Moving to higher communication throughputs and carrier frequencies motivates the search of

innovative ADCs, specifically when sampling rates reach several gigahertz. This is because employing traditional ADCs would result in very expensive architectures, particularly at high sampling rates; since they require a large die area and consume extremely high power even for resolutions as low as 7-bits [1–4]

To overcome these issues, different methods, such as the time-interleaving structure and the multichannel filter-bank approach, have been proposed in the literature. Unfortunately, these techniques are only suitable for special scenarios or applications because of their high power consumption and their non-ideal characteristics. For further details, the interested reader can refer to [1–4] and the references therein. More recently, a novel sampling strategy based on the emerging technique of compressive sensing (CS) [5–7], is able to reduce the sampling rates considerably. This strategy is also called compressive sampling since it breaks through the limits of the Nyquist sampling theory.

The technique of CS enables the reconstruction of a sparse (compressible) signal vector $\boldsymbol{x} \in R^N$ from the measurement vector $\boldsymbol{y} \in R^M$ generated by

$$\boldsymbol{y} = \boldsymbol{\Phi x} \tag{1}$$

where $\boldsymbol{\Phi} \in R^{M \times N}$ is the measurement matrix with $M << N$. It has been demonstrated that the proper selection of the measurement matrix $\boldsymbol{\Phi}$ is a key point for the success of CS [6].

During the last decade, CS has been successfully applied in many applications, such as image processing [8], wireless sensor networks and communication networks [9]. Although some recent works have studied the application of CS to radar and localization [10], several important questions have not yet been answered. For example, the application of CS in electronic warfare and passive radar scenarios has not been studied well. Furthermore, the effects of clutter and other structured noises on the performance of CS-based radar systems have not been comprehensively investigated to the knowledge of the authors. The extra computational burden caused by signal reconstruction methods is another practical challenge that should be carefully considered. While all previous works have improved our knowledge, the above shortcomings greatly motivate us to provide a more realistic analysis that addresses these important issues. The main aim of this chapter is to investigate some aspects of CS applied to radar concerning the reduction of ADCs' sampling rates. Also, we present a novel CS-based strategy to decrease the traffic of large-scale localization networks with reduced computational complexity. It is not the aim of this chapter to investigate numerically efficient algorithms but to point out some problems, arising when designing and developing practical CS-based radars and localization systems, as well as possible solutions.

In the literature, the terms "compressive sensing" and "compressive sampling" are used interchangeably. Here, we make the distinction that compressive sensing means a dimension reduction of a data vector using a compressed sensing measurement matrix. Compressive sampling is the reduction of the sampling rate (from the Nyquist rate) in the digitization of an analog signal.

The organization of this chapter is as follows. In Section 2, we briefly review the basics of CS theory. In Section 3, we first present the radar main concepts. Then, we show how employing

CS can reduce the sampling rate substantially. Next, we introduce two main scenarios where the standard CS radar formulation is not applicable. Finally, we propose an efficient technique that can be used to address the shortcomings of existing methods. In Section 4, we first briefly review the main concepts of localization. Then, we explain how the reconstruction step of the CS technique significantly increases the complexity of localization algorithms. Finally, we introduce a novel method which eliminates the complex recovery step of CS-based localizers and reduces the data traffic between the sensors and the fusion center.

2. Compressive sampling basics

Suppose a signal $\boldsymbol{x} \in R^N$ can be represented as:

$$\boldsymbol{x} = \boldsymbol{\psi}\, \boldsymbol{s}, \tag{2}$$

where $\boldsymbol{\psi} = [\boldsymbol{\psi}_1, \ldots, \boldsymbol{\psi}_{\mathrm{N}}] \in R^{N \times N}$ is a full rank, orthonormal basis matrix, sometimes also known as the basis matrix [5], and the vector $\boldsymbol{s} = [\mathrm{s}_1, \ldots, \mathrm{s}_{\mathrm{N}}] \in R^N$ has K non-zero elements. Then the signal $\boldsymbol{x}$ is K-sparse. In fact, the signal $\boldsymbol{x}$ is K-sparse if it is a linear combination of only K basis vectors; that is, only K elements of vector $\boldsymbol{s}$ in (2) are nonzero and the other (N-K) elements are zero. Also, we say that the signal $\boldsymbol{x}$ is compressible if the representation (2) has just a few large coefficients and many small coefficients in $\boldsymbol{s}$. A sparse signal is compressible as described below. Putting (2) into (1) yields:

$$\boldsymbol{y} = \boldsymbol{\Phi\psi s} = \boldsymbol{\Theta s}, \tag{3}$$

where $\boldsymbol{\Theta} = \boldsymbol{\Phi}\psi \in R^{M \times N}$ is called the sensing matrix. Since $M < N$, $\boldsymbol{y}$ is a compressed measurement of $\boldsymbol{x}$. Such compression makes possible the storage and transmission of $\boldsymbol{x}$ at a lower dimension. Hence, CS is an important data compression technique.

This means that instead of measuring the N-point signal $\boldsymbol{x}$ directly, the CS framework acquires the information from far fewer measurements ($M \ll N$) than traditional methods. Notice that since $\boldsymbol{\Theta}$ has far fewer rows than columns, (3) is non-invertible and underdetermined, rendering the CS problem ill-posed [11]. The main question therefore is: "how to recover $\boldsymbol{x}$ from $\boldsymbol{y}$?"

In general, (3) has no unique solution since it has more unknowns (N) than equations (M). However, since $\boldsymbol{x}$ is K-sparse, we know that N-K unknown elements in $\boldsymbol{s}$ are zero. It is then possible to recover $\boldsymbol{s}$ from (3) using a technique known as l_1 minimization [6]. From $\boldsymbol{s}$ we recover $\boldsymbol{x}$ via (2).

The signal $\boldsymbol{x}$ is thus compressible and recoverable. It is well known that images and speech signals are compressible signals. Another example is a vector $\boldsymbol{x}$ whose elements are sums of samples of two sinusoids. Its $\boldsymbol{\psi}$ in (2) consists of columns of sinusoidal samples of frequencies $w_1, \ldots, w_N$. If the sinusoids have frequencies w_3 and w_5, then $\boldsymbol{s}$ has only non-zero elements at positions 3 and 5.

There are mathematical conditions on $\boldsymbol{\Theta}$, and the numbers of measurements M, needed to ensure recovery of $\boldsymbol{s}$. They are given in the next three subsections.

2.1. Number of measurements

Choosing the number of measurements M is a trade-off: While a small M is desirable for high compression, it must be sufficiently large to enable reconstruction. Generally M should be in the order of $\log_2 \frac{N}{K}$. A rule of thumb is $M \cong 4K$ [6] provided that $\boldsymbol{\Theta}$ satisfies both the conditions of Incoherence (Subsection 2.2) and Restricted isometry property (Subsection 2.3).

2.2. Incoherence

From (3), it is seen that the elements of $\boldsymbol{y}$ are a linear combination (l.c.) of the elements of $\boldsymbol{s}$, via the matrix $\boldsymbol{\Phi\psi}$. If $\boldsymbol{\Phi}$ is highly correlated to $\boldsymbol{\psi}$, the probability of having independent l.c. (or measurements) of $\boldsymbol{s}$ decreases.

To see this, suppose $\boldsymbol{\Phi\psi}$ has a column, say the i-th column that contains all zeros. Then $\boldsymbol{y}$ is missing a measurement of the i-th element in $\boldsymbol{s}$, and if this element is non-zero, we cannot recover $\boldsymbol{s}$ from $\boldsymbol{y}$. This will happen if a row of $\boldsymbol{\Phi}$ is orthogonal to a column of $\boldsymbol{\psi}$, i.e., there is a strong correlation between $\boldsymbol{\Phi}$ and $\boldsymbol{\psi}$. In CS theory, there is a theorem that relates the required number of measurements M, for perfect reconstruction, to the coherency (a numerical number) of $\boldsymbol{\Phi}$ and $\boldsymbol{\psi}$. The higher the coherency, the higher the required M is.

2.3. Restricted isometry property (RIP)

For $\boldsymbol{\Theta} = \boldsymbol{\Phi\psi}$, the RIP requires that for perfect reconstruction, $\boldsymbol{\Theta}$ must satisfy the inequality

$$\alpha\|\boldsymbol{s}\| \le \|\boldsymbol{\Theta s}\| \le \beta\|\boldsymbol{s}\|, \tag{4}$$

with $0 < \alpha < 1$ and $1 < \beta < 2$.

Notice that the isometry is the length of a vector. The inequality (4) limits the amount by which Euclidean distance $\|\boldsymbol{\Theta s}\|$ can differ from $\|\boldsymbol{s}\|$. The lower bound in (4) ensures a perfect recovery. Suppose $\|\boldsymbol{s}\| \neq 0$ but $\|\boldsymbol{\Theta s}\| = 0$. This violates the lower bound of (4). Indeed, if $\boldsymbol{y} = \boldsymbol{\Phi\psi s} = 0$, we cannot recover $\boldsymbol{s}$ from $\boldsymbol{y}$. Note that $\|\boldsymbol{\Theta s}\| = 0$ when $\|\boldsymbol{s}\| \neq 0$ implies that $\boldsymbol{s}$ is in the null space of $\boldsymbol{\Theta}$, meaning that at least two columns of $\boldsymbol{\Theta}$ are linearly dependent. Further to this point, consider two K-sparse vector $\boldsymbol{s}$ and s^*. The maximum sparsity of $\boldsymbol{s}$-$\boldsymbol{s}^*$is 2 K. To be able to distinguish $\boldsymbol{\Theta s}$ from $\boldsymbol{\Theta}s^*$, we must have

$$\boldsymbol{\Theta}(\boldsymbol{s} - \boldsymbol{s}^*) \neq 0. \tag{5}$$

i.e., any 2 K columns of $\boldsymbol{\Theta}$ must be linearly independent. This ensures that $\boldsymbol{\Theta}$ satisfy the lower bound of (4).

The upper bound is necessary to keep the lower bound meaningful. Otherwise, $\boldsymbol{\Theta}$ can be arbitrary scaled to satisfy the lower bound.

Note that incoherency and RIP both give conditions for perfect reconstruction. But the incoherency condition is valid only for a K-sparse vector. In contrast, RIP applies even when $\boldsymbol{s}$

is a non-sparse vector; in this case, the recovered vector will consist of the K most significant elements.

Checking if a chosen $\boldsymbol{\Theta}$ satisfies the RIP criteria is computationally expensive and cannot be realized in practice. It has been shown in [6] that with high probability, random Gaussian, Bernoulli, and partial Fourier matrices do satisfy the RIP condition.

Finally, in practice, noise is commonly present in the measurement. Therefore, (3) becomes

$$\boldsymbol{y} = \boldsymbol{\Phi\psi s} + \boldsymbol{e} = \boldsymbol{\Theta s} + \boldsymbol{e}, \tag{6}$$

where $\boldsymbol{e} \in R^M$ represents an unknown noise vector. Recovering $\boldsymbol{s}$ from $\boldsymbol{y}$ will yield additional errors due to $\boldsymbol{e}$. A bound on this error, as a function of the power of $\boldsymbol{e}$, can be obtained [7].

2.4. Sampling rate reduction by CS

In some applications, for example in an electronic warfare (EW) receiver, a high sampling rate is required because the receiver must scan for signals with high bandwidths. High rate ADCs have low accuracy and consume high power. In addition, the high number of samples can fill up the available memory quickly. As we will show, compressive sampling can essentially reduce the sampling rate and number of samples via a system known as the random-modulation pre-integrator (RMPI) [12].

A simplified block diagram of the sampling scheme given in [12] is shown in **Figure 1**. An RMPI with four output channels generates a CS vector $\boldsymbol{y} \in R^{80}$.

Here, $\boldsymbol{x}$(t) represents the input signal with bandwidth B Hz. Also, note that the Nyquist sampling rate is 2B Hz, and one-bit duration is equal to $\frac{1}{2B}$ second. Since the duration of 52 bits is $\frac{52}{2B}$, an ADC samples at $\frac{2B}{4\times52}$ Hz. So, the actual sampling rate is $\frac{2B}{52}$ Hz and each integrator sums $\frac{52}{2B}$ seconds of the product of $\boldsymbol{x}$(t) and PRBS, then resets and repeats. We have:

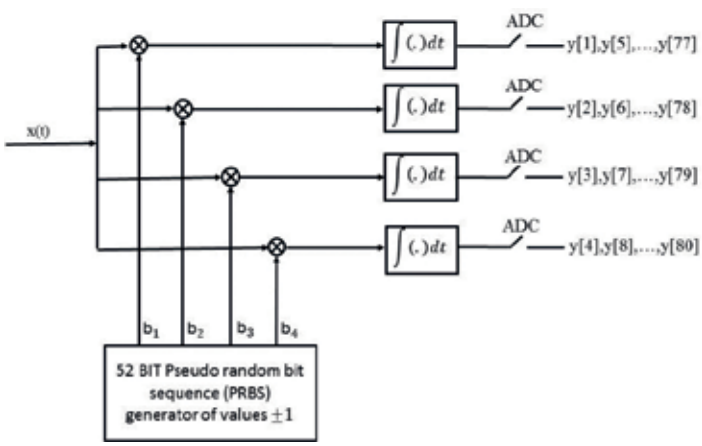

Figure 1. Block diagram of RMPI with four channels.

$$\boldsymbol{x} = [x(1), \ldots, \mathrm{x}(1040)]^T \tag{7}$$

$$\boldsymbol{y} = \left[y(1), \ldots, \mathrm{y}(80)\right]^T \tag{8}$$

$$\boldsymbol{\Phi} = \begin{bmatrix} \boldsymbol{A}_1 & 0 & \ldots & 0 \\ 0 & \mathbf{A}_2 & \ldots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \ldots & \mathbf{A}_{20} \end{bmatrix} \tag{9}$$

where $A_i \in R^{4\times 52}$contains elements of ± 1. Hence, the sampling rate is reduced by a factor of 13, as is the number of samples, i.e., $\frac{N}{M} = 13$.

3. Application of CS to radar

In this section, we seek to provide a more realistic analysis of the application of CS in practical radar systems. We follow an alternative approach instead of that used in previous published works in the context of CS radar, which is a generalization of a canonical CS formulation. Although our approach is designed for the radar scenario, it is also capable of accommodating other practical scenarios in which the basis matrix is (partially) unknown and/or the observed data is contaminated by structured noises (interference).

3.1. Introduction

Radar (radio detection and ranging) systems are present in many different civilian, military, and biomedical applications [13]. Radar systems are used to detect and determine the range, angle, and velocity of different objects, such as aircraft, missiles, ships, tanks, helicopters, and ground stations. Air traffic control, mapping of ground contours, detecting weather formations, and automotive traffic enforcement are some civilian applications of Radar systems.

Traditional radar systems consist of a transmitter, a transmitting antenna, a receiving antenna, and a receiver (powerful processor). The transmitter sends probing pulses of electromagnetic waves toward the areas of interest. The properties of the transmitted waves change when they are reflected by the potential targets. This enables the radar to locate the unknown targets (threats). This kind of detection is usually called active detection. Passive radars, which are essentially receive-only radars, do not transmit any probing signal. Instead, passive radars perform detection and estimation from signals that come from sources such as radar, radio and television (TV) stations [14].

A single-input single-output (SISO) radar consists of a single transmitter and a single receiver. A few decades ago, multiple-input multiple-output (MIMO) radar systems have been proposed as an extension of SISO radar systems. MIMO radar systems employ multiple elements on the transmitting and receiving sides, while SISO radars employ one element on each side. It

is demonstrated that employing multiple transmit and receive elements significantly improves the performance. Since an SISO radar can be considered as a special case of MIMO radars, most recent works have focused on the MIMO scenario.

Broadly speaking, there are two main groups of MIMO radars: Co-located MIMO radars and distributed MIMO radars [15]. In the co-located MIMO radar all the antennas are closely spaced, while in the distributed MIMO radar, the antennas are widely separated. To be more precise, a distributed MIMO radar views the potential target from different angles. Hence, if the received signal from any specific path is weak, it can be compensated by signals received from other paths. Although all transmit-receive antenna pairs in a co-located MIMO radar see the potential target from the same view, transmitters use different probing waveforms. In summary, a distributed MIMO radar exploits the spatial diversity, while a co-located MIMO radar exploits the waveform diversity.

3.2. CS for radar

Usually, radar detection and classification tasks require the transmission of wide-bandwidth probing signals during short observation times. Employing wideband probing pulses necessitates using fast ADCs with high sampling rates, which in turn leads to the generation of a huge amount of data. In most cases, data processing becomes one of the most important design issues. Recently, the emerging technique of compressive sampling has been proposed to alleviate the identified practical problems [16]. As mentioned previously, CS exploits the sparsity (compressibility) of received signals in different spaces to reduce the sampling rate as well as the volume of generated data and hence, is a promising technique for sophisticated radar systems.

The idea of using the CS technique in the context of radar systems was initially proposed by Herman and Strohmer in [17]. They showed that since the number of targets is typically much smaller than the number of range-Doppler cells, the prerequisite on the signal sparsity is often met in most radar scenarios, and hence CS can be efficiently used in radar systems. It is worth mentioning that [17] just focused on the simple SISO radar scenario. Then, Chen and Vaidyanathan in [18] extended the work in [17] to the MIMO radar case. During the last decade, different aspects of employing CS in both SISO and MIMO radars have been investigated; please see [15, 19] and the references therein.

Although CS has been applied in radar problems, it has not been comprehensively studied with respect to clutter and other structured noises. To be more precise, all related works modeled the observed signal by radar as a signal contaminated by additive noise. However, it is more realistic to add another term into the model to account for the clutter. Also, the proposed methods in the literature are suitable only for the case where radar transmitting waveforms are completely known, and hence, are not applicable to some important practical cases, such as electronic surveillance and threat recognition cases. To the best of our knowledge, none of the published works, on application of CS to radar, studied the general case where the signal is contaminated by clutter and the basis matrix is (partially) unknown.

The above shortcomings motivate us to provide a more realistic model that addresses these important issues. To this end, in the next subsection, we first present a high-level block diagram of CS-based radar architecture to show how CS can be employed to reduce the sampling rate of traditional radar systems. Then, in the next subsections, we study the case where perfect knowledge of the transmitted waveforms is not available, and when the received signals are contaminated by clutter and other structured noises. Finally, we introduce our solution for such a complex problem.

3.3. Sub-Nyquist radar system

We now explain how CS is able to relax the required Nyquist-sampling rate of traditional radar systems. Let $x(t)$ represent the signal received by a radar system with bandwidth B. As depicted in **Figure 2**, $x(t)$ is first multiplied by the sensing matrix $\mathbf{\Phi}(t)$ in the time domain at Nyquist frequency f_S. The modulated signal is then integrated for a duration of $\frac{N}{f_S}$.The output is sampled at sub-Nyquist rate $\frac{f_S}{N}$. One can easily show that

$$y_i = \int_t^{t+\frac{N}{f_S}} \Phi_i(t)\mathbf{x}(t)dt, \quad i = 1, \ldots, M, \tag{10}$$

where N is the number of integration samples per compression block. The selection of the sensing matrix that multiplies the input vector is a key point for the success of every CS approach. It has been shown that in most applications, the use of random sensing matrices provides a good performance. Let us assume that

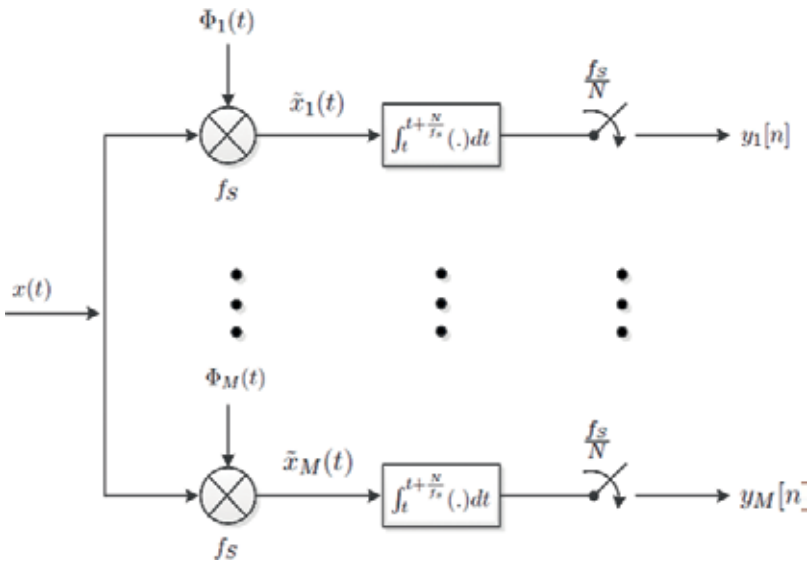

Figure 2. Block diagram of compressive sampling architecture for radar systems.

$$\Phi_i(t)\Big|_{t=\frac{j-1}{f_S}}^{t=\frac{j}{f_S}} = \Phi_{i,j} \in \{+1, -1\}, \quad i = 1, \ldots, M, \;\; j = 1, \ldots, N. \tag{11}$$

Then, y_i in (10) can be represented as

$$y_i = \sum_{j=1}^{N} \Phi_{i,j} x_j, \;\; i = 1, \ldots, M, \tag{12}$$

$$\begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_M \end{bmatrix} = \begin{bmatrix} \Phi_{1,1} & \Phi_{1,2} & \ldots & \Phi_{1,N} \\ \Phi_{2,1} & \Phi_{2,2} & \ldots & \Phi_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ \Phi_{M,1} & \Phi_{M,2} & \ldots & \Phi_{M,N} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_N \end{bmatrix} \tag{13}$$

where $x_j = \int_{t+\frac{(j-1)}{f_S}}^{t+\frac{j}{f_S}} \Phi_i(t) x(t) dt$ and x_j are simply the Nyquist samples of the input signal x(t). For our purposes, it is more convenient to write (3) in matrix form as:or, equivalently, as (excluding noise):

$$\boldsymbol{y} = \boldsymbol{\Phi x}, \tag{14}$$

where $\boldsymbol{y} = [y_1, \ldots, y_M]^T$, $\boldsymbol{x} = [x_1, \ldots, x_N]^T$, and $\boldsymbol{\Phi} = \begin{bmatrix} \Phi_{1,1} & \Phi_{1,2} & \ldots & \Phi_{1,N} \\ \Phi_{2,1} & \Phi_{2,2} & \ldots & \Phi_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ \Phi_{M,1} & \Phi_{M,2} & \ldots & \Phi_{M,N} \end{bmatrix}$. Thus, CS reduces the sampling rate to $\frac{Mf_S}{N}$, which is much lower than the Nyquist rate f_S.

The architecture presented in **Figure 2** can be adapted to any application. The main idea is that the input signal is first compressed in the analog domain and then, traditional ADCs are used for sampling.

Remark: Exploiting the sparsity of the received signal $\boldsymbol{x}$ in different spaces, we have: $\boldsymbol{x} = \boldsymbol{\psi s}$, where ψ represents the basis matrix in which signal $\boldsymbol{x}$ is sparse. Taking into account the noise (denoted by **e**), $\boldsymbol{y}$ can be expressed as:

$$\boldsymbol{y} = \boldsymbol{\Phi \psi s} + \boldsymbol{e}. \tag{15}$$

The standard equation (15) is the starting point of existing literature in the context of CS-based radars. To be more precise, exploiting the sparsity of radar signals in various spaces, radar problems are first transformed into the CS context (radar problems are reformulated as a recovery of sparse vectors). Then the CS problems are solved by conventional sparse recovery methods. All conventional recovery methods assume that both sensing ($\boldsymbol{\Phi}$) and basis ($\boldsymbol{\psi}$) matrices are known and available. As we will discuss in Subsection 3.4, this fundamental assumption is not valid in some important radar applications.

3.4. Blind compressive sampling

In some radar scenarios, knowledge of the basis matrix ($\boldsymbol{\psi}$) is available. For example, in MIMO radar scenario, the transmitted waveforms are known a priori. Therefore, a receiver can use this knowledge to construct the basis matrix locally. However, in some practical cases like passive radars, the transmitters are not part of the radar system, and hence, perfect knowledge of the transmitted waveforms is not available. Therefore, a receiver is only able to reconstruct from a noisy version of the basis matrix ($\boldsymbol{\psi}$). As discussed in the related literature, erroneous basis matrices can lead to a significant performance loss (huge decrease in probability of detection), which is not acceptable in practice.

Also, in some other applications such as electronic surveillance and threat recognition, electronic warfare (EW) [14] receivers are preferred to both passive and active radars. Particularly, EW receivers need neither probing pulses nor illuminator signals, since they listen to the electromagnetic radiations of the potential threats instead of weak reflected radar (illuminator) signals. More specifically, EW receivers detect potential targets through sensing the electromagnetic spectrum, and extracting (and/or analyzing) the characteristics of their transmissions. Therefore, their detection range is much higher than that of radars, while they remain electronically silent and undetectable. However, applying standard CS techniques in the context of EW receivers is not possible. This is because a priori knowledge about the transmitted signal by unknown source is not available at all, which means a receiver is not able to build the basis matrix ($\boldsymbol{\psi}$).

The above-mentioned scenarios motivated us to study the CS problem for the case where perfect knowledge of the basis matrix ($\boldsymbol{\psi}$) is not available ($\boldsymbol{\psi}$ is completely unknown or noisy). This interesting scenario can be referred to as the blind CS problem [11]. In summary, the blind CS problem aims to recover the sparse vector $\boldsymbol{s}$ from measurements $\boldsymbol{y}$ obtained from $\boldsymbol{y} = \boldsymbol{\Phi\psi s}+\boldsymbol{e}$, while the basis matrix $\boldsymbol{\psi}$ is unknown. This is in sharp contrast to the existing CS literature which is based on a perfect knowledge of the basis matrix. In general, solving such a problem is very hard since we have three unknowns: sparse vector $\boldsymbol{s}$, basis matrix $\boldsymbol{\psi}$, and noise vector $\boldsymbol{e}$. An efficient CS-based method which iteratively solves this problem has been proposed in [14].

3.5. CS-based radars in cluttered environments

Clutter, a term used for unwanted echoes, can cause serious performance issues with radar systems. Although CS has been applied to different radar problems, it has not yet been studied with respect to clutter and other structured noises. It is not possible to neglect the effects of clutter since clutter is produced from nearly all surfaces when illuminated by a radar, such as ground, sea, rain, animals/insects, chaff and atmospheric turbulences. In order to build reliable practical CS-based radars, it is necessary to investigate the harmful effects of clutter and other environmental factors on the CS performance. Up to now, all existing works in the field of CS radar limited their studies to the ideal clutter-free scenario.

The definition of clutter depends on the mission and function of the intended radar system. Usually, in the context of radar, clutter is modeled as the superposition of echoes from all

unwanted objects. Therefore, it is realistic to introduce a third term in the CS model (15) to account for clutter and other interfering signals. In the presence of clutter, the signal measured by the radar receiver can be written as

$$\boldsymbol{y} = \boldsymbol{\Phi\psi s} + \boldsymbol{e} + \boldsymbol{c}, \tag{16}$$

where $\boldsymbol{c}$ represents the clutter. As stated in [20], merging the clutter $(\boldsymbol{c})$ and the additive (unstructured) noise $(\boldsymbol{e})$ components allows us to address this kind of problems. However, it is important to highlight that merging the noise $(\boldsymbol{e})$ and the clutter components $(\boldsymbol{c})$ or ignoring the weaker component (usually additive noise) leads to poor performance in most practical cluttered environments. Therefore, it is important to derive a novel framework for recovering the sparse signals from corrupted measurements by noise and clutter. The developed method should be able to obtain knowledge on the structure of clutter. This knowledge can be used to discriminate the intended signal from the contaminating sources.

However, adding clutter as in (16) makes the sparse recovery problem much more challenging since, as stated in [21], the clutter covariance matrix is usually unknown in radar applications and has to be estimated from the observed data. This means that in addition to the sparse vector $\boldsymbol{s}$, the noise and the clutter covariance are other unknowns that should be estimated from measurements $\boldsymbol{y}$.

To be more precise, the ultimate goal is to determine the non-zero elements of vector $\mathbf{s}$ from far fewer measured samples $\boldsymbol{y}$ generated by (16), while the covariance matrix of the clutter $\boldsymbol{c}$ and the variance of the noise $\boldsymbol{e}$ are both unknown. Similar to the Blind CS problem, reconstruction of sparse radar signals in the presence of clutter is a complicated problem.

3.6. Proposed solution

As we discussed in previous subsections, reconstruction of sparse radar signals under the scenario where the received vector is contaminated by clutter and/or perfect knowledge of the basis (dictionary) matrix is not available, is very complicated. In the canonical CS formulation, i.e., $\boldsymbol{y} = \boldsymbol{\Phi\psi s}+\boldsymbol{e}$, only two unknowns exist: sparse vector $\boldsymbol{s}$ and $\boldsymbol{e}$ and its variance. However, in both Blind CS and cluttered environment cases, in addition to the sparse vector $\boldsymbol{s}$ and variance of the noise, the basis matrix (covariance matrix of the clutter) is another unknown that should be estimated from the measurement vector $\boldsymbol{y}$.Unfortunately, none of the proposed approaches for conventional CS formulation is applicable to these complex scenarios.

Applying a probabilistic approach seems to be the best method to efficiently handle these complex problems. As mentioned in [20], most probabilistic approaches for sparse signal recovery are Bayesian. It is well known that the Bayesian methods regularize the under-determined problem by employing priors on the regression coefficients. In fact, since Bayesian methods estimate the posterior distribution of the unknown coefficients instead of their point estimates, they gain more information than other methods. Also, it is worth mentioning that the performance of Bayesian approaches is better than that of other techniques, especially when a probabilistic model is a reasonable representation of the physical process that generates the observations [20].

Sparse Bayesian Learning (SBL), which was first proposed by Tipping [22], is one of the most important families of Bayesian algorithms. In the last decade, this method was the focus of numerous studies and it was greatly extended by many other researchers; for more details please see [23] and the references therein. Having noticed the benefits of SBL, [14] has recently applied SBL to EW receiver design. Also, [20] applied SBL to the scenario where the observed data is represented as the superposition of signal plus noise plus interference. These works can be considered as a good start for the most general scenario where data measured by a radar are contaminated by clutter and perfect knowledge of the basis matrix is not available.

3.7. Complexity analysis

Applying CS to radar and other systems, on one hand, reduces the volume of generated data and Nyquist sampling rate, but on the other hand, results in additional computational cost [24]. In some practical scenarios, the extra computational burden caused by CS reconstruction methods appears as a new design challenge. For example, when the number of sensors (network size) increases, this extra computational cost becomes prohibitive. Hence, finding low-complexity CS recovery methods has become one of the most popular topics in CS theory.

More recently, [25] introduced a general framework, called compressive signal processing, in which signal processing problems are solved directly in the compressive measurement domain. This methodology is in sharp contrast to the standard CS problem where full signals are first recovered from compressed measurements and then signal processing approaches are performed on the reconstructed signals. Applying such an interesting strategy enables us to take advantage of CS benefits without any extra cost. In the next Section, we will provide a similar compressive signal processing-based foundation for the localization of unknown sources.

4. Application of CS to localization

4.1. Introduction

Determining the location of unknown sources, often called localization, is an important problem in many different applications, sometimes as the first step toward solving more complicated tasks [26]. As stated in [27], a common approach to localize unknown sources in wireless systems is to collect the ranging information from radio signals traveling between the unknown source and a number of reference nodes. Usually, ranging information is measured based on one or more physical parameters of the radio signal, such as the time of arrival (TOA), time-difference-of-arrival (TDOA), received signal strength (RSS), and angle of arrival (AOA). Among these techniques, TOA-based range estimates are inherently more accurate than others, while the RSS-based is low-cost and easily implementable.

Localization of unknown sources is not possible unless the required number of reference nodes exist in the neighborhood of the unknown source. For example, in the 2-D case, at least three reference nodes are required for localization. Therefore, usually a network of reference nodes is

utilized for the positioning of unknown sources in the area of interest. In such an architecture, all reference points send their ranging measurements to a special reference point, called Fusion Centre, which performs the localization.

In most practical cases, due to limitations such as low data-rate links between reference points and high network traffic, it is not possible to send all measurements to the Fusion Centre. This significantly affects the localization accuracy. To address these issues, some recent works have applied CS to localization; for example, see [28], and the references therein. Applying CS is a promising approach to handle the aforementioned problems since it significantly reduces the amount of data generated by reference nodes. However, the extra computational burden caused by CS reconstruction methods becomes prohibitive as the number of sensors (network size) and/or sampling rate (bandwidth) increases. Hence, the challenge is to find a low-complexity CS based framework for practical localization networks.

In the following, we focus on the TDOA-based localization scenario and develop a novel CS-based localization framework that estimates the TDOAs directly from CS measurements without reconstructing the full-scale signals. It is worth mentioning that the developed method solves the computational cost issue since it eliminates the reconstruction step. Although this approach is specially designed for TDOA-based localization, it can be developed for other applications.

4.2. TDOA-based localization

Typically, TDOA-based localization consists of three main steps:

- Step 1: All reference points (also known as observing receivers) send their collected samples to the Fusion Centre.
- Step 2: Fusion Centre estimates TDOAs between different reference points involved in the positioning of unknown sources.
- Step 3: Fusion Centre solves the equations that relate the unknown source position to the estimated TDOAs.

Therefore, estimating TDOAs is an essential first step for localization of unknown sources [29], and affects the accuracy of the positioning. Most practical localizers obtain TDOA estimates by cross-correlating the received signals from different reference points. This method is usually called generalized cross-correlation (GCC). However, large distances between reference points and Fusion Centre impose limitations on the data rate between the nodes [28]. Therefore, it is not possible to estimate TDOAs of all sensor pair combinations. This limitation reduces the accuracy substantially.

Some recent works employ CS to overcome the identified issues. The block diagram of this strategy is shown in **Figure 3**. In particular, reference points first apply the technique of CS on their observed samples and then transmit CS-based version of their collected samples to the Fusion Centre. Fusion Centre then applies one of the CS recovery methods on the received CS measurements to reconstruct the Nyquist samples from CS measurements sent by the

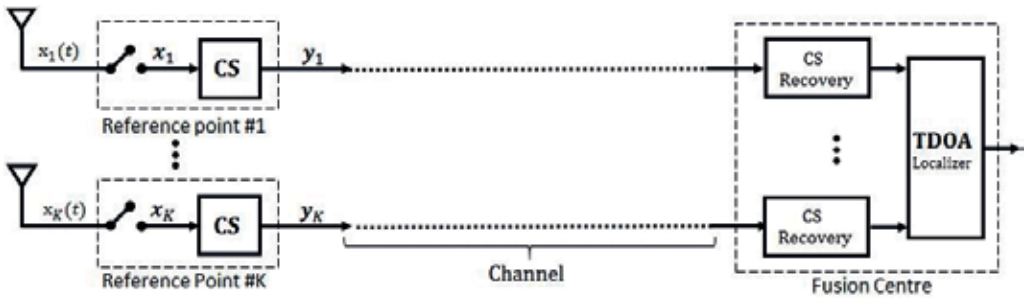

Figure 3. Block diagram of CS-based TDOA localizer.

reference points. Next, it estimates TDOAs by cross-correlating all reconstructed signal pairs. Although applying such a strategy significantly reduces the traffic of localization networks (the amount of data that need to be sent from the reference receivers to Fusion Centre), the reconstruction step introduces a prohibitive extra computational burden on the Fusion Centre. Also, it should be highlighted that all the existing recovery algorithms are subject to errors, especially in the presence of noise, interference, and clutter, which affect the accuracy of positioning. The above shortcomings motivate us to provide a new framework that addresses these important issues.

4.3. TDOA estimation without reconstruction

Consider the estimation of the TDOA between two $N \times 1$ vectors

$$\boldsymbol{x}_1 = [x(0), \ldots, \mathrm{x(N-1)}]^T \tag{17}$$

and

$$\boldsymbol{x}_2 = [x(D), \ldots, \mathrm{x(D+N-1)}]^T \tag{18}$$

where D, an integer, is the TDOA between $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$.

The circular cross-correlation of $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$ will yield a peak at a correlation shift of D samples. Now with CS, the measurements become

$$\boldsymbol{y}_1 = \boldsymbol{\Phi x}_1 \tag{19}$$

and

$$\boldsymbol{y}_2 = \boldsymbol{\Phi x}_2, \tag{20}$$

where $\boldsymbol{y}_1 \in R^M, \boldsymbol{y}_2 \in R^M$, $\boldsymbol{\Phi} \in R^{M \times N}$, and $M < N$. In general, the transformations $\boldsymbol{\Phi x}_1$ and $\boldsymbol{\Phi x}_2$ will break up the time-shift relationship between $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$. A cross correlation of $\boldsymbol{y}_1$ and $\boldsymbol{y}_2$ will not give a peak at a shift of D. A common solution is to reconstruct $\boldsymbol{x}_1$ and $\boldsymbol{x}_2$ from (19) and

(20), via CS reconstruction techniques. But the computations could be time-consuming and the reconstruction will have errors if noise is present.

A novel way to obtain CS measurements that preserve the time-shift relationship uses a $\mathbf{\Phi}$ that sums the elements of a vector. As an example, let $M = 4$, $N = 16$, and

$$\mathbf{\Phi} = [\,\mathbf{I} \mid \mathbf{I} \mid \mathbf{I} \mid \mathbf{I}\,] \in R^{M \times M} \tag{21}$$

where $\mathbf{I} \in R^{M \times M}$ is an identity matrix. Then, the elements of $\boldsymbol{y}_1$ are

$$\begin{aligned} y_1(0) &= x(0) + \mathrm{x}(4) + x(8) + x(12) \\ y_1(1) &= x(1) + \mathrm{x}(5) + x(9) + x(13) \\ y_1(2) &= x(2) + \mathrm{x}(6) + x(10) + x(14) \\ y_1(3) &= x(3) + \mathrm{x}(7) + x(11) + x(15) \end{aligned} \tag{22}$$

and for $\boldsymbol{y}_2$

$$\begin{aligned} y_2(0) &= x(D) + \mathrm{x}(\mathrm{D}+4) + x(D+8) + x(D+12) \\ y_2(1) &= x(D+1) + \mathrm{x}(\mathrm{D}+5) + x(D+9) + x(D+13) \\ y_2(2) &= x(D+2) + \mathrm{x}(\mathrm{D}+6) + x(D+10) + x(D+14) \\ y_2(3) &= x(D+3) + \mathrm{x}(\mathrm{D}+7) + x(D+11) + x(D+15) \end{aligned} \tag{23}$$

Suppose $D = 2$, then, the circular cross correlation of $\boldsymbol{y}_1$ and $\boldsymbol{y}_2$ will peak at a shift of 2. In this example, $\mathbf{\Phi}$ has compressed the measurements from $N = 16$ to $M = 4$, and TDOA estimation is obtained directly from $\boldsymbol{y}_1$ and $\boldsymbol{y}_2$, without the need for reconstruction.

5. Conclusion

This chapter has introduced the concept and advantages of compressive sampling (CS). Applying CS to radar signals with a high bandwidth can significantly reduce the sampling rate and the power required by the Analog-to-Digital converter. It has also been shown that even when the transmitted signal and the basis matrix $\boldsymbol{\psi}$ are unknown, such as in passive radars and Electronic Warfare receivers, or when clutter with an unknown covariance matrix is present, CS can be used with Sparse Bayesian Learning to reduce the sampling rate and the amount of data generated. Finally, another application of CS to localization of unknown sources has been described. When estimating the TDOA between signals, using CS can reduce the data traffic between the reference points and Fusion Centre. Furthermore, a method to estimate the TDOA without reconstructing the signals at Fusion Centre has been developed to avoid the huge computational cost and possible errors that other CS-based techniques using reconstruction require.

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Chapter 6

High-Speed Electronic Memories and Memory Subsystems

Prateek Asthana and Loveneet Mishra

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/intechopen.76257

Abstract

Memories have played a vital role in embedded system architectures over the years. A need for high-speed memory to be embedded with state-of-the-art embedded system to improve its performance is essential. This chapter focuses on the development of high-speed memories. The traditional static random access memory (SRAM) is first analyzed with its different variant in terms of static noise margin (SNM); these cells occupy a larger area as compared to dynamic random access memory (DRAM) cell, and hence, a comprehensive analysis of DRAM cell is then carried out in terms of power consumption, read and write access time, and retention time. A faster new design of P-3T1D DRAM cell is proposed which has about 50% faster reading time as compared to the traditional three-transistor DRAM cell. A complete layout of the structure is drawn along with its implementation in a practical 16-bit memory subsystem.

Keywords: SRAM, DRAM, memory subsystem, P-3TD, static noise margin

1. Introduction

In today's modern evolving electronics, manufacturing semiconductor memory technology is an essential element. Normally, based on semiconductor technology, memories, which are being used in any equipment, use processor in one form or the other. Processors have recently become much popular with an increasing number of multiprocessor system being fabricated on a single chip to increase the performance of a system. In order to support this system, memory technology needs to be escalated to compete with processor technology. An additional driver has been endowed with the fact that the software associated with the processors and computers has become more sophisticated and much larger, and this too has greatly

increased the necessity for semiconductor memory. In view of the pressure on memory, new and upgraded semiconductor memory technologies were being researched, and development could have been very expeditious. The mature semiconductor memory technologies are still extensively used and would form the paradigms of manufacturing for years to come.

The requirement for semiconductor memories with rapid advancement in technologies has been an overabundance of technologies and types of memories that have emanated viz. ROM, RAM, EPROM, EEPROM, Flash memory, static random access memory (SRAM) [1, 2], dynamic random access memory (DRAM) [3, 4], synchronous dynamic random access memory (SDRAM), and the very new magnetoresistive random access memory (MRAM) that could now be seen in the electronics literature. Each one has its own merits and areas in which it may be used. In addition to these new applications such as digital cameras, PDAs and many more applications have given rise to the exigency of memories. This chapter discusses the advancement made in the field of SRAM and DRAM memory cells while proposing a new architecture of a faster DRAM cell.

2. Static random access memory (SRAM)

In high-performance integrated circuits, static random access memories (SRAMs) have been used as on-chip memories, due to its intense access speed and compatibility with process and supply voltage. Due to aggressive complementary metal oxide semiconductor (CMOS) technology scaling, the demand for a high-performance technology has increased the amount of on-chip memory integrated into modern semiconductor devices. Recently, there has been a rapid increase in the total area occupied by these memories. The continued scaling of CMOS technology has also resulted in problems which were less severe in earlier generations. These include process-induced variations, soft errors, transistor degradation mechanism, and so on. SRAM dominates the memory hierarchy in performance, but due to area limitations and high cost per bit, they are often integrated in lesser capacity. Furthermore, as the technology scales deepen into nanometer levels, there is a reduction of the stability of SRAM to noise and radiation is reduced. It is becoming increasingly challenging to maintain an acceptable static noise margin (SNM) of SRAMs while scaling the minimum feature sizes and supply voltages. Static noise margin (SNM) degradation, which characterizes the data integrity of SRAM during a read operation, has driven the development of SRAM cell design into a new direction as the supply voltage reaches near the threshold voltage. However, the shrinking of the transistor dimensions has also increased the probability of radiation-induced errors. This chapter has the following outline. We discuss the background information on different SRAM cells and describe the SRAM stability concept along with equations. In this section, we present our simulations and discuss the results [5].

2.1. Different types of SRAM cells

2.1.1. SRAM 6T cell

The conventional SRAM cell consists of two cross-coupled CMOS inverters with two access transistors connected to supportive bit lines. **Figure 1** shows the circuit diagram of a SRAM 6T cell. During read operation, pre-charge the bit lines (BL), BLB (bit line bar) to VDD. Turn on

WL (word line). BL or BLB will pull down to low depending on storage node QD and QB. For write operation, drive bit line (BL) and bit line bar (BLB) with necessary values (0.1 or 1.0) [6]. Turn on word line, bit lines (BL or BLB overpower cell with a new value).

2.1.2. SRAM 11T cell

An SRAM 11T cell is shown in **Figure 2**. The circuit enumerates a circuit which exists as two cross-coupled inverters along with an access transistor which is controlled by the read word line (RWL) for read operation and two more access transistors which are controlled by the write word line (WWL) for write operation [3]. **Figure 2** depicts the circuit diagram of an SRAM 11T cell.

2.1.3. SRAM 8T cell

In SRAM 8T cell, two voltage sources S1 and S2 are used, one connected to the output of the bit line and the other with the bit bar line. Two NMOS transistors are connected with inputs of bit line and bit bar line, respectively, straight to switch ON and OFF the power source supply during write 0 write 1 operations. The SRAM 8T cell is shown in **Figure 3**. These power supply sources diminish the voltage swing at the output node when write operation is being performed [7]. **Figure 3** shows the circuit diagram of SRAM 8T cell.

2.2. Static noise margin

The stability of an SRAM cell is critically functional in nanometer technologies as it determines the ability to retain stored information. The static noise margin (SNM) is a measure

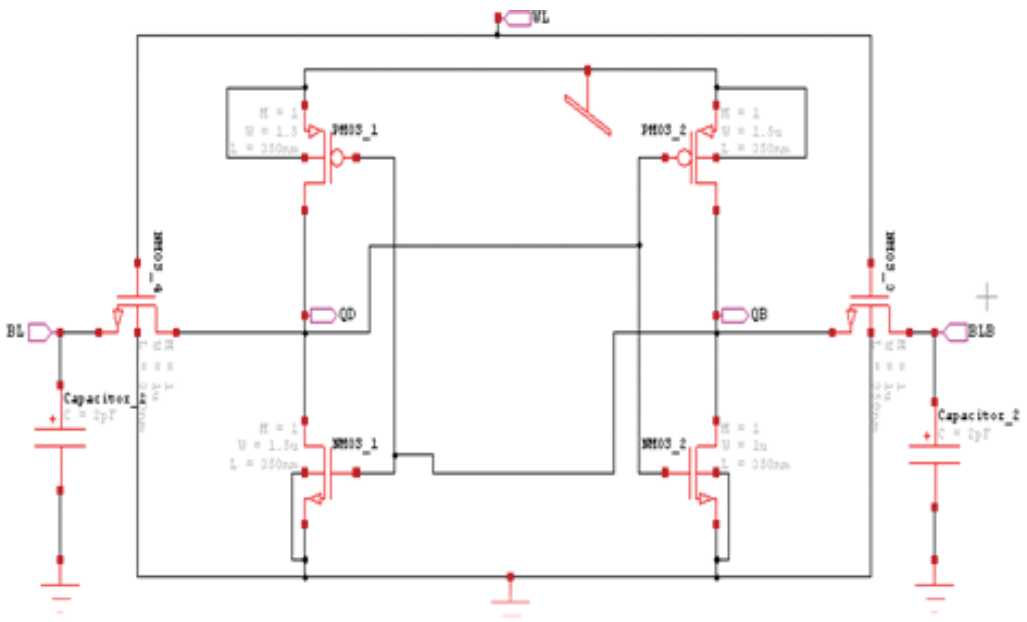

Figure 1. SRAM 6T cell.

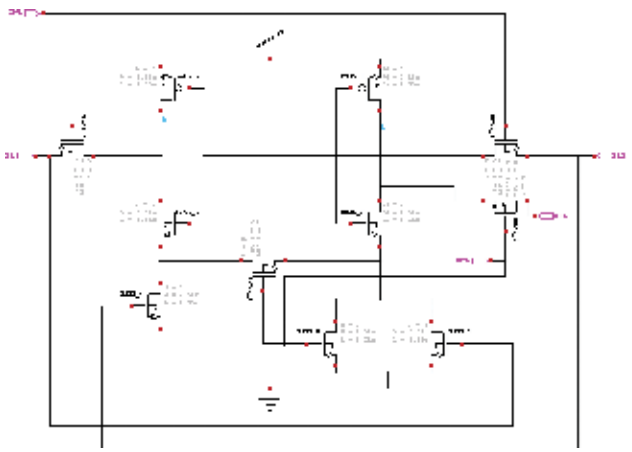

Figure 2. SRAM 11T cell.

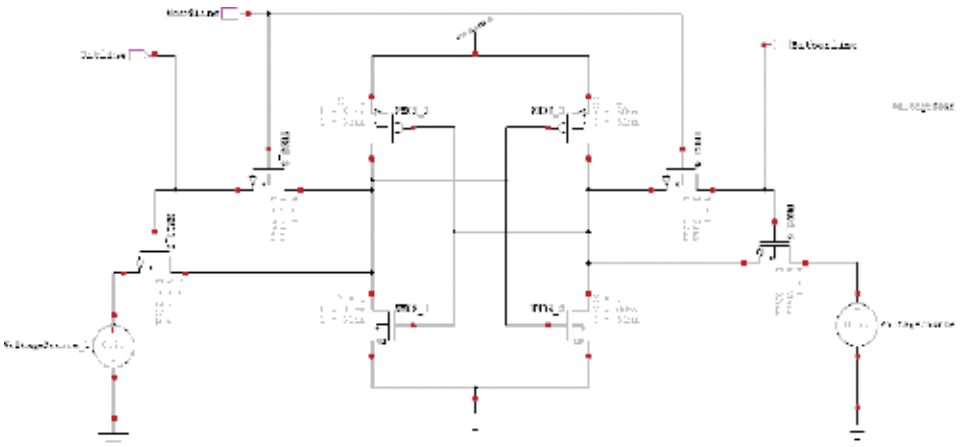

Figure 3. SRAM 8T cell.

of the SRAM stability; it is defined as the maximum static noise voltage that could be tolerated by the SRAM stability and without the loss of stored information. In other words, SNM quantifies the amount of noise voltage V_n required to flip the cell data during a read access or a standby mode. **Figure 4** shows an SRAM cell presented as two equivalent inverters with the noise voltage inserted between the corresponding inputs and outputs. Both series voltage noise sources have the same value and act in a synchronized way to upset the state of the cell.

The SNM of an SRAM cell can be represented graphically using the superimposed voltage transfer characteristics (VTC) of the inverters as shown in **Figure 5**. The resulting two-lobed curves are generally referred to as the "butterfly curve." The SNM is now defined as the length of the side of the largest embedded square inside the butterfly plot. In an ideal SRAM cell, the VTC of both inverts would be symmetrical. However, due to process variations, change in

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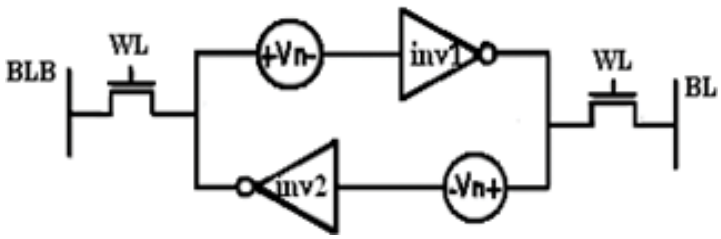

Figure 4. SRAM cell with a noise source.

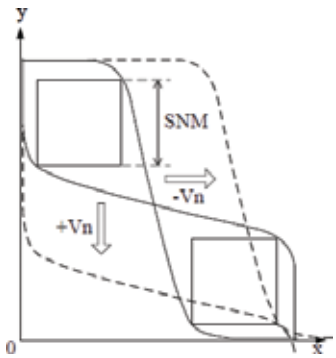

Figure 5. Static noise margin.

Cell ratio (CR)	SNM 6T SRAM (mV)	SNM 11T SRAM (mV)	SNM 8T SRAM (mV)
1	136.84	328.7	336.4
1.4	141.4	343.2	391.2
1.8	150.53	348.5	411.5
2.0	159.65	354.6	429.6

Table 1. SRAM variation with CR.

transistor attributes could result in cell imbalance. If the inverters of cell are not identical, one lobe is smaller than the other. Then, the SNM of the cell is the length of the side of the largest square that fits inside the smaller of the two lobes [8].

2.3. Measurement results

Table 1 presents the SNM variation of different SRAM cells with the cell ratio (CR) during the read operation. It can be seen that as the CR of the SRAM cell increases, the SNM also increases. Cell ratio: the ratio of driver transistor to access transistor is an important cell parameter called the cell ratio.

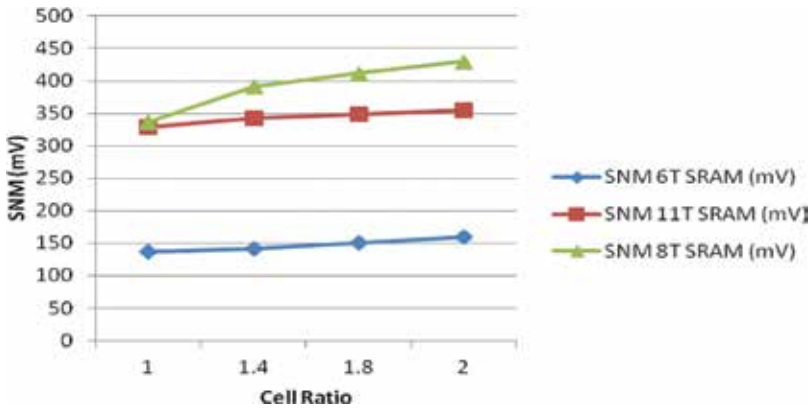

Figure 6. Cell ratio versus static noise margin.

In **Figure 6**, the SNM variation of different SRAM cells with cell ratio is shown. It can be concluded from the graph that the noise tolerance of 8T SRAM cell is more than the other two cells [9].

3. Dynamic random access memory (DRAM)

Economical and faster dynamic random access memories (DRAMs) have been widely used in all kinds of electronic devices. DRAMs have found extensive application; their mass production embarks the maturity of a semiconductor technology, which is continuously driven to give smaller dimension devices. A new semiconductor technology era having a relatively higher yield has led to the mass production of novel DRAM-generation structures. DRAM refers to a volatile memory, that is, data stored have to be dynamically refreshed to generate a correct memory data value. DRAM bits are randomly accessible compared to a conventional tape recorder. Read and write operations are necessary for DRAM cells. For reading a DRAM cell, row addresses are sent to row decoders in order to select the cell to be read by activating the necessary word line driver. When one of the word line drivers is high, the turned-on DRAM cell capacitance will charge the bit line capacitance, forming a voltage in the range of 100–200 mV [10].

In order to amplify the bit line voltage value and recover the stored data, sense amplifier is used. One sense amplifier is connected to multiple cells; hence a large amount of data is available at the same time, and large data are divided into pages, which can be accessed simultaneously. To indicate the completion of reading process, word line is turned on to isolate the DRAM cell from the bit lines. A write operation follows the similar process, with a global bit line giving the row address to the decoder and local bit lines of the cell are activated. With the help of sense amplifiers, VDD or "0" are written into the cell. A refresh operation is required to compensate for the leakage current and to refurbish the storage cell value of the cell as it elapses gradually with time. For refresh process, column access is not required as compared to the read process. First-stage sense amplifiers easily refresh the memory cells [12].

The number of data bits per unit area is the area efficiency of a memory array. It is one of the essential parameters of a memory cell along with access times. These parameters determine the overall storage capacity and memory cost per bit. Access time is essential in determining

the time required to store and/or retrieve data from the memory array. Access time helps in the determination of the speed of the memory array cell structure. Power consumption both static and dynamic is also a significant factor of the design. In this section, we would instigate various types of DRAM cells with speed and power consumption comparison being carried out between the designs. A new DRAM cell design has been described which considerably improves the speed of DRAM. The improvement in data rate consists of improvement in read access time, write access time, and retention time. These improvements will help in gaining a DRAM cell design that will be capable of giving a high performance in terms of delay and power consumptions [11, 12].

3.1. Different DRAM cells

Different DRAM cell designs based on their power and retention time are analyzed. Different DRAM cell designs are as follows:

1. 1T1C DRAM CELL
2. 3T DRAM CELL
3. 4T DRAM CELL
4. 3T1D DRAM CELL

These DRAM structures differ in the form of a number of transistors, area occupied. All these different designs have different structures and properties. The first three DRAM architectures use parasitic capacitance to store data values while the last one utilizes gated diodes to store the values. These gated diodes are generally formed from N-type metal oxide semiconductor field-effect transistor (MOSFET), but in order to reduce the power dissipation, P-type MOSFET can be utilized in their place. The advantage of this modification has been shown in comparing the various DRAM structures based on power consumption (during full cycle operation of write "0," read "0," write "1" and read "1"), write access time, read access time, and retention time (refresh time) (**Figure 7**).

3.2. Performance comparison

A new cell structure with a P-type MOSFET as a gated diode working as a capacitor has been compared on the basis of data rate and power consumption with the already existing DRAM cell structures. This gated diode cell structure is much faster than the already existing cell structures. All the cell structures are compared in an identical environment with their simulation profile as described in **Table 2**. Write and read operations are carried out on these cell structures, and their performances have been compared in **Table 3**. **Figure 8** shows the operation read-write waveform [14, 15].

3.2.1. Analysis of DRAM designs

Power consumption and access times decrease the P-3T1D DRAM cell, hence making it a faster and a low power cell as compared to the other variations. While the retention time also tends to decrease slightly, this means the memory has to be refreshed after a slightly smaller duration [11].

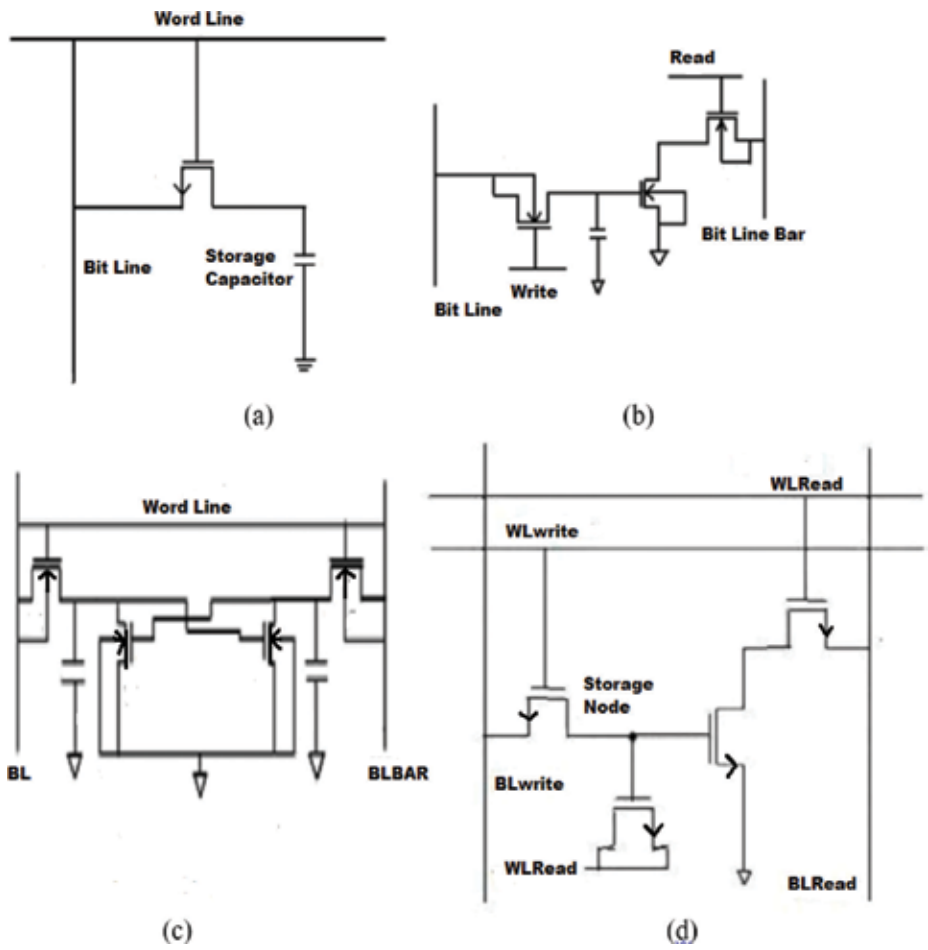

Figure 7. (a) 1T1C DRAM cell, (b) 3T DRAM cell, (c) 4T DRAM cell, and (d) 3T1D DRAM cell [13].

Operation	Time period (ns)
WRITE "1"	2–3
READ "1"	4–5
WRITE "0"	6–7
READ "0"	8–9

Table 2. Working operation of cells.

Power consumption for the proposed cell is less than the existing cells. However, the write access time is quite comparable to gated diode type DRAM cell. Read access time is almost 50% less than traditional 3T and 4T DRAM cells and approximately 34% less than N-3T1D DRAM cell. One of the most important parameters for DRAM cell is the retention time

Parameter	4T DRAM	3T DRAM	N-3T1D DRAM	P-3T1D DRAM
Average power consumption (μW)	2.384711	2.262632	2.170092	2.149554
Write access time (ps)	37.45	20.89	385.45	312.69
Read access time (ps)	71.19	70.7	68.65	44.89
Retention time (μs)	2.45621	3.49827	40.07223	33.716

Table 3. Parameter comparison for DRAM cell simulation results.

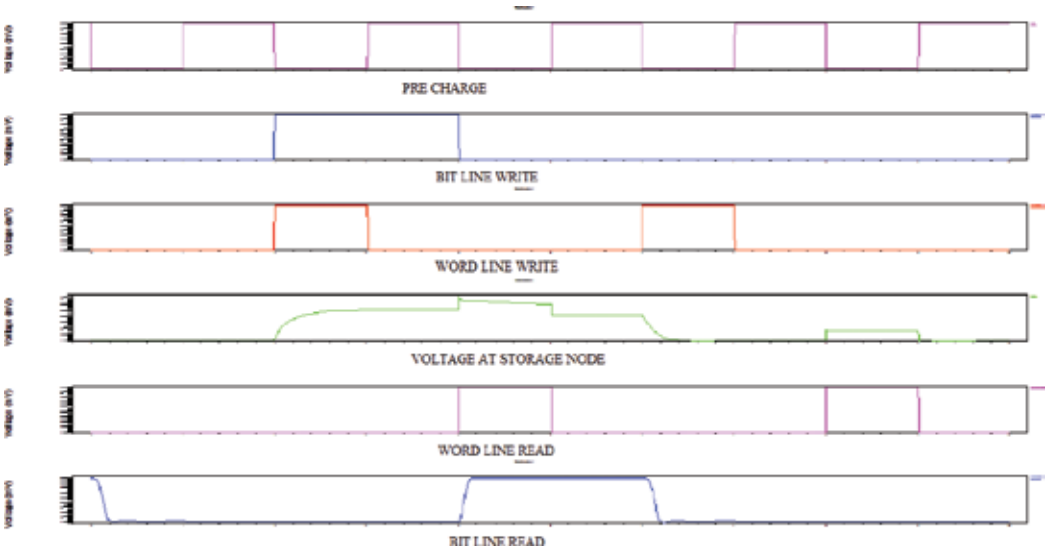

Figure 8. Read-write waveform.

or the time after which the cell needs to be refreshed while the traditional cell has a very small retention time; it is quite comparable with the already existing gated diode-based DRAM cell.

3.3. Layout for P-3T1D DRAM cell

The layout of P-3T1D cell is drawn on a 250-nm technology occupying an area of 1139.29 μm^2. The layout is drawn on LEDIT and it perfectly resembles the circuit implementation as being verified by layout versus schematic verification (**Figure 9**).

3.4. Full 16-bit memory subsystem using P-3T1D DRAM cell

A full memory is being implemented using the P-3T1D DRAM cell. The memory consists of a writing decoder, a reading decoder, 16 instances of P-3T1D DRAM cell, and four instances of output cell-reading circuitry. This output cell-reading circuitry consists of a precharge circuitry and a gated diode sense amplifier (**Figure 10**).

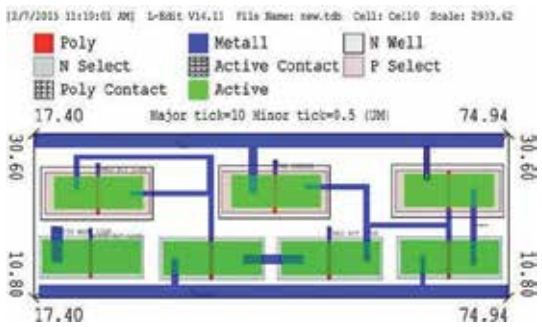

Figure 9. P-3T1D layout on 250 nm.

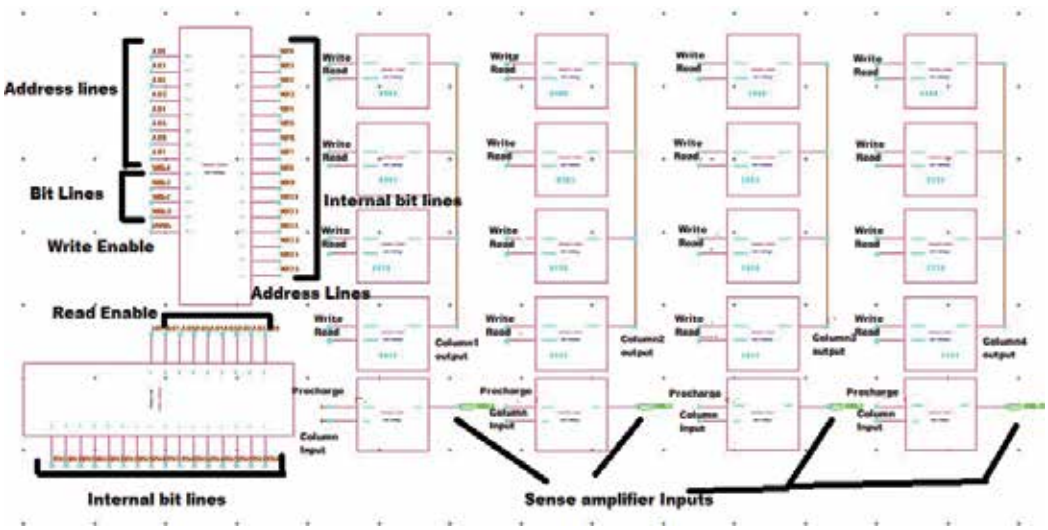

Figure 10. 16-bit memory using P-3T1D.

There are eight address lines AD0–AD7. AD0 and AD1 are used to select a bit cell from Column 1. AD2 and AD3 are used to select a bit cell from Column 2. AD4 and AD5 are used to select a bit cell from Column 3. AD6 and AD7 are used to select a bit cell from Column 4. WBL0, WBL1, WBL2, and WBL3 are 4-bit write data lines that are used in this memory cell subsystem design (**Figure 11**). RBL0, RBL1, RBL2, and RBL3 are 4-bit read data lines that are used in this memory cell subsystem design (**Figure 12**). RWL is used to control read operation turned 1 to read. WWL is used to control write operation turned 1 to write. The time for execution of the circuit is 0–50 ns. In these data 1, 0, 1, and 0 is written into CELL0, CELL 5, CELL 10, and CELL 15, respectively.

For the time period 0–10 ns, reading and writing are both turned off and PRECHARGE is at one.

For the time period 10–20 ns, PRECHARGE is low, writing is turned on, reading is off, and address line selected the cells. Using the writing decoder and address lines, data from write bit line are written onto the CELLS 0, 5, 10, and 15.

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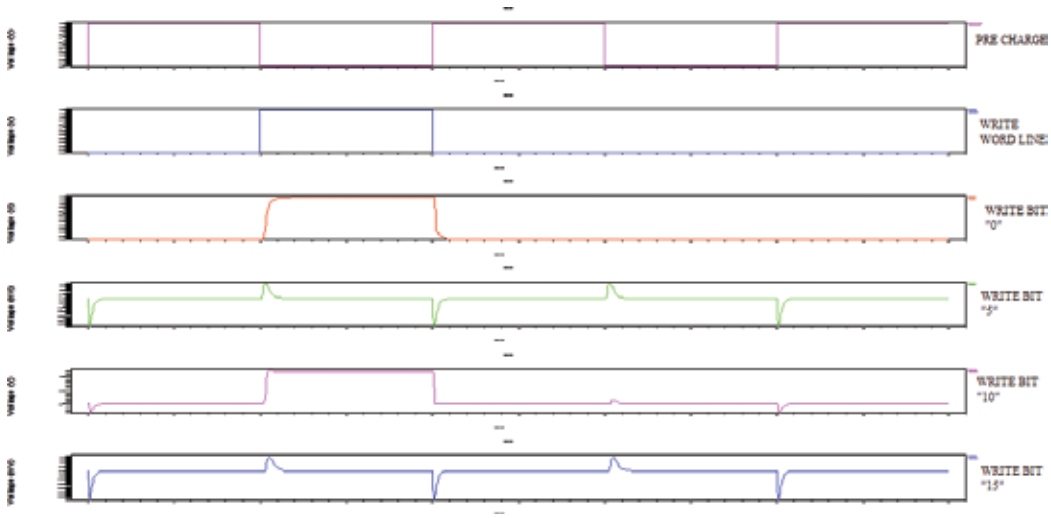

Figure 11. Writing waveform.

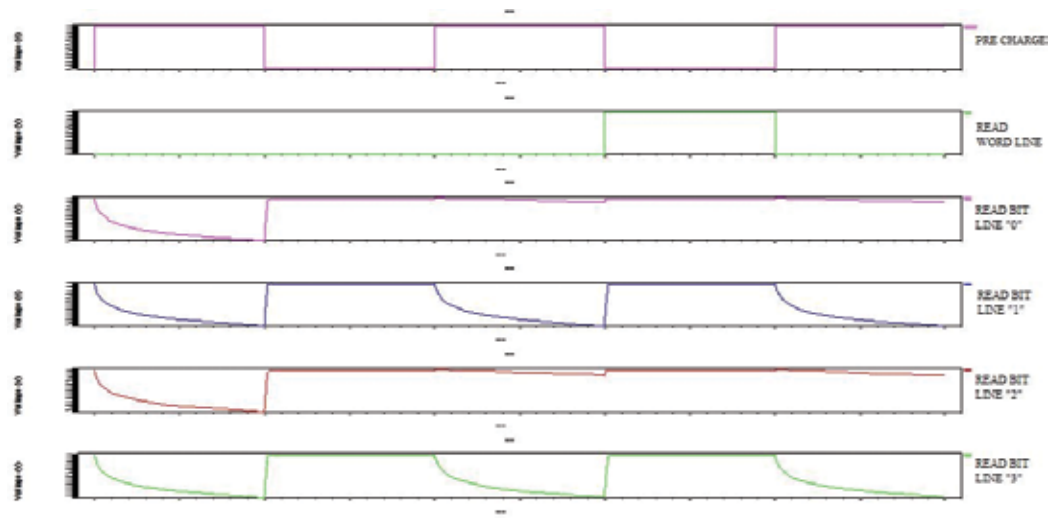

Figure 12. Reading waveform.

For the time period 20–30 ns, PRECHARGE is high, reading and writing both turned off, and data are stored in the cell.

For the time period 30–40 ns, PRECHARGE is low, writing is turned off. Reading is on as READ WORD LINE is turned on. Address line selects the cells. Using the reading decoder and address lines, data are read from the CELLS 0, 5, 10, and 15 and transferred to the output circuitry of the required column.

For the time period 40–50 ns, PRECHARGE is high after performing sensing and amplification of the required data. Data are read from READ BIT LINES 0, 1, 2, and 3 together (**Figure 13**).

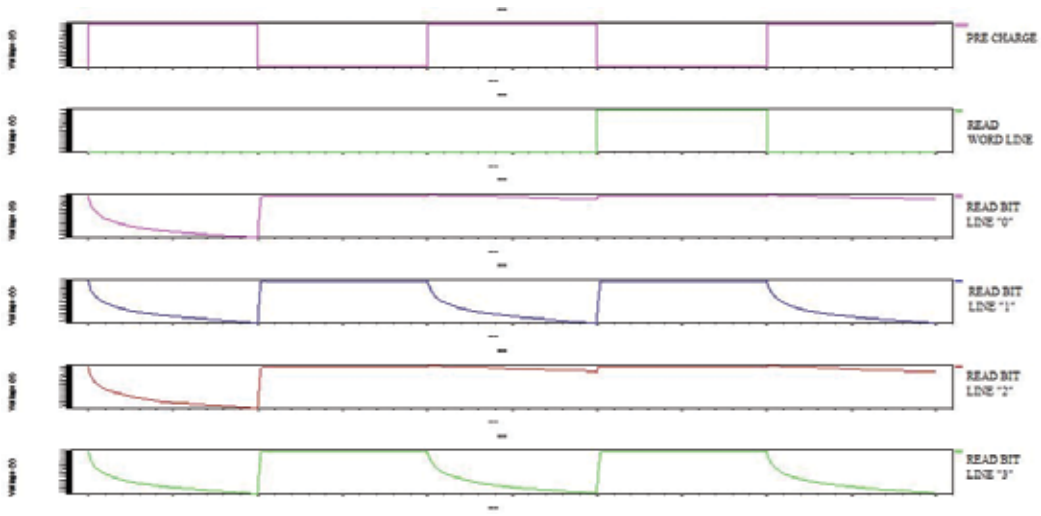

Figure 13. Final read output.

4. Conclusions

A memory architecture has been proposed in this chapter. From the analysis of static noise margin (SNM) for SRAM cell, it could be concluded that the SRAM 8T cell has a higher SNM than the SRAM 6T and SRAM 11T, that is, SRAM 8T cell has a greater noise tolerance. The only drawback of the SRAM 8T and SRAM 11T is the area overhead over the SRAM 6T cell. In order to reduce this area overhead, DRAM-based memory systems are being used. Different types of DRAM cell structures have been used in the study. A novel structure using P-type-gated diode-based capacitor has been utilized in this work. The average power consumption for the structure is lower than those being implemented in the study. A significant reduction in both write and read access time has been achieved when the structure is compared with a similar structure. Area layout for the structure shows the reduction in the area overhead compared to the other implemented designs. A full memory subsystem implementation depicts the working of the architecture in practical working environment, achieving greater results. The memory subsystem implemented could successfully store 16 bits of data and the saved data could also be read effectively.

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Chapter 7

High Voltage Energy Harvesters

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Chee Huei Lee, Rong Zhao and Moe Z. Win

Additional information is available at the end of the chapter

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Abstract

Green energy helps in reducing carbon emission from fossil fuel, harvesting energy from natural resources like wind to power consumer appliances. To date, many researches have been focusing on designing circuits that harvest energy from electromagnetic signals wirelessly. While it could be designed to be efficient, the generated power however is insufficient to drive large loads. Wind energy is highly available environmentally but development of small-scale energy harvesting apparatus aiming to extract significant power from miniature brushless fan has received limited attention. The aim of this chapter is to give audience an insight of different voltage multipliers used in energy harvester and knowledge on various circuit techniques to configure voltage multipliers for use in different high voltage applications. These include AC-DC converter, AC-AC converter and variable AC-DC converter.

Keywords: alternating current, capacitor, charge pump, circuit, generator, converter, diode

1. Introduction

Evolution of portable electronic devices over the past decades has led to surge in demand of batteries. The issues arise from using the batteries include maintenance cost, limited durability and associated environmental pollutions. Further, the size of battery becomes the bottleneck for miniaturization of electronic device. **Table 1** shows the severity of lead battery pollution in some developing regions due to unregulated and immature recycling process [1]. Renewable energy sources have become the viable solution to overcome the limitations of batteries. Although such type of energy sources from wind and hydropower have long existed, they are used mainly to power electrical appliances in streets and buildings with large turbines rated at hundreds of kW [2]. Solar energy is another attractive option due to its high availability. However, the cost of solar panel is high and the manufacturing process is associated with air pollution. RF energy harvester has become a hot research topic

Region	Number of sites affected	Impacted Population
South America	15	322,800
South Asia	10	287,000
Africa	8	154,000
Southeast Asia	34	123,500

Table 1. Ranking of lead pollution severity by region [1].

in recent decades with emergence of RFID technology. Nevertheless, it is only useful for low power applications [2] and is thus not relevant to the interest of this chapter. Other available ambient energy sources include thermal energy, mechanical vibration and human activities. Implementation of small scale wind energy harvester is possible by using miniature brushless fan as a AC generator. Wind energy harvester is chosen to be focus of the works in the chapter as it fits the goal of sustainable development to create intelligent, autonomous and eco-friendly systems. Practically, windy condition can be created when moving on a transport or resting under a blowing fan. A well-designed energy harvester circuit can enhance the power generation efficiency.

Practically, it is desirable to boost the output voltage of energy harvester by connecting it to a voltage converter. The most intuitive way of boosting the output voltage of energy harvester is using step-up transformer. However, additional rectifier circuit is needed to convert the secondary voltage of transformer into DC voltage. Further, the size and cost of the transformer is a concern for realizing miniature energy harvester. Switch capacitor circuits [3, 4] and boost converters [5–7] could be used to serve the same purpose. However, they require additional clock signals at the input and is thus not feasible for use in energy harvester. Meanwhile, diode capacitor based voltage multipliers [8–14] are more preferred to be used in energy harvester circuit due to its simplicity in circuit architecture and low cost. The works presented in this chapter focus on using miniature wind energy harvester to generate high voltage (>10 V) for powering portable devices at milliwatt level.

Three different architectures of energy harvesters are detailed in this chapter. This first wind energy harvester adopts Cockcroft-Walton voltage quadruppler and a 2.4 W brushless fan to achieve more than 17 V DC at output. The second energy harvester is a AC to AC converter that uses a self-powered inverting op-amp to achieve the purpose. Lastly, a variable DC voltage generator is presented. It is formed by connecting a voltage doubler to the output of self-powered op-amp. They are detailed in Section 3. In Section 2, various architectures of existing voltage multipliers are exploited and reviewed.

2. AC to DC converter

In this section, the fundamentals of the voltage multipliers are reviewed.

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2.1. Villard voltage doubler

The most fundamental component of a voltage doubler is basically a voltage clamp which was invented by Paul Ulrich Villard [8]. As shown in **Figure 1(a)**, it consists of only a shunt diode and a series capacitor. During negative cycle of input voltage, diode D1 conducts and voltage across capacitor, Vc is charged to a value that is equivalent to peak amplitude of AC input voltage, Vp. In the next positive cycle, voltage seen at output terminal hit peak value of 2Vp as the capacitor now behaves as battery with DC potential of Vp. Overall, the resulted output voltage waveform is a similar copy of input AC voltage waveform but with DC level shifted from 0 to Vp. Nevertheless, voltage clamp cannot be used directly to power DC load due to unregulated output. Note that the analysis described above ignore the forward biasing voltage of diode, V_{D1} for ease of explanation. In practice, the maximum output voltage of diode voltage clamp is $2V_p - V_{D1}$. **Figure 1(b)** shows the comparison of input and output waveform.

2.2. Greinacher voltage doubler

Greinacher overcomes the deficiency of Villard voltage doubler by connecting an envelope detector in cascade with it at the output [9]. As shown in **Figure 2(a)**, the envelope detector consists of a series diode, D2 that steer current generated from voltage clamp into storage capacitor. This operation occurs at positive cycles of input voltage whereby diode D2 is forward biased and diode D1 is reverse biased or open-circuited. As shown in **Figure 2(b)**, the capacitor, C2 is charged up to 2(Vp−Vd) with voltage drops across diodes taking into consideration. During negative cycles, diode D2 acts as a potential barrier to ensure that only capacitor C1 is charged at that instance. With charging and discharging actions of storage capacitor, C2 across positive and negative operating cycles, the ripple content of voltage signal

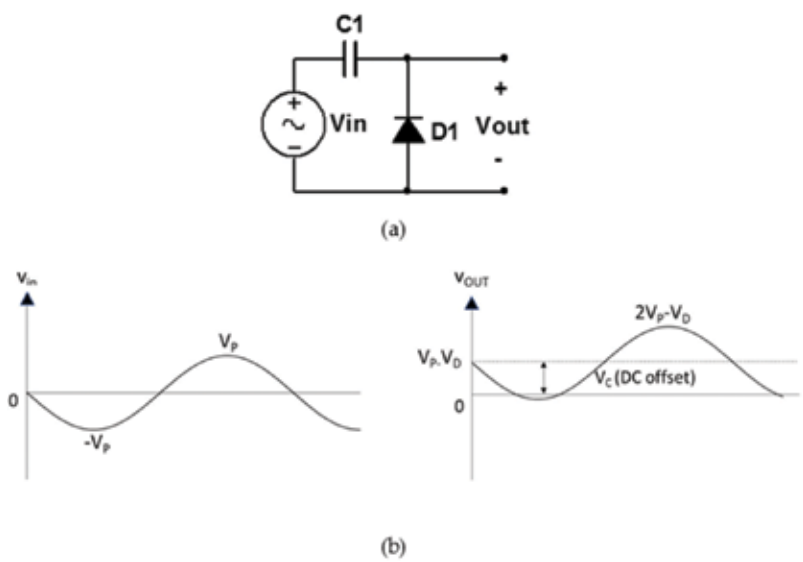

Figure 1. (a) Villard voltage doubler circuit and (b) its corresponding input/output waveform [8].

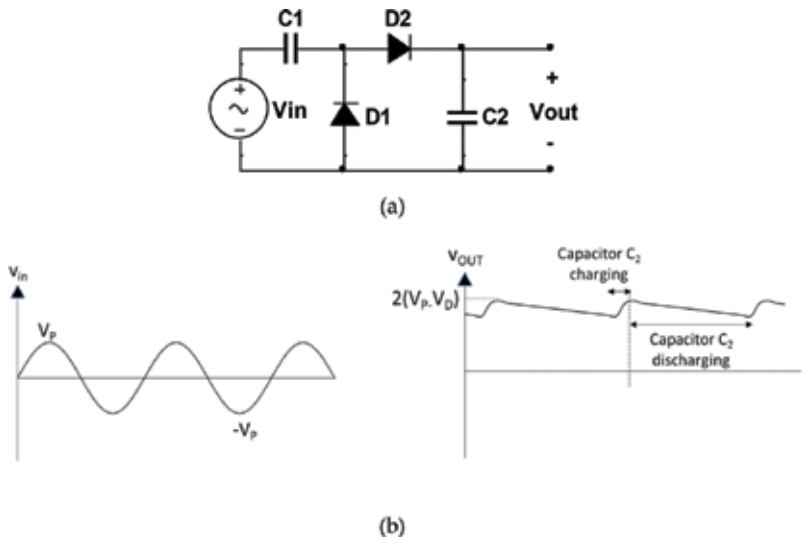

Figure 2. (a) Greinacher voltage doubler circuit and (b) it's corresponding input/output waveform.

at the output is greatly reduced or smoothed. Intuitively, the efficiency of the voltage doubler could be improved by choosing diodes that have low forward bias voltage.

2.3. Cockcroft-Walton voltage multiplier

In 1932, John Douglas Cockcroft and Ernest Thomas Sinton Walton developed a voltage multiplier for powering their particle accelerator [10]. The circuit architecture proposed is basically cascading stages of Greinacher voltage doubler and thus it is also known as Greinacher voltage multiplier. With the cascading connections described, the output voltage could be further boosted by arbitrary times higher but at the cost of reduction in current drivability. Also, the output impedance increases proportionally with the number of multiplying stages as more stage capacitances are connected in series. **Figure 3** illustrates the circuit architecture of Cockcroft-Walton voltage multiplier. Ideally, the n-cascading stage voltage doublers produces 2n times increased in output voltage.

In practice, the output voltage of Cockcroft-Walton voltage multiplier drops significantly from ideal prediction especially when the number of multiplying stages increases and significant loading current occurs at output. The regulation voltage, V_{Reg} which measures the drop in output voltage from ideal condition could be calculated as follows:

$$V_{Reg} = \left[I_{Load}\left(N^2 + 9N^2/4 + N/2\right)\right]/12fC \tag{1}$$

Where,

I_{Load} is the load current (Amps)

C is the stage capacitance (Farads)

f is the AC frequency (Hz)

N is the number of stages.

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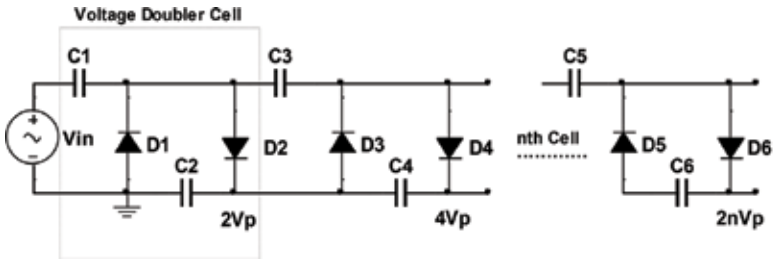

Figure 3. N-stage Cockcroft-Walton voltage multiplier circuit [10].

Hence, the DC output voltage could be written as:

$$V_{OUT} = N(V_P - V_D) - V_{Reg} = N(V_P - V_D) - \left[I_{Load}\left(N^2 + 9N^2/4 + N/2\right)\right]/12fC \tag{2}$$

Meanwhile, the ripple voltage at the output of voltage multiplier is given as:

$$V_{Rip} = [I_{Load}N(N+1)]/2fC \tag{3}$$

Based on (1) and (2), the loading impact on output voltage could be minimized by increasing the values of stage capacitances and frequency of input AC voltage. The performance of Cockcroft-Walton voltage multiplier will further deteriorates if the stray capacitances at coupling nodes are significant fractions of stage capacitances. Therefore, it is not suitable for applying on monolithic integrated circuits.

2.4. Bridge voltage multiplier

So far, the voltage multiplier circuits discussed in previous sections are classified as half-wave type since voltage at output appear as single polarity (Positive or minus) with respect to ground of input source. Instead, voltage doubler can be implemented using bridge circuit (Delon circuit) whereby two peak detectors with opposite polarities are stacked in series and fed by a common AC source (**Figure 4**). Thus, the voltage tapped across the outputs of peak detectors is twice the amplitude of AC source ideally. The orientation of diode determines the polarity of peak detector output since it only conducts either half of the operating cycle. As compared to Greinacher voltage doubler, there is no voltage clamp needed in bridge type voltage doubler for achieving the same purpose.

Similarly, the half-wave Greinacher Voltage Doubler/Multiplier described in previous section could be extended to full-wave bridge configuration by stacking the negative version of it in series. **Figure 5** illustrates the circuit schematic of full-wave Greinacher Voltage Doubler. The upper half version of the circuit is a positive voltage doubler whereby the lower half version is a negative voltage doubler. The resulted output voltage is double of those in half-wave version. Also, the voltage rating of stage capacitors (C3, C4) only need to be halved of those used in half-wave version for generating the same output voltage. As the ripple frequency of full-wave doubler is twice the supply frequency, it has lower ripple content than the half-wave voltage doubler. However, there is no common ground between the input and output.

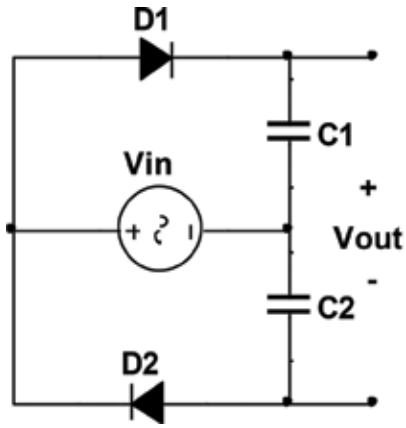

Figure 4. Delon bridge circuit.

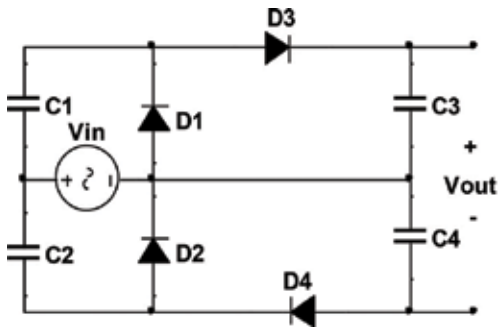

Figure 5. Full-wave Greinacher voltage doubler circuit.

2.5. Dickson charge pump

Dickson charge pump [11] was invented to overcome the deficiency of Cockcroft-Walton voltage multiplier in dealing with stray capacitances. **Figure 6** shows the schematic of Dickson charge pump circuit where the output stage is a peak detector to hold the multiplied voltage at final stage. Under this configuration, clock signals with orthogonal phases are fed separately into capacitive coupling nodes at odd and even stages of charge pump. As compared to Cockcroft-Walton voltage multiplier, the stage capacitances in Dickson charge pump are parallel connected instead of series connected. The main advantages of this configuration are that the stray capacitances have little impact on the performance of voltage multiplier even with relatively high value. Also, the current drive capability is not affected by the number of multiplying stages. However, it is not suitable for high voltage application since the output node alone need to withstand the multiplied voltage entirely. As a result, the voltage rating of output capacitor becomes the bottleneck of maximum output voltage achievable. In addition to that, the circuit is not feasible for energy harvesting applications since it requires extra feeding of two anti-phase clock signals to operate. The operation principle of Dickson charge pump circuit can be summarized as follows:

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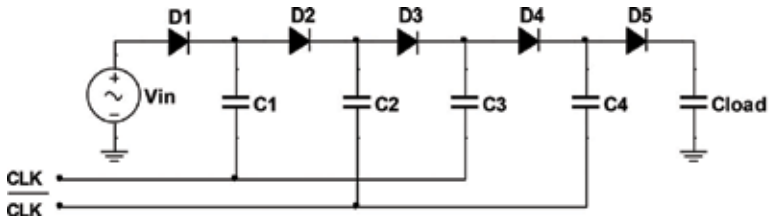

Figure 6. Dickson charge pump circuit.

1. During the zero cycle of the clock pulse, *CLK*, the first diode, D1 at the input stage will be forward biased and charge the stage capacitor, C1 to the peak DC input voltage (Vin).

2. As the clock signal, *CLK* goes high and $\overline{CLK}$ goes low, the voltage appears at top plate of C1 is boosted by twice to 2Vin. Under such circumstance, diode D1 becomes reverse biased whereas diode D2 becomes forward biased. Thus, current flows through D2 to charge capacitor, C2 for up to 2Vin assuming negligible voltage drops across diodes.

3. Similar operations described are repeated for next subsequent stages of charge pump voltage multiplier. The final output voltage stored in C4 is captured by a peak detector consisting of diode, D5 and load capacitor, C_{load}.

The output voltage of Dickson charge pump for N multiplying stages could be expressed as follow:

$$V_{OUT} = N(V_P - V_D) \tag{4}$$

In order to improve the efficiency of Dickson charge pump, Schottky barrier diodes should be adopted due to its lower forward biasing voltage. However, such component is not readily available in CMOS technology. In such case, diode connected MOSFET [15–17] is more preferred due to its lower cost, wider availability and receives better support from Process Design Kits (PDKs). **Figure 7** shows different version of Dickson charge pump circuit where conventional diodes are replaced by diode connected MOSFET. Nevertheless, the efficiency of such circuit is no better than those versions with Schottky barrier diodes due to its high threshold voltages and leakages. Although the threshold voltage of MOS transistor could be canceled using external biasing described in [17], the MOS transistor could not swing to "ON" state or "OFF" state fully. This resulted in high conduction resistance, leakage current, and thus lower efficiency. Active diode reviewed in next section presents a better alternative to conventional diode.

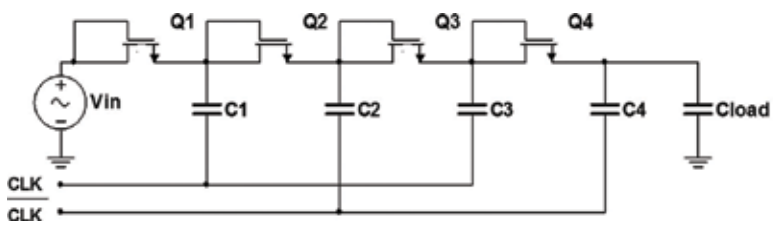

Figure 7. Dickson charge pump circuit based on diode connected MOSFETs.

2.6. Karthaus-Fischer cascade voltage multiplier

For applications where the clock signals are absent, the Dickson charge pump circuit described in previous section could be modified such that the anti-phase clock signals are replaced by input AC source and its corresponding ground connection. This resulted in much simplified circuit as shown in **Figure 8**. The circuit configuration described is also known as Karthaus-Fischer cascade voltage multiplier [12, 13]. It is interesting to note that the unit voltage doubler cell is resembled back to a Greinacher Voltage Doubler. As compared to Cockcroft-Walton voltage multiplier, the inputs of all multiplying stages are parallel connected whereas their outputs are fed into voltage clamp of next multiplying stage. In addition to that, all output peak detectors of multiplying stages share the same ground as input.

During the negative half cycle of the input sinusoidal signal, the pumping capacitors are pre-charged in parallel, and next positive half cycle charged pumping capacitors deliver current to the storage capacitors and output capacitor (CL) connected to the ground node. Input current from the received RF carrier enters to the diodes only half period of the signal in the half wave voltage multiplier.

Nevertheless, the modified Dickson charge pump is still associated with stringent requirement of capacitor ratings. Thus, another version of the charge pump is proposed in [14] whereby the output capacitances of multiplying stages are connected in series with each other instead (**Figure 9**). As a result, the minimum voltage rating required for each output capacitor is only twice of AC voltage amplitude at input. Such modifications also correspond to higher output impedances and thus implementation in full-wave configuration is recommended to reduce the impact of current loading.

2.7. Active diode based voltage multiplier

Active diode based charge pump [18–21] has been introduced lately as a good candidate for replacement of conventional diode in voltage multipliers. As shown in **Figure 10**, it is actually

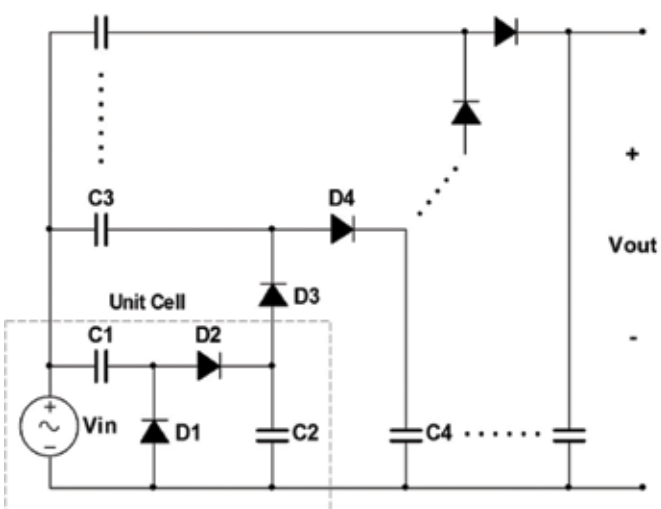

Figure 8. Karthaus-Fischer cascade voltage multiplier circuit.

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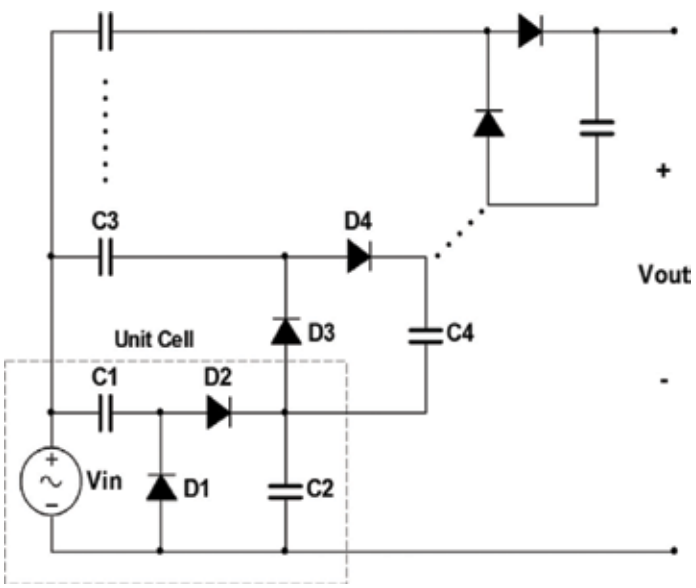

Figure 9. Modified Karthaus-Fischer cascade voltage multiplier circuit.

a comparator controlled active switch which turns on or off depending on the potential difference between anode and cathode terminal. When the voltage at anode terminal is greater than cathode terminal, the comparator output becomes low. As a result, the PMOS transistor connected to the comparator output is turned on and the entire circuit acts like a forward biased diode. The opposite happens when the voltage potential of cathode is greater than anode. It behaves like an ideal diode since only very small voltage difference at the comparator input is needed to trigger the active diode for operation in the desired state. Further, the conduction resistance of the ohmic CMOS switch is small while the reverse current is negligible due to high output impedance of PMOS switch. Thus, it has great advantages of driving low voltage input due to high sensitivity. Several types of voltage multipliers have been reported using active diodes. These include Delon, Dickson and off-chip Cockcroft–Walton types of voltage multipliers. Nevertheless, additional power supply is required for the comparator circuits and the power efficiency degrades with increases in input voltage due to more dominance of conduction loss in transistor switch.

3. Energy harvester circuit

In this section, three small scale wind energy harvester circuits based on voltage multipliers are implemented for different types of applications. Cockcroft-Walton voltage multiplier scheme is adopted for all cases since it is more suitable for generating high voltage with less stringent demand on voltage ratings of capacitors. Also, it is more compact than the conventional transformer used for power generation. The voltage multipliers are designed using discrete components instead of integrated circuits to avoid the complex issues of stay capacitances. They are described in three separate sub-sections below.

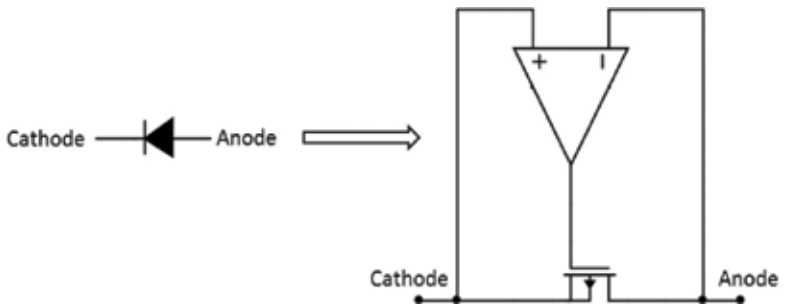

Figure 10. Active diode circuit.

3.1. Quadruppler voltage generator

A small-scale wind energy harvester circuit using voltage quadruppler is presented. As shown in **Figure 11**, it consists of two stages of Cockcroft-Walton voltage doubler that work as AC to DC booster. Schottky diodes, 1N5817 are used in the circuit given its low forward biasing voltage (≈0.3 V for current, Id < 0.1 A). This is essential to keep the efficiency of voltage quadruppler as high as possible. A miniature brushless fan is used in the reverse way as AC generator by removing its commutator circuit. The current rating of the fan is chosen to be high (0.2 A) for better powering of voltage quadruppler. It generates around 3.5 V AC rms voltage at 80 Hz. Meanwhile, the values of stage capacitances (220 μF) are optimized based on frequency of brushless fan (around 50 Hz) when rotating at fan speed. Choosing lower capacitances will enable the voltage multiplier circuit charge up faster to maximum DC voltage but at the cost of lower current drivability. Charging rate becomes slow when much higher capacitances are used and resulted in lower output DC voltage. The load devices used for this demonstration are LEDs. Therefore, voltage regulation issue is less concern since LEDs need very low current (in the order of μAs) to turn on or produce illuminations. The output of the voltage quadruppler is a

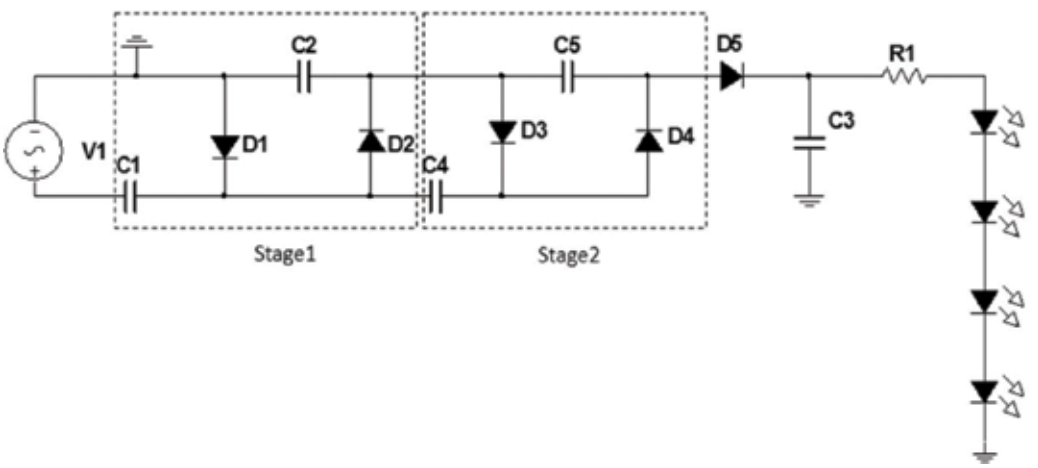

Figure 11. Quadruppler voltage generator circuit.

peak detector that consists of diode, D5 and capacitor, C3. The capacitance value of C3 is chosen to be large since it is used as a battery to power the loads at the absence of AC input voltage. as well as filtering of ripples.

The operation principle of a single voltage doubler stage could be described as follows. During the negative half cycle of the AC voltage source, diode D1 will be forward biased and charge capacitor C1 to the maximum voltage amplitude of the AC source. In the next positive half cycle, diode D1 will become reverse biased and act as a potential barrier to block current from flowing through it. Meanwhile, diode D2 will be forward biased, charging capacitor C2 to twice the maximum voltage amplitude of the source. The same operation repeats at the second voltage doubler which boost output DC voltage to four times of input signal amplitude.

Due to large capacitance of C3, it took around 2 min to charge it fully. The DC output voltage generated under no load condition is around 17 V and 15.5 V with load connected. It matches the calculation in (2) which takes into consideration of voltage drop across diodes. As demonstrated in **Figure 12**, it can light up six blue LEDs for more than 7 min given the high capacity of storage capacitor, C3.

3.2. Self-powered AC voltage booster

In the section, a self-powered AC voltage booster is presented for driving high AC voltage load instead of DC load discussed in previous section. Basically, the circuit comprises of a multi-stage Cockcroft-Walton voltage multiplier and an op-amp, LM324N. Here, the output of the voltage quadruppler is used as a DC supply for powering the op-amp. As compared to [18–21], the op-amp is used as an inverting amplifier and not an active diode. The op-amp requires higher supply voltage to increase the operating range of output voltage when used as an amplifier. Meanwhile, the AC voltage generated from brushless fan is used as an input source for both op-amp and voltage quadruppler. The resistance ratio, R1/R2 can be used to adjust amplification factor of input AC signal injected. Nevertheless, the maximum dynamic range of the output voltage swing is governed by the DC supply from voltage multiplier. Therefore, it is desirable to have larger number of stages of voltage doublers to achieve higher amplification and output voltage swing. Note that the loading current of op-amp will deteriorate the maximum output

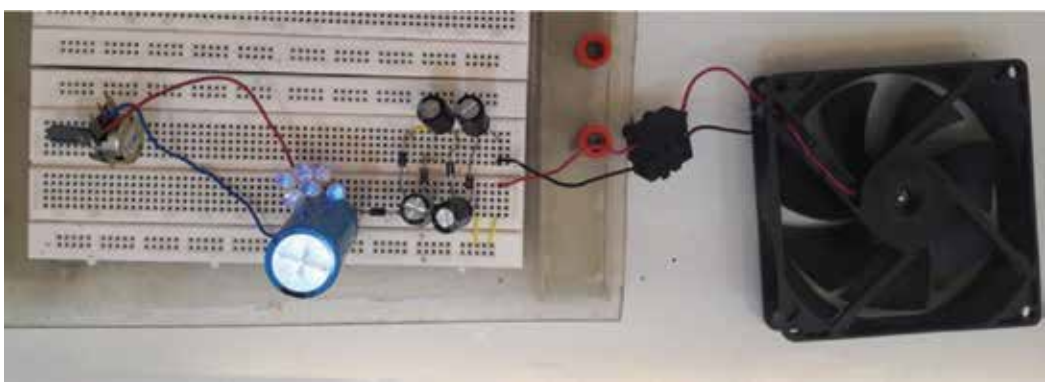

Figure 12. Demo photo of wind energy harvester using voltage quadruppler.

voltage achievable as discussed in Section 2.3. The shunt capacitor, C3 with large value helps improving the current drivability by reducing the output impedance. It also helps providing stable DC power supply voltage to op-amp by smoothing the ripples. **Figure 13** shows the schematic of proposed AC voltage booster using three-stage Cockcroft-Walton voltage doubler.

The functionality of the circuit is evaluated using MULTISIM software. As shown in **Figure 14**, the output AC voltage (Amplitude of 3 V) is twice of input AC source (Amplitude of 1.5 V) for resistance ratio, R1/R2 of op-amp set as 2. There is no distortion in the output as the DC power supply to the op-amp is well above the output voltage swing (6.96 V). Note that the input and output AC voltage are out of phase with each other since inverting op-amp is used in this case.

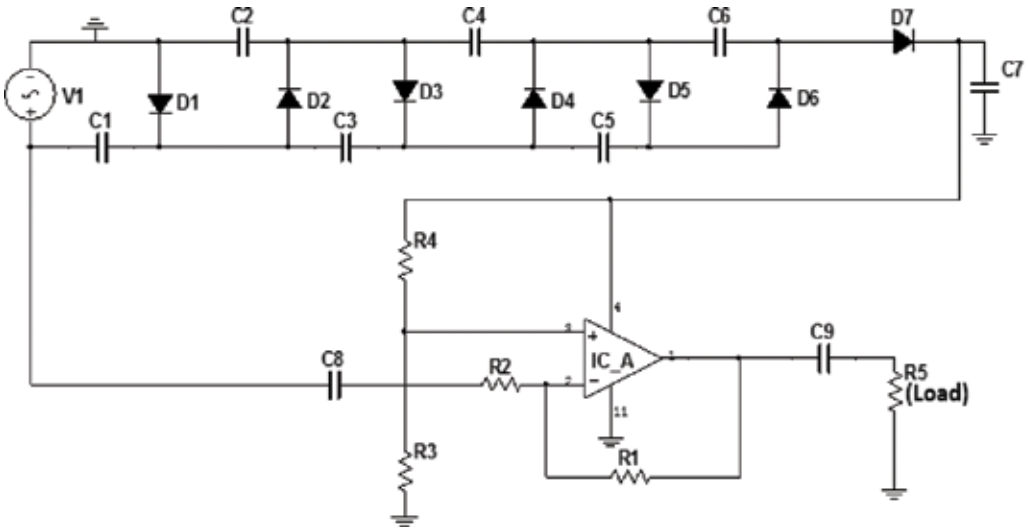

Figure 13. AC voltage booster circuit.

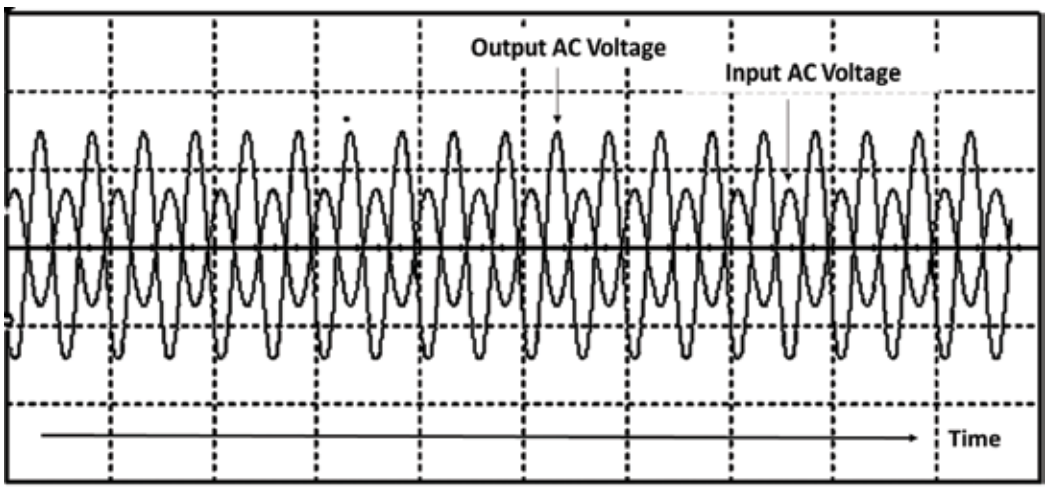

Figure 14. Simulated input and output voltage waveform of AC-AC converter.

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Another version of the circuit (**Figure 15**) is implemented practically using only two stages of voltage doubler (voltage quadruppler) to power the op-amp. A function generator is used as the input of AC source instead for the purpose of analysis. The values of stage capacitances (100 μF) and storage capacitance (1000 μF) are chosen based on consideration on the load drivability of function generator. Meanwhile, the potential divider R3 and R4 act as the DC biasing circuit that determine the operating point of inverting op-amp. The biasing point is chosen to be at the midpoint of supply DC voltage to maximize the dynamic range of output voltage. Here, the impact of resistance ratio, R1/R2 on output AC voltage is studied experimentally. As shown in **Figure 16**, the output AC voltage increases proportionally with the resistance ratio, R1/R2 and saturates as the output voltage swing hits its supply limit. Note that the output AC voltage displayed is normalized with respect to those at unity resistance ratio (R1/R2 = 1). The maximum output voltage achievable using voltage quadruppler is around 1.5 times the input AC source. The result is within expectation since only one stage of voltage quadruppler is used to power the op-amp as compared to three stage voltage doublers described in previous simulation analysis.

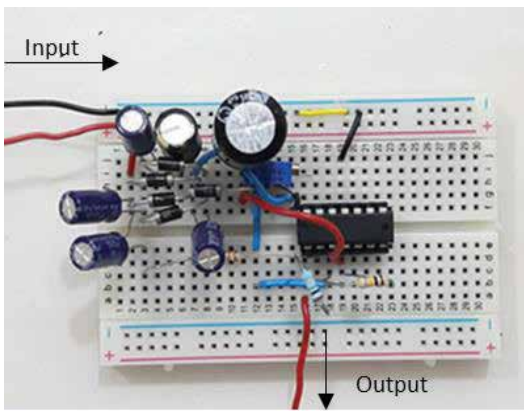

Figure 15. Circuit photo of AC voltage booster.

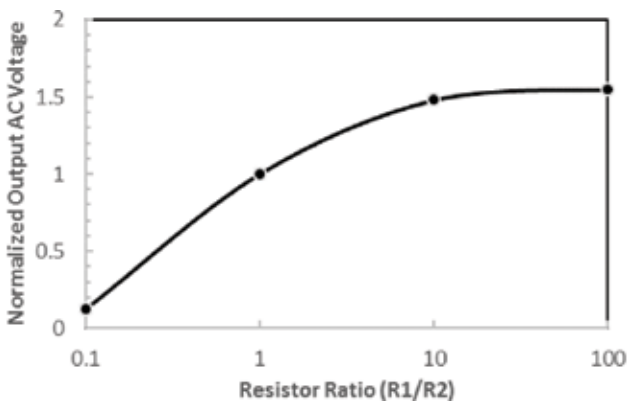

Figure 16. Measured output AC voltage with normalization.

3.3. Variable DC voltage generator

In actual applications, it is desirable to have variable DC power supply to meet the needs for different types of load devices. The conventional voltage quadruppler could be modified further using self-powered op-amp to provide varying supply DC voltage at output. **Figure 17** shows the circuit schematic of variable DC voltage generator. It is similar to AC voltage multiplier circuit presented in **Figure 13** with an exception that additional voltage multiplier stage is attached to the output of op-amp. The circuit works by using the resistance ratio of inverting op-amp to vary the output of connected voltage multiplier. The base voltage of the variable power supply could be further boosted up by tapping the ground connection of voltage multiplier at op-amp output to its own DC power supply node.

Circuit analysis is performed to evaluate the useful range of resistance ratio to be used for producing maximum variation of output voltage. The value of output voltage is normalized with respect to DC power supply from two stages of voltage quadruppler. As shown in

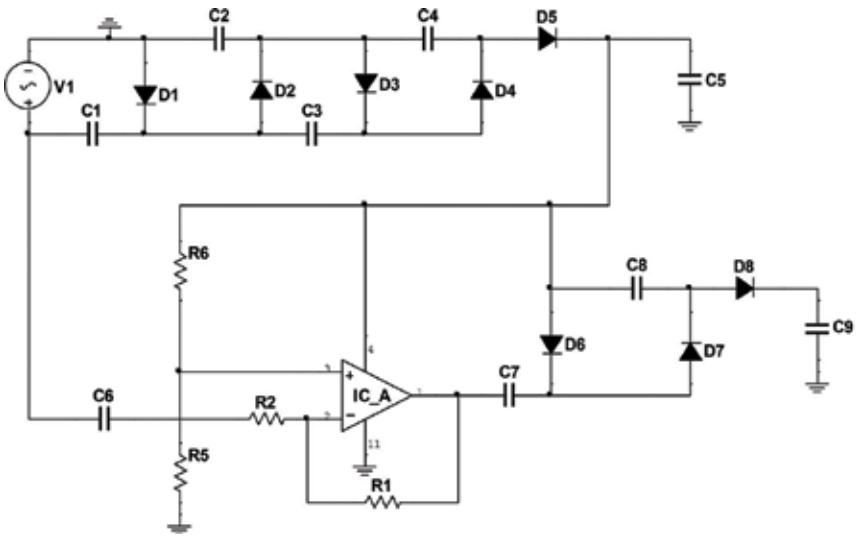

Figure 17. Variable DC voltage generator.

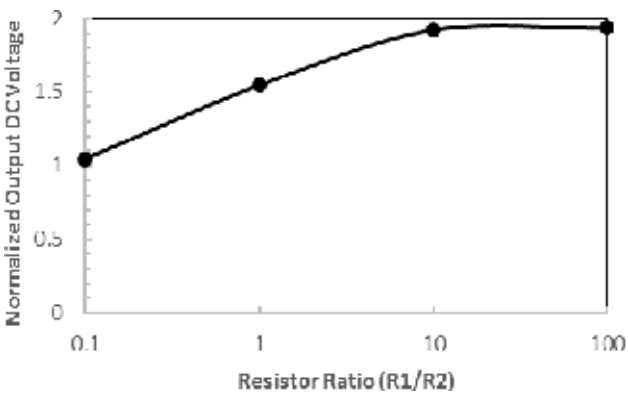

Figure 18. Simulated output DC voltage (normalized) versus resistor ratios of inverting op-amp.

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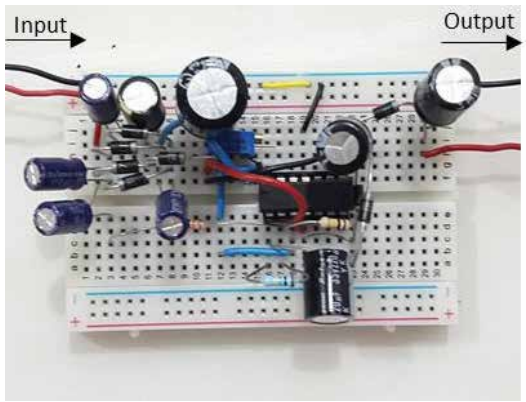

Figure 19. Circuit photo of variable voltage generator.

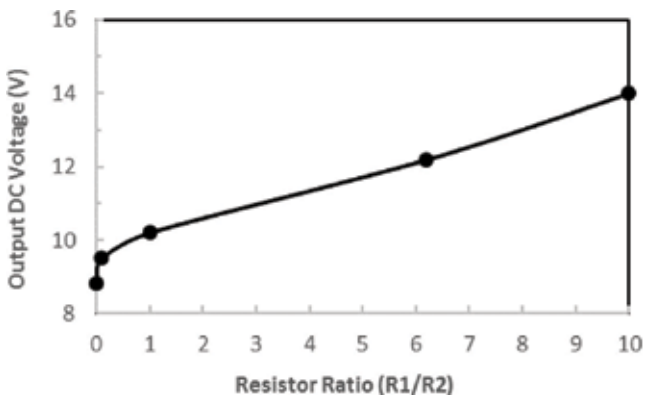

Figure 20. Measured output DC voltage versus resistor ratios of inverting op-amp.

Figure 18, the output DC voltage vary from DC power supply of op-amp to around 1.9 times of it. The useful range of resistance ratio to produce linear variation of output voltage is between 0 and 10 V for this case. Wider tuning range of output DC voltage is possible by cascading more numbers of voltage doublers at the output of inverting op-amp.

As shown in **Figure 19**, the circuit is implemented on a breadboard using discrete capacitors, resistors and an op-amp. It is similar to the version shown in **Figure 15** with an exception that a voltage doubler is connected to the output of op-amp to evaluate its functionality. **Figure 20** shows the variation of output DC voltage across different resistor ratios, R1/R2 of inverting op-amp. The output voltage of the circuit spans from 8.8 to 14 V. This shows that the circuit indeed functions as a variable DC voltage generator.

4. Conclusion

This chapter presents a miniature wind based energy harvester that is designed based on two stages of Cockcroft-Walton voltage doublers. The harvester circuit can generate 17 V DC voltage and light up six series connected blue LEDs for over 7 min when the source is

disconnected. Such circuit can also be used directly for battery charging and power other high voltage device under windy environment. An AC voltage doubler based on self-powered inverting op-amp is also presented. It is attractive for use to replace transformer given its miniature size. Besides that, it could be extended for wireless charging application since boosted AC voltage can be transmitted wirelessly and provide more charging power than those harvest directly from RF signal. The self-powered inverting op-amp circuit could be transformed into variable DC voltage generator when a voltage multiplier is attached to its output. It can vary by 90% of op-amp supply voltage when a voltage doubler is connected at the output. By doing so, the circuit allows flexibility to powered electronic devices of different supply voltage requirements through harvesting energy from wind.

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Section 4

Circuit Test and Analysis

Chapter 8

Experimental Studies of the Electrical Nonlinear Bimodal Transmission Line

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Additional information is available at the end of the chapter

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Abstract

After a few years of calm, the investigations on the dynamic, especially nonlinear, systems returned to the front of the research in non-linear physics. We propose, in this chapter, a study of an electrical nonlinear transmission line, realized in a previous work, to use the latter to highlight certain properties (modulation instability—MI, Fermi-Pasta-Ulam (FPU) recurrence, fragmentation of solitons in wave trains, multiplication(increase) and division of frequencies, etc.), which are observed in several domains in applied physics: hydraulic, artificial neuronal, network physical appearance (physics) of the plasma, and the circulation.

Keywords: nonlinear transmission line, trains of solitons, modulation instability, FPU recurrence, dispersion curve

1. Introduction

Nowadays, the study of electrical nonlinear transmission lines (NLTLs) progresses in both the theoretical field [1, 2] and technology [3–5]. The tools for the simulation of mechanical systems and the study of electrical transmission lines became a major challenge because many electronic systems have nonlinear transmission line (NLTL) modules. The experimental results presented in this chapter are part of an effort to understand the phenomena that occurs in the NLTL. We designed and built the experimental device to perform many investigations on the fundamentals that allow the understanding of the nonlinear effects. Other researchers

focused more on specialized aspects that allowed us to revisit nonlinear effects in a completely new light of research that have marked the history of nonlinear physics in particular.

In Section 2 of this chapter, we present the experimental device realized in a preceding work. In Section 3, we propose an experimental method of determination of wavelength and the velocity phase and velocity group that allowed us to trace point by point the curve dispersion of the line. The effects of fading and nonlinearity are highlighted in Section 4. The phenomenon of modulation instability (MI) is the object of Section 5. In Section 6, we discuss the follow-ups in the periodic recurrence of Fermi-Pasta-Ulam (FPU) in low and high frequencies. Section 7 is dedicated to some applications to use our experimental platform.

2. Overview of the experimental device

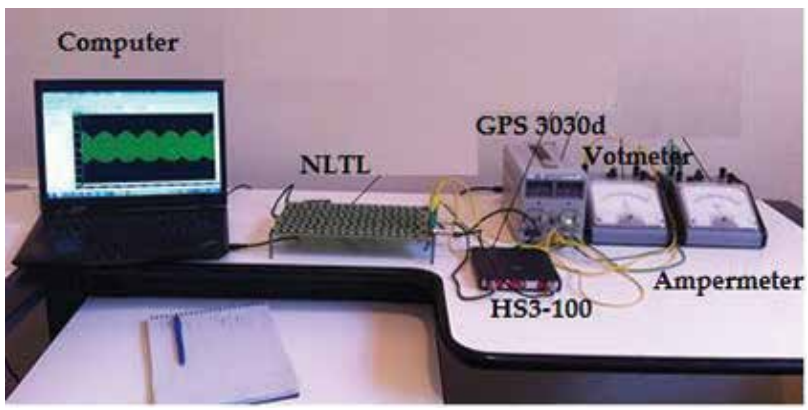

Photo 1: Experimental device.

Computer: for control, acquisition, and data processing;

NLTL: electrical nonlinear transmission line;

HS3–100: which accommodates the arbitrary signal generator and digital oscilloscope;

GPS-3030d: generator of analog tension to polarize the line;

Voltmeter: for the control of the tension of polarization of the line;

Amperemeter: for the control of the current, which crosses the line.

3. Curve dispersion

The first step in the study of an electrical transmission line is to determine its ability to convey electric waves. Indeed, the electric nonlinear transmission line like all wave guides presents a different response depending on the type of the wave introduced.

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3.1. Wavelength determination

To determine the wavelength of a signal, we introduce one low amplitude sine wave in the line input in order to stay in the linear approximation (50 mV), then we put a first probe at the entrance of a cell of order n, then a second probe to a cell located at the position $n + 1$, $n + 2$ until the signals observed from the two probes are in phase. Thus, we determine the wavelength expressed in terms of cell number.

We have at the determined level the wave number k given in the relationship (Eq. (1)):

$$k = \frac{2\pi}{\lambda} \tag{1}$$

where k is expressed in rad/cel and λ is a wavelength.

However, this method is quite unclear, and it is rare to see a wavelength that is always equal to an integer multiple of the number of cells. However, this step has the advantage to confirm that the wavelength is greater than the cell, which allows considering the use of a method more precise by calculating the phase velocity of the wave.

3.2. Determination of the phase velocity

Staying in the linear approximation, we introduce the input of line at low amplitude (50 mV) sine wave and visualize the signals collected by two sensors located on two consecutive cells. We then determine the phase of the wave velocity by choosing a point of the wave, which has the same phase (e.g., maximum). This phase velocity is expressed in cell/s (**Figure 1**). We determine then the number of waves by the relationship (Eq. (2)):

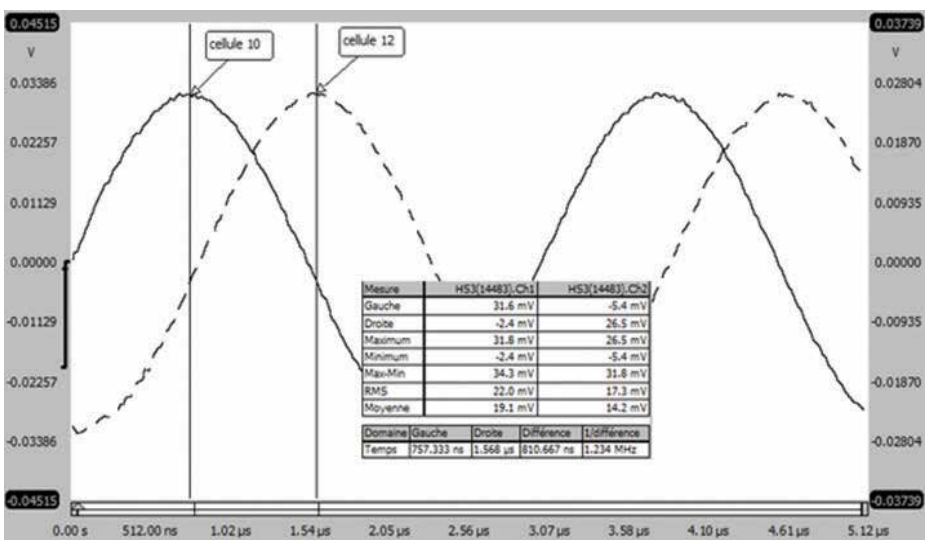

Figure 1. The phase velocity of the wave measured by taking the signals at the entrance of two inductors of the same values that are consecutive. Then we determine the difference of time between these two points, making sure that the two points of the wave are the same phase; cells 10–12, $f = 330$ kHz, $\Delta t = 810.667$ ns, $v_{\varphi} = 2.46\ 106$ cells/s.

$$k = \frac{\omega}{v_\varphi} = \frac{2\pi f}{v_\varphi} \tag{2}$$

where f is the frequency of the incident wave and v_φ the phase velocity.

We determine then the wave number k, for all frequencies available by the system, which allow us to determine the curve dispersion of the line.

3.3. Frequency modes

We present, in **Figure 2**, the curve of dispersion obtained by the theoretical calculation [1] (solid lines) and the experimental points determined by the above-described method (filled triangles). We note a good agreement between our experimental results and the theoretical results. The frequencies of experimentally determined cuts $f_{C1} = (590 \pm 15)$ KHz, $f_{C2} = (830 \pm 20)$ KHz, and $f_{C3} = (975 \pm 25)$ KHz are in good agreement with the theoretical values $f_{C1} = 550$ KHz, $f_{C2} = 807$ KHz, and $f_{C3} = 970$ KHz, respectively. These cut-off frequencies delimit several areas of the dispersion curve, which correspond to modes of propagation of individual waves in the transmission line.

3.3.1. Low frequency mode

Low frequency (LF) mode is the branch of the curve dispersion that lies below the first cutoff frequency.

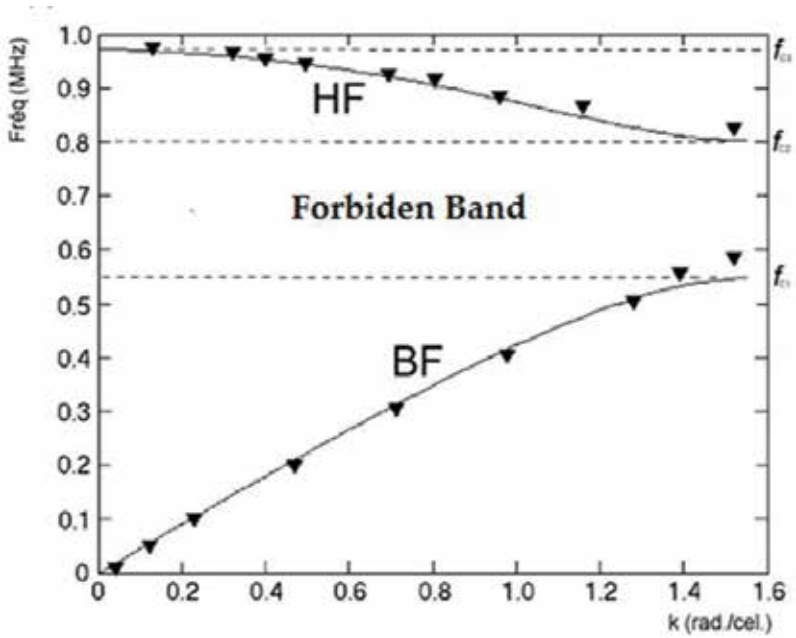

Figure 2. Comparison between the curve dispersion experimental triangles and that obtained by calculation (continuous line) for the bimodal transmission line ($L_1 = 220\ \mu F$, $L_2 = 470\ \mu F$ with polarization voltage of line $V_0 = 1.5$ V).

3.3.2. High frequency mode

High frequency (HF) mode is the branch of the curve of dispersion which lies between the second and the third cut-off frequency f_1 and f_2, respectively. It is noted that practically there is no science that has managed to determine the curve dispersion in HF mode with much precision than that presented in the present work. This is due to the fact that, on the one hand, in HF mode signals are weak compared to those of the bi-frequency (BF) mode, and, on the other hand, the quality of the experimental device impacts the measures as we have used a more accurate methodology.

3.3.3. Forbidden band

The forbidden band is a range of frequency between the cut-off frequencies of f_2 and f_3. In this area, other physical laws [1] govern the wave propagation.

4. Nonlinearity and dissipation effects on the signal

Dissipation and dispersion phenomena affect the wave propagation in nonlinear electrical line in various proportions.

4.1. Effect of dissipation

Because of the presence of dissipative element in the line, signals introduced at the entrance of the line undergo a weakening that increases with the distance traveled in the line. Impairment affects the wave in a uniform manner, it is a linear phenomenon that leads to a global change in the amplitude of the wave; however, the overall shape of the wave remains intact. In order to observe the effects of wave dissipation in the nonlinear electrical line, we have to diminish the effects of the nonlinearity. To do so, we are in an almost linear approximation by introducing into the line of very low amplitude waves.

We see, in **Figure 3**, the sine wave introduced at the entrance of the line keeps its intact shape to the 144th cell; however, we note a weakening of the signal, which sees its amplitude virtually halved.

Note, finally, that the weakening of the signal affects all signals introduced in the line. It is important to note that the HF mode signals are more sensitive to the effects of dissipation; also explained by the fact that high-frequency inductors have impedances higher than in BF mode. This often makes the phenomena more difficult to observe in the HF mode than in BF mode.

4.2. Effect of the nonlinearity

To observe the effects of nonlinearity in the nonlinear transmission electric line, the amplitude of the signal introduced into the line is increased. Indeed, by increasing the amplitude of the signal, the voltage varies significantly around the tension of polarization V_0 of the diodes varactor thus leading their operating point to move on a significant range of value around the Q_0 resting on the characteristic C(V) (**Figure 4**) point. The various points of the signal, not meeting the same value of the capacity, then move at different velocity, thus leading to a dispersion of the signal.

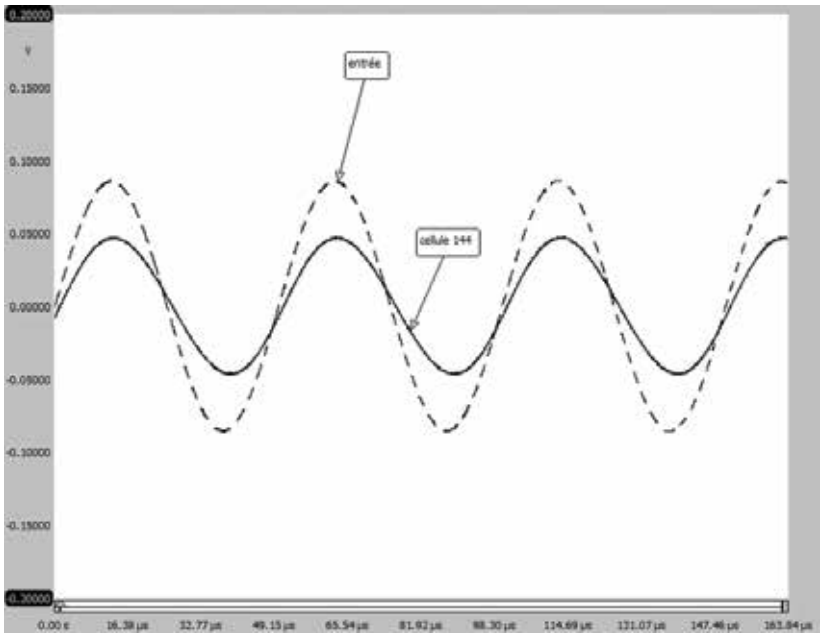

Figure 3. Evolution of an input signal of small amplitude sinusoidal shape (*f* = 20 KHz, V signal = 50 mV) after crossing a stretch of 144 cells of the nonlinear electrical line bi-inductance. Note the linear weakening of the signal keeps sinusoidal shape intact.

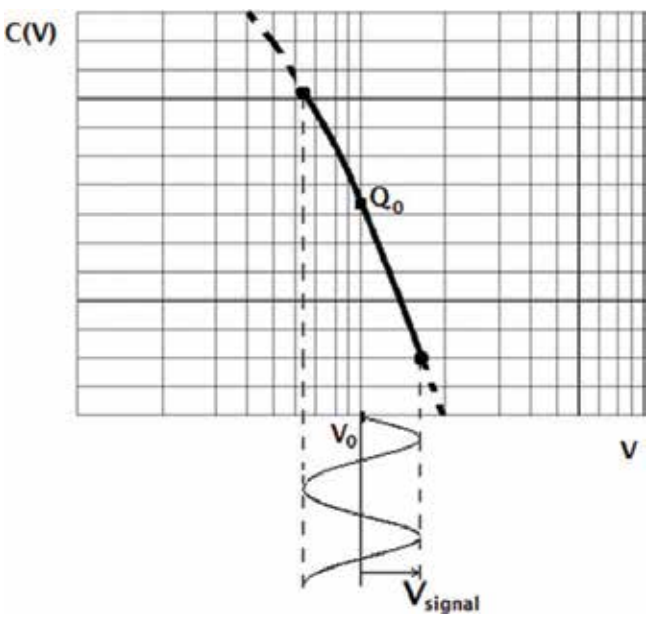

Figure 4. Vsignal of amplitude input voltage is superimposed on the bias of the varactor diode voltage to impose on them an operating point located on the one hand and the resting point Q_0 on the other hand.

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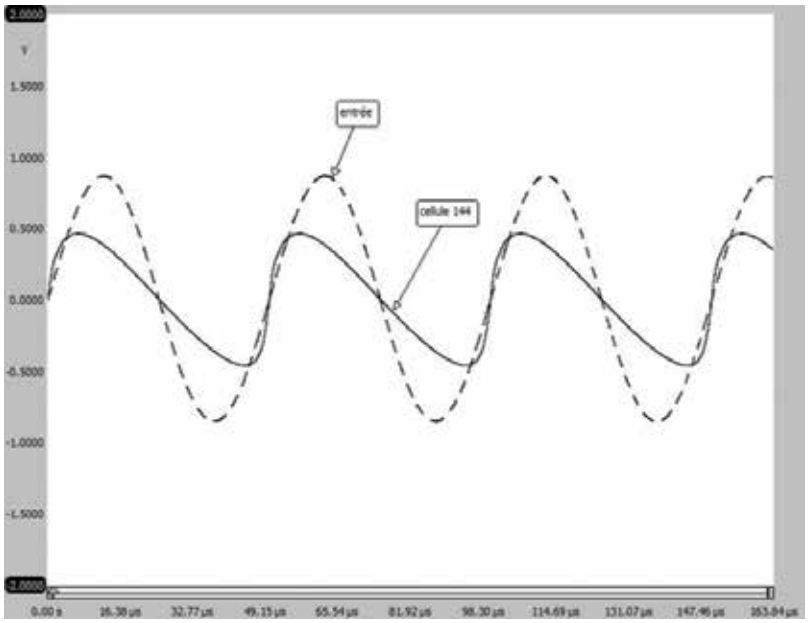

Figure 5. Nonlinearity caused by crossing a stretch of line of 144 cells induces a very strong dissymmetry of the signal, which then presents a flat forehead.

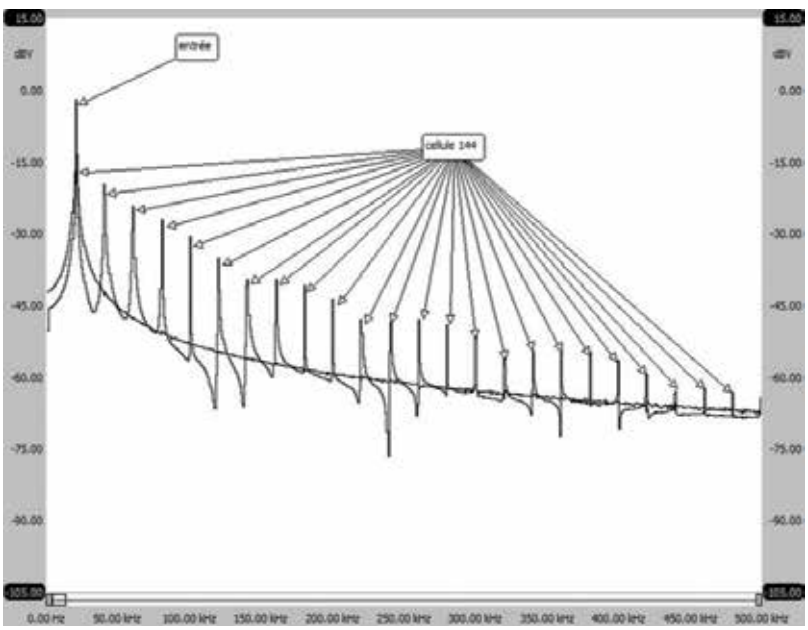

Figure 6. Illustration of the spreading of the wave in the spectral domain due to the effects of nonlinearity after crossing a section of power line nonlinear of 144 cells by a sinusoidal signal of frequency f = 20 kHz, amplitude Vsignal = 1.5 V for a polarization of the V_0 line voltage = 1.5 V.

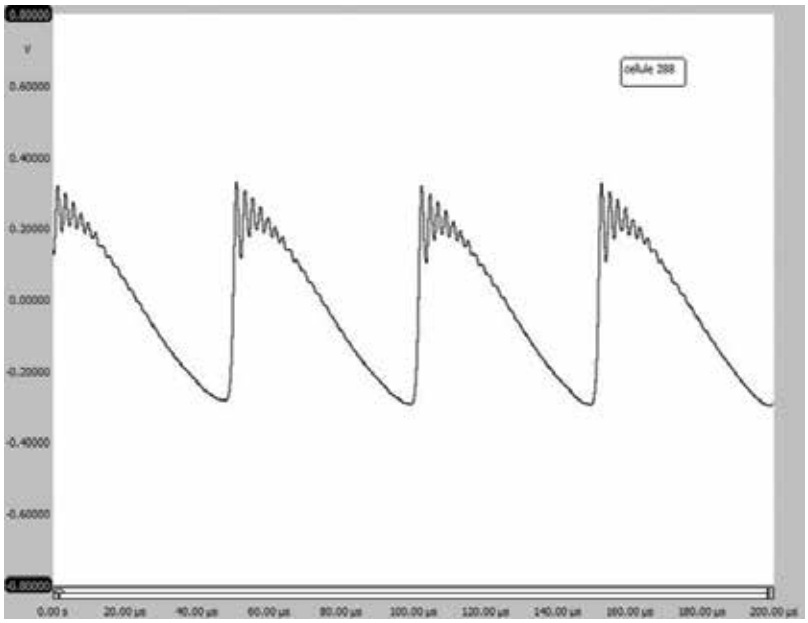

Figure 7. Destruction of the sine wave kept after crossing a section of electrical nonlinear line aft 288th cells by a sinusoidal signal of frequency f = 20 kHz, amplitude Vsignal = 1.5 V, and a polarization of the line voltage V0 = 1.5 V.

The signal can then undergo a significant distortion as it penetrates into the line. We present a characteristic effect related to the effects of nonlinearity of the signals (in **Figure 5**). It is obvious that the 144th cell wave become very asymmetrical, as phases of the various points of the wave velocity are different.

In fact, everything happens as if parts of the wave with large amplitudes are moving faster than low amplitude. The wave starts to break down; it shows more and more overtones, thus reflecting the complexity of the shape and explains why nonlinearity leads to a spreading of the wave (**Figure 6**).

Ultimately, the wave front flattens completely; called shock wave similar to the phenomenon observed in the aerodynamic field when a mobile starts to move at a speed greater than the speed of sound. At this moment, the wave breaks (**Figure 7**).

5. Modulation instability

Modulation instability (MI) is a universally known phenomenon-affecting continuum. It reflects the ability of a weakly perturbed wave to undergo very strong modulations that finally break down in a stable wave [6–8] train. Historically, the MI studied in hydrodynamic fields [9–11] and subsequently the phenomenon observed in other media of propagation of the waves such as electrical transmission lines nonlinear [12–15] optical guide. The MI can occur in space or in time domain. Benjamin and Feir were the pioneers of the study of the MI. In 1967, they studied the evolution in time of MI and demonstrated both theoretically and

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experimentally that a uniform continuous wave train could be unstable to the disruptions that modulate its envelope [7, 8]. The impact of the work of Benjamin and Feir, often called instability of Benjamin-Feir, is mainly in hydrodynamics.

5.1. Criterion of modulation instability in the electrical bi-inductance line

In a previous work, Pelap [1] conducted a theoretical study of a power nonlinear transmission line bi-inductance. He first showed that the wave propagation in the line governed by an equation of type Ginzburg Landau complex (GLC) then sought solutions of the equation in discrete semi-approximation. The approach was different from that adopted by Lange and Newell for hydrodynamic fields [16] to establish a criterion of instability for a plane wave propagating through a nonlinear bi-inductance linear and weakly dissipative inductance. The wave is unstable under modulation if the pseudo-product (Eq. (3)) is positive that is:

$$P_r Q_r + P_i Q_i > 0 \tag{3}$$

where P_r, P_i, Q_r, and Q_i are, respectively, the real and imaginary coefficients of dispersion terms P and of nonlinearity Q .

If the pseudo-product (Eq. (3)) is positive, it means then that the wave is unstable under the modulation and the system will be the seat of an MI.

We study, for our electrical nonlinear bi-inductance transmission line, the evolution of the pseudo-product in HF mode (**Figure 8**) and the BF mode (**Figure 9**).

Knowledge of the values of the critical wave in the HF mode allows us to clarify if areas of the curve dispersion of the wave are stable under the modulation or not (**Figure 10**). Thus, we are building a decision tool that allows us in our different investigations to determine the frequency of the signals that we send in the line for the observation of specific phenomena properly.

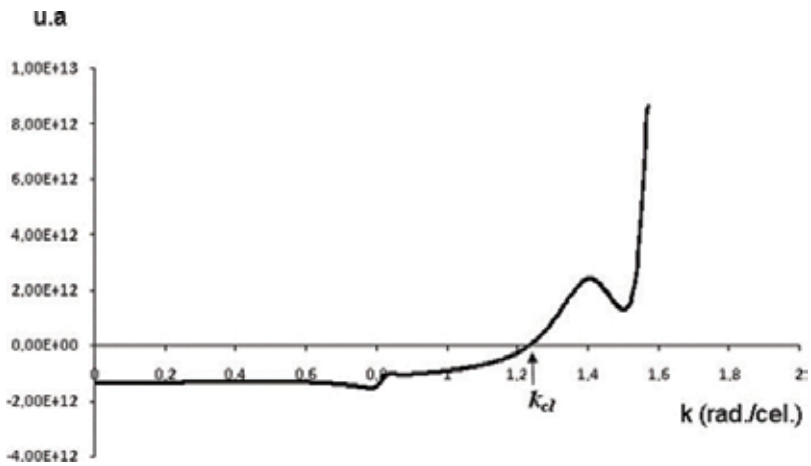

Figure 8. Shape of the pseudo-product in BF mode for the inductance bi line. The value of the wave number is critical in this mode which marks the separation between the area of stability, and the zone of instability is k_{cl} = 1.23305 rad./cel.

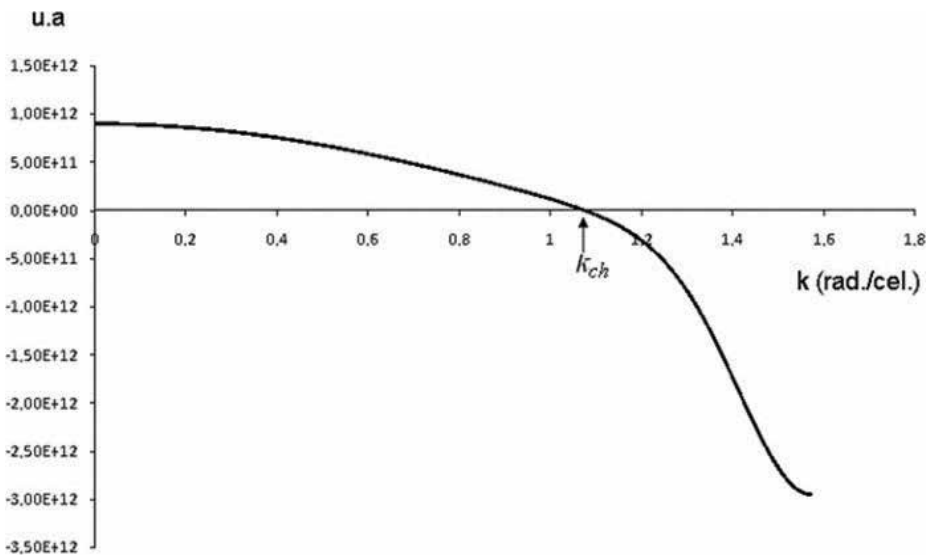

Figure 9. Changing of the pseudo-product in HF mode for the inductance bi line. The value of the wave number critical separation between the area of stability and the zone of instability in this mode is k_{ch} = 1.07595 rad./cel.

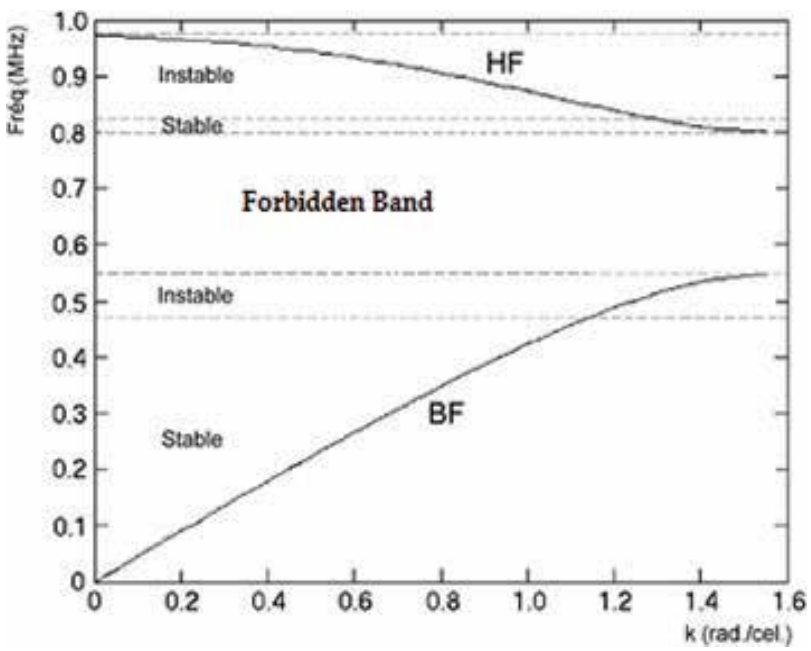

Figure 10. Delimitation of modulation areas of stability and instability of the electric nonlinear bimodal transmission line based on the criterion of modulation instability.

5.2. Observation of MI in the nonlinear bimodal transmission line

We observe modulation instability in the bi-inductance line in the BF mode. To do this, on the one hand, we must choose a signal whose frequency is in the region of modulation

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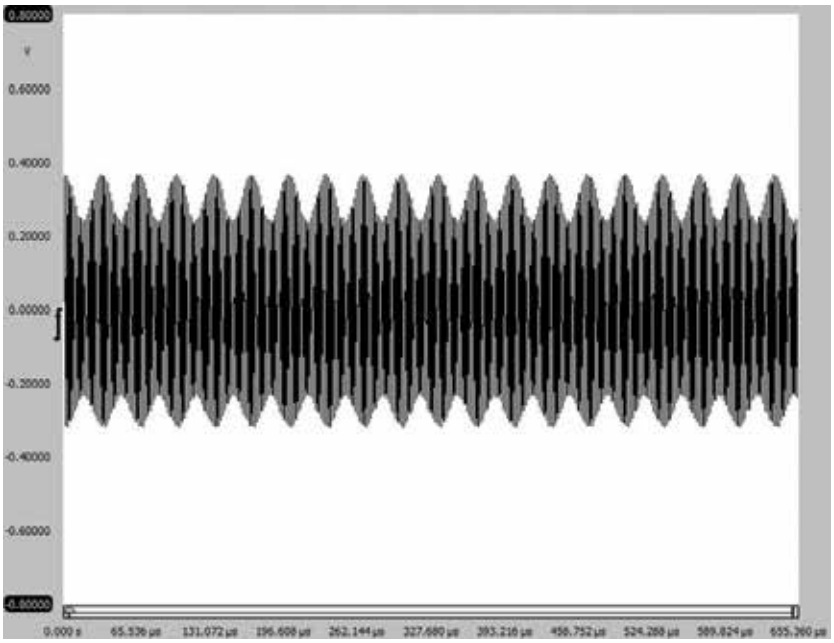

Figure 11. Observation of MI in the BF mode in the nonlinear bimodal transmission line for a signal of frequency f = 491.5 kHz, and amplitude V_M = 3.6 V observed at the 138th cell.

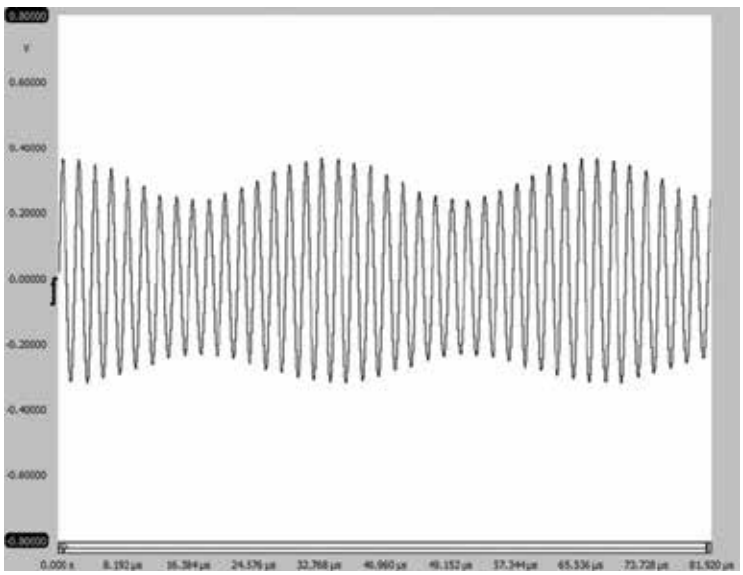

Figure 12. Details of signal in BF mode in the nonlinear bi-inductance transmission line for a signal of frequency f = 491.5 kHz and amplitude V_M = 3.6 V observed at the 138th cell. Note that wave plane of entry is modulated in amplitude (M = 0.18 modulation rate).

instability such as provided for in the calculations, and on the other hand, to introduce amplitude that is strong enough to initiate the disruption that will trigger the IM of the wave. To do this, we have chosen a sinusoidal signal whose frequency was f = 491.5 kHz for

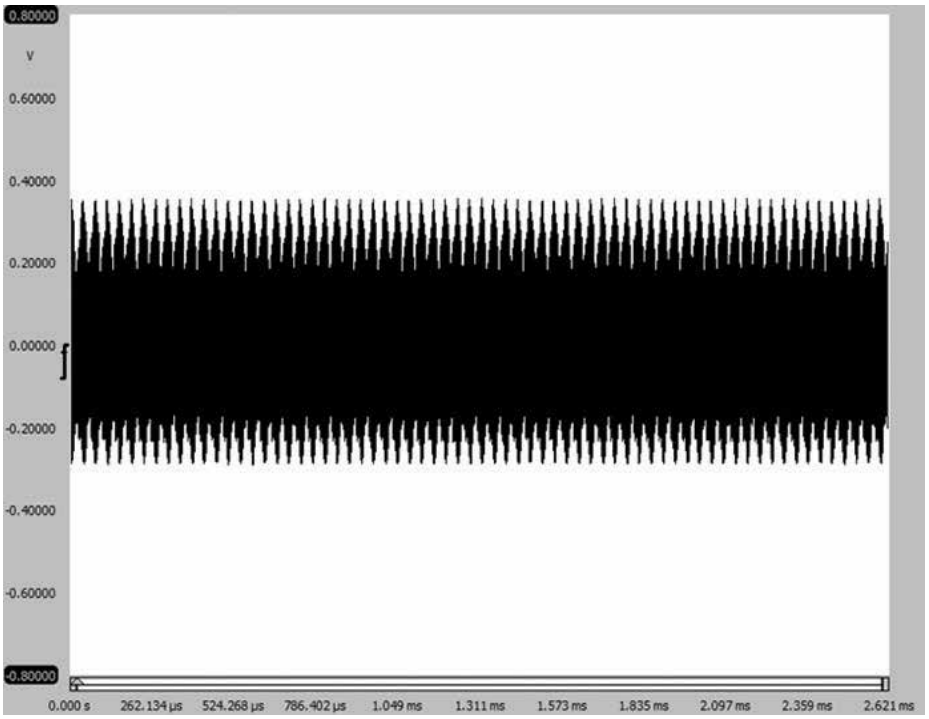

Figure 13. Observation of modulation instability in HF mode in the transmission of nonlinear bi-inductance line for a signal of frequency f = 897 KHz and amplitude V_M = 3.6 V observed at 130th cell.

amplitude V_M = 3.6 V. We observe in **Figure 11**, the signals are collected at the level of the 138th cell.

Zooming on the recording of the signal shows that plane wave, which is injected at the entrance to the line, shows the MI in amplitude whose rate is 0.18 (**Figure 12**).

Modulation instability was also observed in HF mode. In this case, we have chosen a signal whose frequency is in the region of modulation instability such as provided for by the calculations in HF mode and which has a magnitude large enough to initiate the disruption that will trigger the MI of the wave. To do this, we have chosen a sinusoidal signal whose frequency is f = 897 KHz and amplitude V_M = 3.6 V. We observe in **Figure 13**, the signals collected at the level of the 130th cell.

6. Fermi-Pasta-Ulam recurrence

6.1. Historical reviews

In 1952, Fermi et al. [17] led a digital experience on a nonlinear constituted 64 particle system point of identical mass related to their neighbors by springs weakly nonlinear. They expected that the introduced nonlinear coupling between neighboring oscillators would allow a transfer of energy between successive vibration modes, thus causing an equipartition of energy over a wide spectrum. Against all odds, the system introduced a quasi-periodic behavior of

the most complex. They found that all the energy which was initially excited almost returned to fundamental mode. This phenomenon was later called recurrence Fermi-Pasta-Ulam (FPU). This experience was important for two reasons—first, it highlighted the complexity of nonlinear systems; second, it demonstrated the power of the complex systems.

6.2. Experimental observation of the Fermi-Pasta-Ulam recurrence in a transmission electrical nonlinear bi-inductance line

The electrical nonlinear bimodal transmission line presents a level of complexity compared to its counterpart mono inductance as far as it has two modes of propagations, the HF and BF mode. We propose to conduct a study of the recurrence of FPU in each mode.

6.2.1. The FPU recurrence in the BF mode

In BF mode, we introduce a sine wave of frequency f = 475 KHz in the line with an amplitude Vsignal = 1.5 V, the polarization of the line voltage is V_0 = 1.5 V, and we collect the signal level of the inductance of each cell L_2 (L_2 inductors are located on cells of even order). We see that the collected signal presents deformations of stochastic appearance that initially will grow as it sinks into the line to finally find the sinusoidal shape of the signal of departure to the 22nd cell (**Figure 14**). This phenomenon observed in the electrical nonlinear bimodal transmission line is known as the Fermi-Pasta-Ulam (FPU) recurrence.

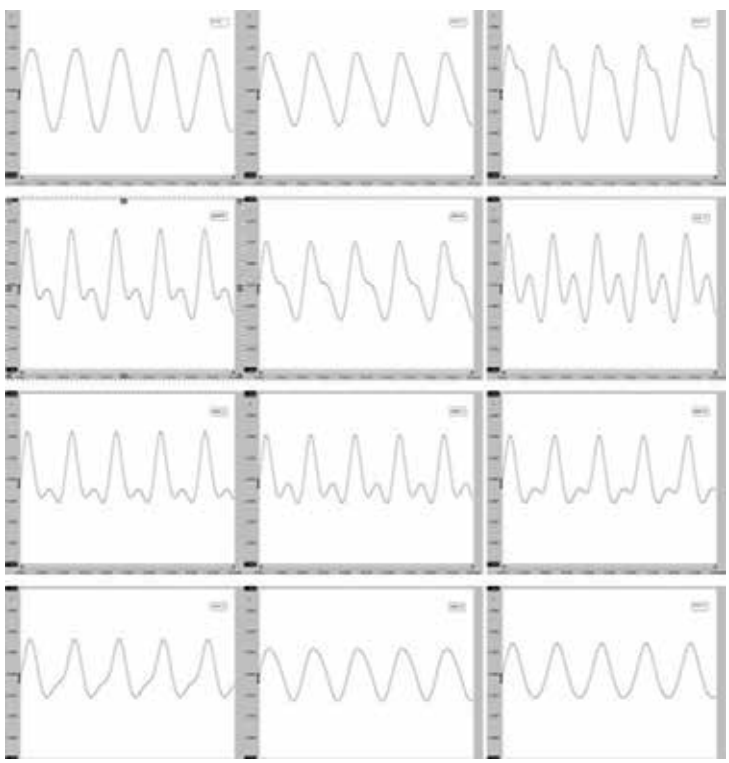

Figure 14. FPU Recurrence observed in electrical nonlinear transmission line in BF mode on inductance L2, for a signal of frequency f = 475 KHz and Vsignal = 1.5 V and V_0 = 1.5 V as voltage polarization of the line.

We continue to find the signal in the following cells (44th, 66th, 88th, and 110th), which enabled us to confirm the return period of the line to 22nd cells (**Figure 15**).

Again, we see that the amplitude of the signals decreases by increasing order from recurrence. This is due to the joule effect because let us not forget that our line is dissipative for the presence of inductor L_1, and $r_1 = 5\Omega$ his resistor and the inductor L_2 and its $r_2 = 8\Omega$.

6.2.1.1. Comparison of the recurrence at the level of cells of inductance L_1 and L_2

We also conducted the study of signals in cells of type L_1 (chokes on the cells of odd order). We find that the period of recurrence for the inductances of L_1 type is the same as that measured for inductors of type L_2. We present the first recurrence observed for L_2 and L_1 cells at the level of cell 22 and 23, respectively, in **Figure 16**. Later, we see that successive recurrences on the inductances of L_1 type intervene at the level of cells 45, 67, 89, 111, and so on. For inductor L_1, we found recurrence period also at 22nd cell.

Yet the study of the evolution of the waveforms between two recurrences often shows a sensitive form between the signals taken on L_2 and those taken on L_1. We see the signals observed at the level of cells 10 and 11 for the inductors L_1 and L_2, respectively, are quite dissimilar in shape in **Figure 17**.

In **Figure 18**, we observe the spectral decomposition of signals collected on inductance L_2 and L_2 at cells 10 and 11, respectively. We see that the two signals contain the fundamental term

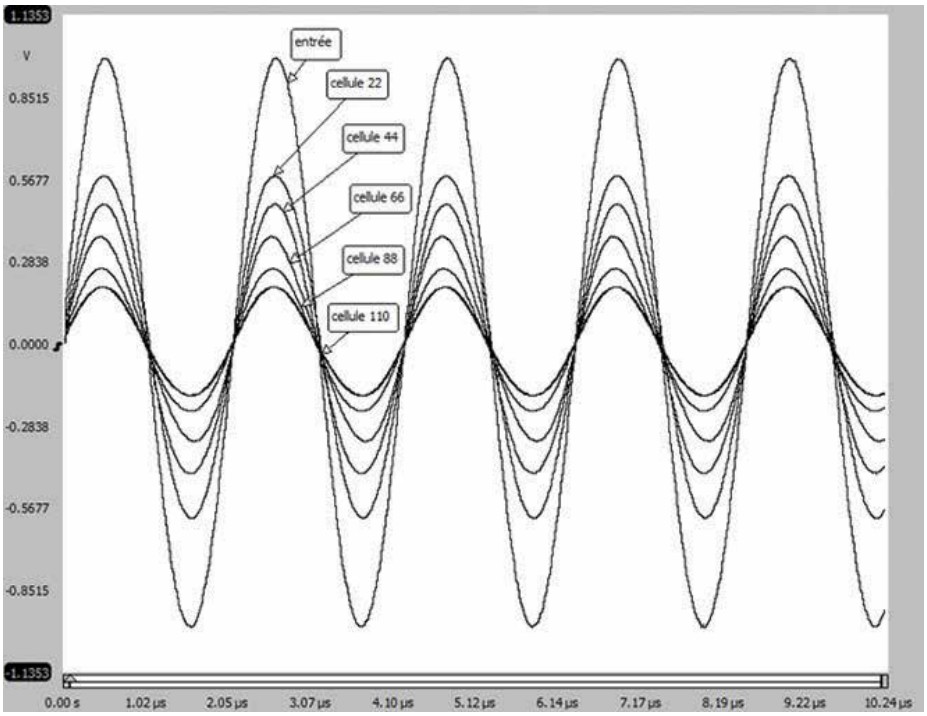

Figure 15. Observation of the first five recurrences for the electrical nonlinear bimodal transmission line in the BF for inductance *L* 2, with *f* = 475 kHz, Vsignal = 1.5 V, and polarization voltage of the line V_0 = 1.5 V.

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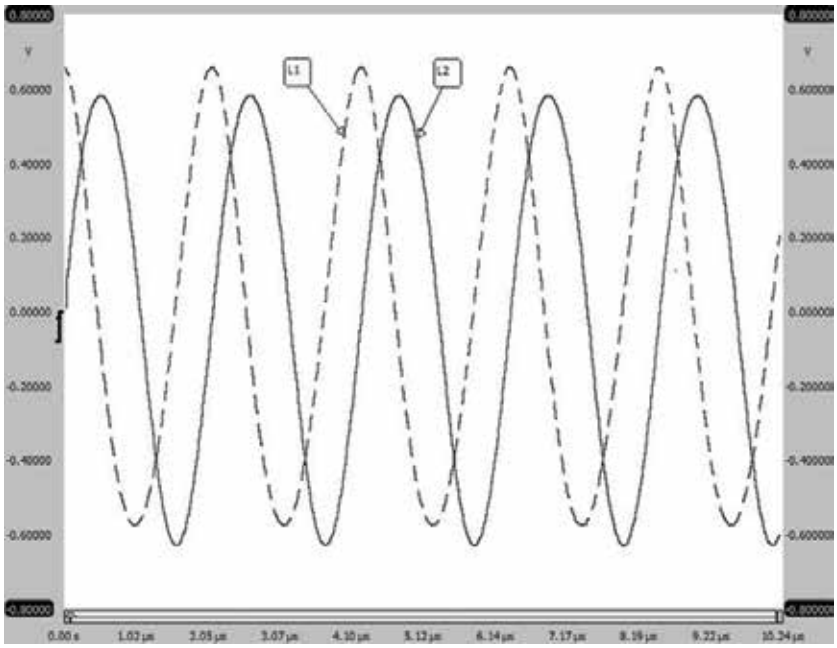

Figure 16. Observation of the first recurrence at the 22nd and 23rd cells on inductors L_1 and L_2, respectively, for a signal in the BF mode of frequency f = 475 kHz and Vsignal = 1.5 V, the voltage polarization of line is V0 = 1.5 V.

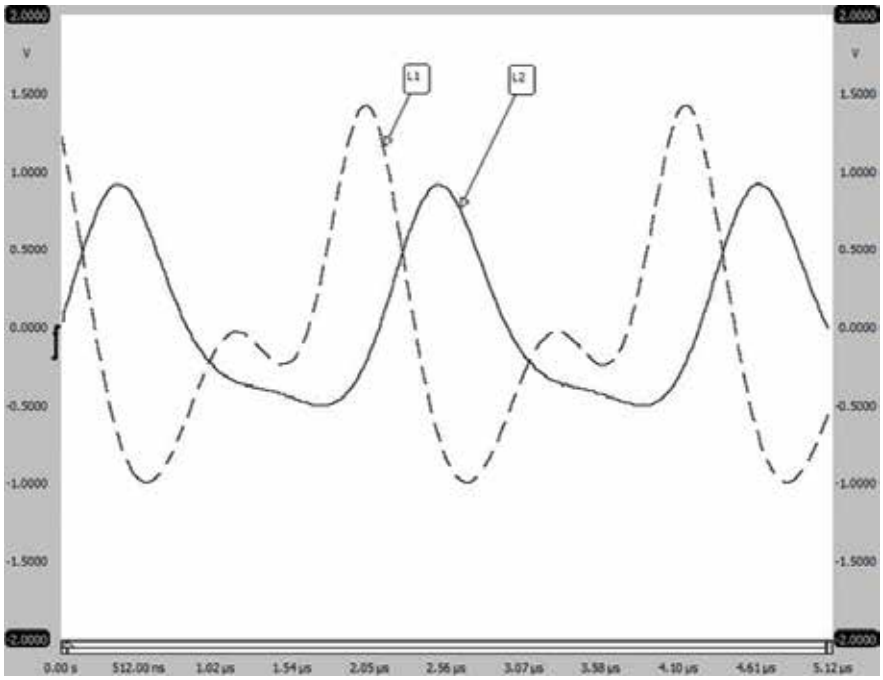

Figure 17. Observation of the signals measured on the inductance L_2 and L_1 at cells 10 and 11, respectively, for a signal in the BF mode amplitude Vsignal = 1.5 V, the voltage polarization of the line V_0 = 1.5 V, and frequency f = 475 kHz.

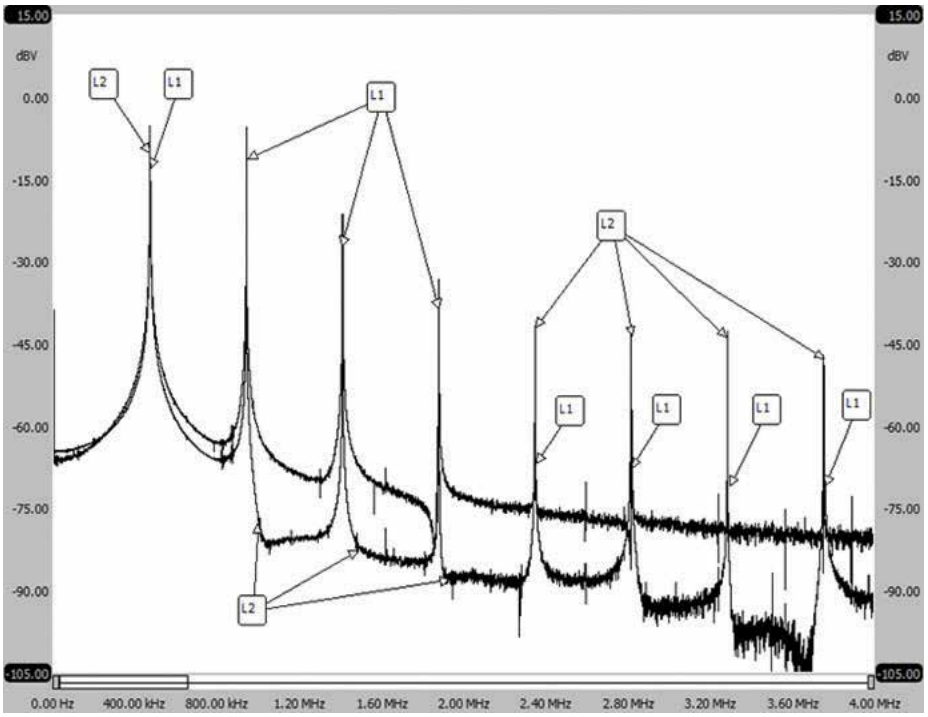

Figure 18. Observation of the Fourier transform of signals measured on the inductance L_2 and L_1 at cells 10 and 11, respectively, for a signal taken in mode BF having a frequency f = 475 kHz, and amplitude Vsignal = 1.5 V, with a voltage polarization V_0 = 1.5 V.

that corresponds to the frequency of the sine wave introduced (f = 475 KHz) and located at frequency harmonics 940 KHz, 1.41 MHz, 1.88 MHz, and so on. We see, for that concerning the cell 10, the signal on the inductor L_2, the contribution of the first three harmonics prevail over others in addition to the fundamental. However, with regard to the collected cell on the 11th cell, inductance L_1, the contribution of the following harmonics are predominant in addition to the fundamental. We can deduce that signals of inductors L_1 and L_2 are in fact identical in spectral terms and that is the relative contribution of the different harmonics, which explains the difference in shape between these signals.

On the other hand, the occurrence of recurrences marks the return to the ground state of the signals observed at the level of the inductance L_1 as L_2. In **Figure 19**, we see the fundamental term becomes predominant, the contribution of the various harmonics being then quite marginal.

6.2.2. The FPU recurrence in the HF mode

Observation of recurrent FPU in HF mode may prove to be more challenging than the BF mode. This is primarily because, in this mode, HF signal amplitude is much lower than in BF mode because of the preponderance of the dissipative effects on nonlinear effects. Let us add to it in high frequencies, the periods of recurrence are much smaller and we count the periods by units of cell. However, we observed the FPU recurrence in HF mode by substantially increasing the amplitude of the input signals. Unlike the BF mode, we have sometimes

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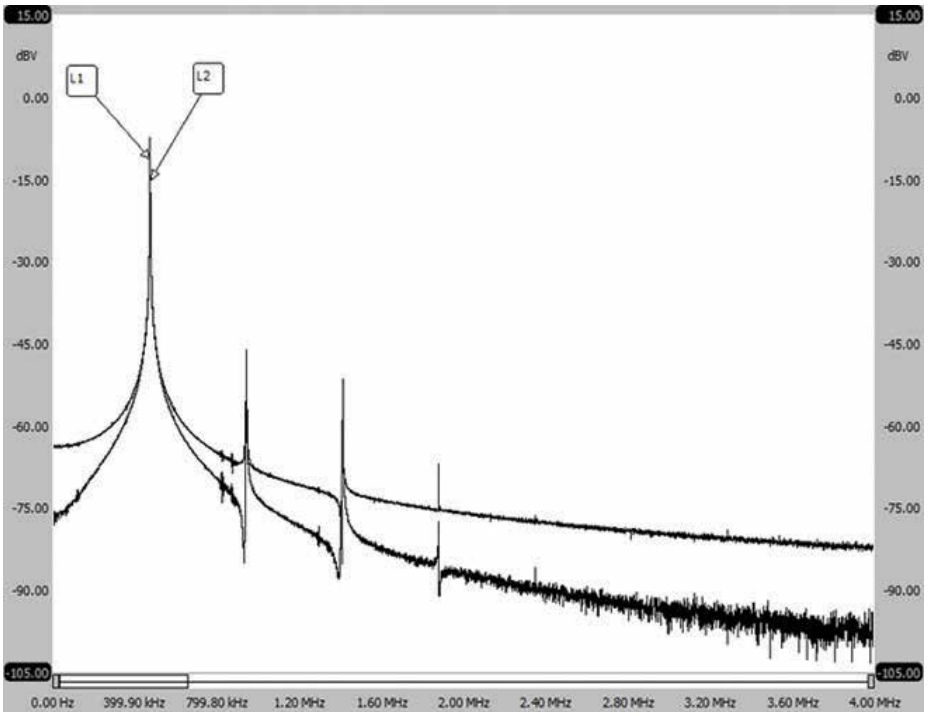

Figure 19. Observation of the Fourier transform of signals measured on inductors L_1 and L_2 in the first recurrence (cell 22 and 23, respectively) for a signal in the BF mode f = 475 kHz frequency and amplitude Vsignal = 1.5 V for a voltage polarization V_0 = 1.5 V. There is a return to the ground state (f = 475 kHz) contribution of the harmonics of orders 1, 2, and 3 is marginal.

resorted the spectral analysis of the transform of Fourier to ensure that the wave has covered its sinusoidal shape. In precedent works [18, 19], we present the evolution of the signal and Fourier transformation (signal frequency f = 910 kHz, Vsignal = 2.2 V and polarized voltage V_0 = 1.5 V). In these works, we see that the amplitude of the signal of the positive half-wave is higher than that of the wave for the negative alternation. This comes from the fact that the nonlinearity of the capacity C(V) does not similarly affect the two alternations. The minimum of the negative alternation seems more flattened than the positive alternation. On the other hand, Fourier analysis reveals the presence of a harmonic with twice the fundamental frequency. We find for the inductors L_1, located in the cells of odd order, recurrences occur to the cells 5th, 11th, 17th, 23rd, and so on. With regard to inductance L_2, located on the cells of even order, the recurrences occur in cells 4th, 10th, 16th, 22nd, and so on. The return period of the line for the HF mode considered is therefore an average of 6th cell.

6.3. Evolution of the period of recurrence based on the amplitude of the signal

We also studied the evolution of the return period depending on the amplitude of the signal in the BF mode and frequency f = 475 KHz. By varying the amplitude of the input signal offered in the line, we see a linear dependence of the period of recurrence with the inverse of the square root of the amplitude of the voltage of the signal [19] (**Figure 20**). Toda [20], in the case of the electric transmission line mono-modal,determined theoretically this dependence of the return period with the amplitude of the applied signal.

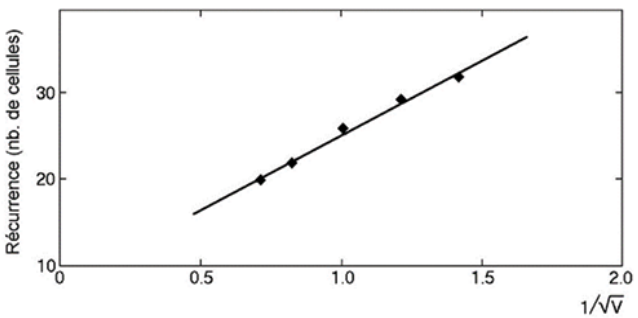

Figure 20. Variation of the return period expressed in number of cell based on the inverse of the square root of the amplitude of the signal applied to a frequency f = 475 KHz wave and voltage polarization V_0 = 1.5 V.

7. Observation of the solitons in the line

7.1. Soliton trains

It is established for a long time that when a wave is subjected to a modulation instability, it eventually splits up in a wave train depending solitons type [12–15]. To observe this behavior in our bi-inductance line, we introduced at the entrance of the line a wave whose frequency is located in the region of modulation instability of BF and the mode, which presents an amplitude sufficiently high to cause a strong disturbance that will trigger the phenomenon of MI. We take a signal of frequency as f = 491.5 kHz and amplitude V_M = 4 V. We put two probes at the cell 74 and the cell 86 to observe the evolution of the wave train. Knowing the frequency of the wave and the wave number through the dispersion curve, we determine the phase of the wave speed thanks to the equation (Eq. (1)), we obtain: f = 491.5 KHz, k = 1.21 rad./cel., by the dispersion curve, and $v_\varphi = 2.55 \times 10^6$ cel/s.

This indicates that the wave crosses a cell in 0.39×10^{-6} s and (86–74) cells or 12 cells closer than 5 ms. This value allows us to identify a particular point of the wave collected at the 74th cell and determine its new position on the waveform of the 86th cell. We present, in **Figure 21**, the waveform of signals collected at the cells 74 and 86. We see in the figure, the train of solitons, which run through the line. We identify a shoulder (cursor C1) which is the waveform corresponding to the signal collected at the 74th cell, which corresponds to two solitons which follow. The cursor positioned on the soliton of greater amplitude. The cursor positioned at 5 ms, (cursor C2) shows the new position of the two solitons. We find that the highest amplitude of soliton exceeded the lowest amplitude of soliton. This observation is in agreement with the results of simulations and observations made on the solitons confirms that the speed of propagation of a soliton is more important than its amplitude [2].

7.2. Propagation of a solitary wave in the line

The image of the optical solitons, which are the natural optoelectronics bits, can be designed as electric solitons that present a sech2 profile in the time domain. We have therefore built a signal whose profile is given by the relationship (Eq. (4)):

$$V(t) = A\,\mathrm{sech}^2(\alpha t) \tag{4}$$

where A and α are adjustable parameters and t time.

We inject into the bi-inductance line a signal in sech2 profile, and we follow the evolution of the signal in the line. We observe, in **Figure 22**, the evolution of signal at input cell 72 and input cell 144. We note that the shape of the signal remains intact during its spread in the line. However, we are seeing a weakening of the amplitude that is bound to the dissipative nature of the line. On the other hand, just like Remoissenet [2], we observe an oscillatory tail that accompanies the solitary wave in its spread.

7.3. Shape modification of the signal

As we previously announced in [18], the LTNL can be used to modify the forms of signals. One example is in the case of the generation of radar abrupt front signals to obtain systems that are more accurate. Even our experimental line is not designed and optimized to produce that effect. We have been able to observe some modification in waveforms by nonlinearity.

7.3.1. Signal compression

To illustrate the phenomenon of signal compression, we inject a sinusoidal wave amplitude V = 1.75 V for a voltage polarization of the line V_0 = 1.5 V and frequency f = 169.4 KHz, at the entrance of the line. We observe at the 101th cell, the signal compared to the starting signal as a factor of compression order 2 (**Figure 23**).

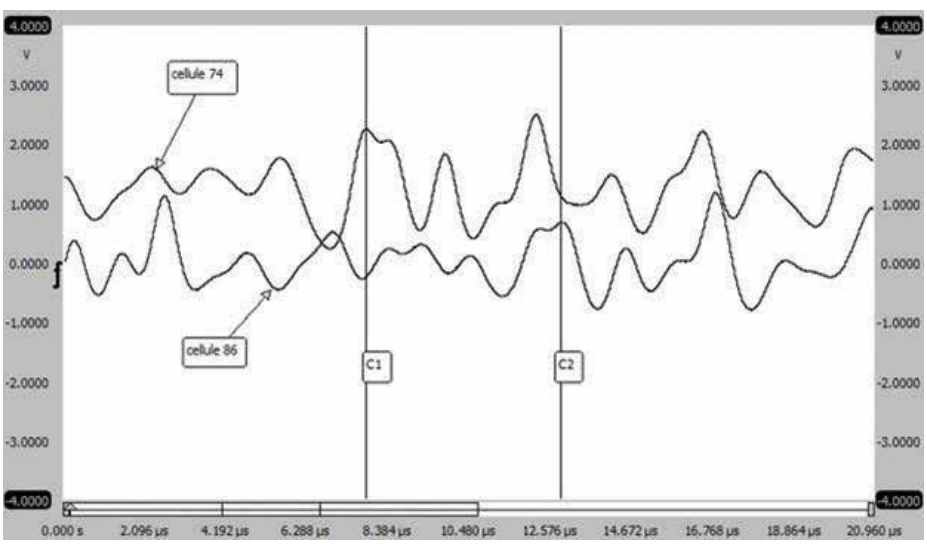

Figure 21. Observation of a train of soliton produced by the fragmentation of a plane wave subject to modulation instability for the BF of 491 kHz frequency and amplitude 4 V. The positions of the C1 and C2 sliders allow seeing the evolution of a pair of soliton in the line at cell 74 and cell 86.

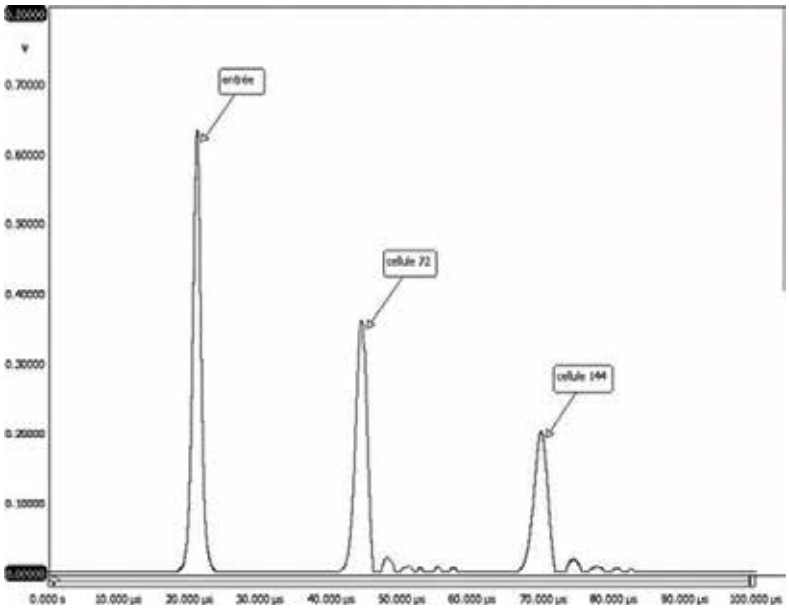

Figure 22. Evolution of a solitary wave sech2 profile in the bi-inductance line. Note the conservation of cohesion of the wave; the decrease amplitude is due to losses by Joule effect and the presence of the oscillatory tail.

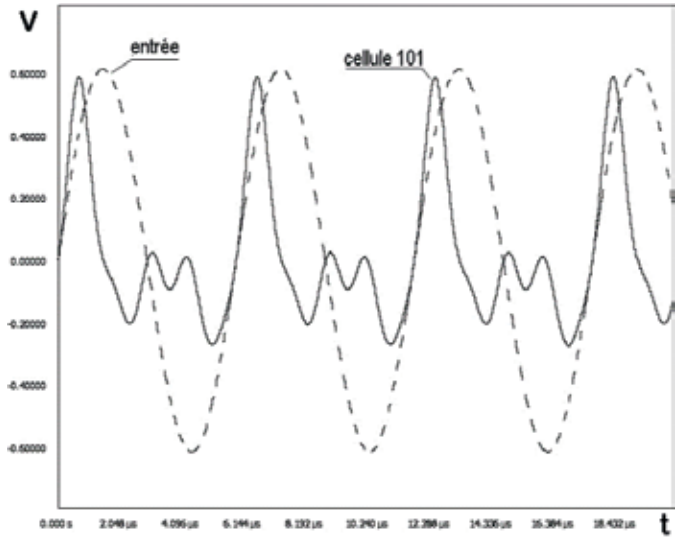

Figure 23. Compression of a signal effect observed in the cell 101 (full lines) for an input signal of sinusoidal form f = 169.4 KHz frequency and amplitude V = 1.75 V (dashed), polarization of the line voltage is V_0 = 1.5 V.

7.3.2. Frequency multiplier

Generally to raise the frequency in electronic systems, it is necessary to use oscillators which present increasingly raised (brought up) frequencies of vibration. Since a few years, the NLTL combined with an amplifier, which amplifies the signals stemming from the noise of the electronics.

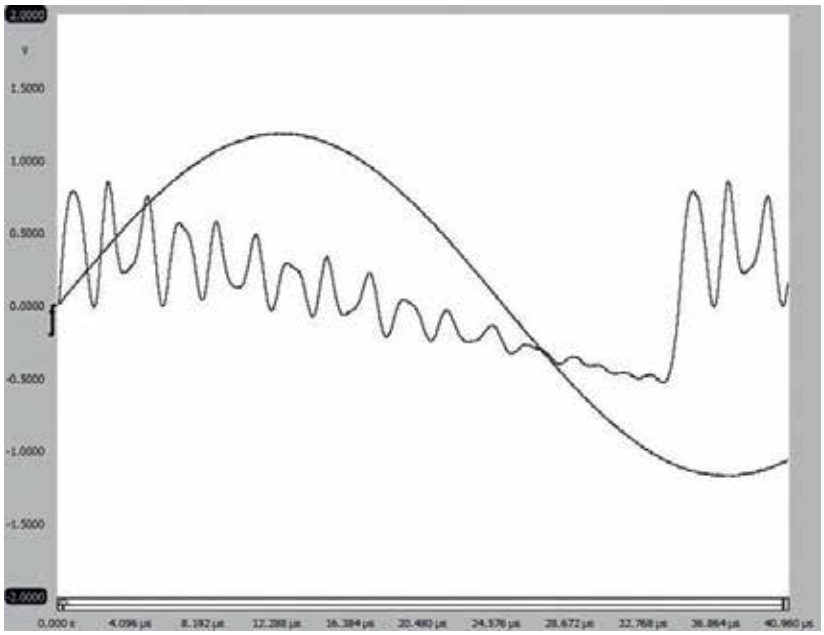

Figure 24. Decomposition of a half period of a sine wave of amplitude V = 1.5 V and f = 20 KHz frequency, in a solitary wave train observed the cell 175 for a voltage polarization V_0 = 1.5 V.

For what concerns us, we show the feasibility of the project by proposing another approach. We had shown in Section 2 that the nonlinearity could produce a shock wave on a sinusoidal signal injected in the NLTL (**Figure 7** in Section 4). If we bring this phenomenon, we show that it is possible to decompose a given plane wave of frequency f = 20 KHz at wave train alone. We show (**Figure 24**) that the half-life of the initial sine wave consists of the solitary wave train, which was observed at the 175th cell. Everything happens if the system increases the frequency of the original wave by a new wave train, which has the frequency greater than the starting frequency.

8. Conclusion

We present in this work a selection of experimental results which we reached and which concerns essentially the system of study of our choice, worth knowing, the electrical nonlinear transmission line.

We notice that our experimental device was proved to be a powerful tool of work characterized by its flexibility and its robustness. Qualities essentially owed to our strategic choice who allowed us to make our investigations on sections of lines in the modest size by comparison to other systems constituted by hundreds or even thousands of cells. This arrangement also allowed us to reduce considerably the sources of drift or of artifacts, which increase with the number of components of the line.

From the point of view of the experimental results, we determined, at first, experimentally the dispersion curve of the line by an original method, which consists of determining the phase

velocity of the wave between two consecutive cells. We determine the dispersion curve with a very good precision.

We proof the reality of the transmission of the waves in electrical lines not shelf spaces. We observed the effects of the waste and the dispersion of the waves. On the other hand, even our device was not designed and optimized to produce certain effects on the signals; we observed the modification of the shape of the signals like the compression of signal and the multiplication (increase) of frequency.

Finally, it is recognized today unanimously that the nonlinear physics was born with the remarkable work of Fermi, Pasta, and Ulam, who concerned an abstract system and the study which was made by numeral calculation, the collection what it was advisable today to call the FPU recurrence is a constant current events whatever is the system. We observed the FPU recurrence in the NLTL in BF mode and in HF mode. Hence, we brought a completely original explanation that gets off the beaten track.

The device carried out during this work makes possible to carry out in future work on the investigations on the nonlinear transmission lines and on the dynamics of the solitary waves in various applications as: characterization of the periodical loaded transmission lines, use of the nonlinear reactance of thin layers superconductive, resolution of the Ginzburd-Landau equations for a tangential magnetic field, supraconductivity in the forbidden band in a bimodal nonlinear system; and so on.

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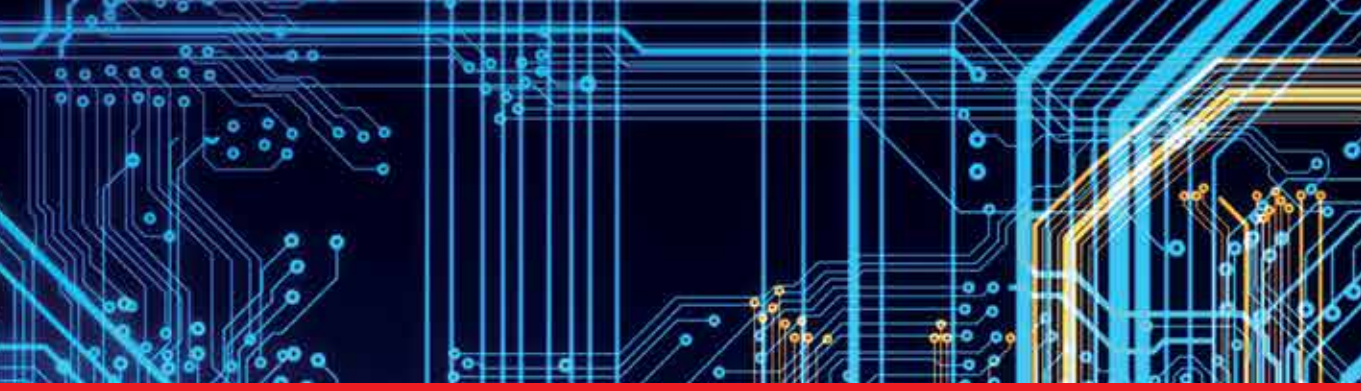

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