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Advanced Silicon Carbide Devices and Processing

Edited by Stephen E. Saddow and Francesco La Via

ADVANCED SILICON CARBIDE DEVICES AND PROCESSING

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Contributors

Mariana Amorim Fraga, matteo bosi, Marco Negri, Duan Baoxing, Olivier Deblecker, Zacharie De Grève, Christophe Versèle, Jean-Francois Michaud, Daniel Alquier, Marc Portail, Stefania Castelletto, Lorenzo Rosa, Brett Johnson, Gong-Ru Lin, Chung-Lun Wu, Chih-Hsien Cheng, Yung-Hsiang Lin, Sadafumi Yoshida, Ming-Hung Weng, Lucy Martin, Hua-Khee Chan, Konstantin Vassilevski, Nick Wright, Alton Horsfall, Feng Zhang, Zhengyun Wu, Guosheng Sun, Yiping Zeng

Notice

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Meet the editors

Stephen E. Saddow is a Professor of Electrical Engineering and member of the Biomedical Engineering Faculty, College of Engineering, at the University of South Florida, Tampa, FL USA. He has been an active researcher in the field of SiC Technology since 1992, when he pioneered the use of 6H-SiC for high-power optical switching. Since this early work, he has specialized in the development of various SiC processing methods, most notably CVD of 3C-SiC on Si. In the last decade he has focused on the use of 3C-SiC for biomedical applications and has been developing SiC-based continuous glucose monitoring systems and neural implants. He has over 150 published papers, 3 books, several book chapters and has several patents, awarded or pending, on the use of SiC for biomedical applications. He has held several visiting researcher/professor positions in Italy, Germany, France, and more recently Brazil.

Francesco La Via was born in Catania, Italy, in September 1961. He received the M.S. degree in physics from Catania University, Italy, in 1985. From 1985 to 1990 he had a fellowship at STMicroelectronics, Catania and was a Visiting Scientist at Philips National Laboratory, Eindhoven, Netherlands. In 1990 he joined the CNR Institute for Microelectronic, Catania as a researcher. In 2001 he became senior researcher and from 2003 he has been responsible of the division of CNR-IMM that develops new processes for silicon carbide epitaxy and hetero-epitaxy. From 2013 he has been in the International Steering Committee of the ICSCRM conference. In 2015 he became co-Chair of the ICSCRM 2015 and Chair of the Technical Program Committee. In this period he published more than 300 papers on JCR journals, one e-book, a focus issue of JMR and three book chapters. He has presented nine invited contributions to international conferences. He has 10 patents on SiC processing.

Contents

Preface

The field of Silicon Carbide has seen steady growth since pioneering work by Nishino and Powell in 1983 when they demonstrated the large-area growth of silicon carbide (SiC) on silicon (Si) substrates. This was the first time that a cost-effect method for producing high-quality SiC material was demonstrated with the possibility of scaling up the technology for industrial applications. While the growth of hexagonal crystals of SiC had been demonstrated by Lely and others as early as the 1950s, it was the possibility of producing scalable substrates of SiC, in this case the cubic polytype known as 3C-SiC, that led to a renaissance in SiC technology. One could argue that this event stimulated renewed efforts to develop high-quality hexagonal substrates of SiC which would allow for the homo-epitaxy of device layers leading to such technologically important devices as blue LEDs. The group of Bob Davis at NC State was able to develop cost-effect methods to grow high-quality bulk crystals of 6H-SiC which led to the founding of Cree Research (now Cree Inc.) and the first commercially available blue LED in the late 1980s. As they say 'the rest is history' and the story of how Cree and other companies globally led us to the current state of SiC technology is well known, resulting in a billion-dollar industry world-wide in the area of solid-state lighting and power electronics. With this in mind, we organized this book to bring to the attention of those well versed in SiC technology some new developments in the field with a particular emphasis on particularly promising technologies such as SiC-based solar cells and optoelectronics. We have attempted to balance this with the more traditional subjects such as power electronics (DC to DC converters, for example), and some new developments in the improvement of the MOS system for SiC MOSFETS. Staying true to the original stimulation of the last quarter century of SiC activity, we also included a review on 3C-SiC for both microsystem and electronic applications. We sincerely hope that this somewhat eclectic mix of topics will be both highly interesting to the reader while helping those who wish to develop SiC materials for use in areas other than main-stream power electronics. It was our distinct pleasure and honor to edit this impressive collection of works from around the world and we wish you an enjoyable experience as you read the book, as we believe it will result in further developments in the field of SiC which continues to grow exponentially world-wide.

Stephen E. Saddow, PhD
Professor of Electrical Engineering,
University of South Florida,
Tampa, FL USA

Francesco La Via, PhD
Italian National Research Council,
Catania, Sicily, Italy

Section 1

SiC Device Processing

Chapter 1

Silicon Carbide in Microsystem Technology — Thin Film Versus Bulk Material

Mariana Amorim Fraga, Matteo Bosi and Marco Negri

Additional information is available at the end of the chapter

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Abstract

This chapter looks at the role of silicon carbide (SiC) in microsystem technology. It starts with an introduction into the wide bandgap (WBG) materials and the properties that make them potential candidates to enable the development of harsh environment microsystems. The future commercial success of WBG microsystems depends mainly on the availability of high-quality materials, well-established microfabrication processes, and economic viability. In such aspects SiC platform, in relation to other WBG materials, provides a clear and competitive advantage. The reasons for this will be detailed. Furthermore, the current status of the SiC thin film and bulk material technologies will also be discussed. Both SiC material forms have played important roles in different microsystem types.

Keywords: silicon carbide, thin film, bulk material, microsystem technology, harsh environment

1. Introduction

As the most popular microelectronic material, silicon (Si) has established itself as the main material for microsystem technology (MST) or micro-electro-mechanical systems (MEMS). This occurred for a number of reasons, including the mechanical properties of silicon (in single crystal form, it is almost a perfect Hookean material and hence no energy dissipation occurs) and economic issues (ready availability of low-cost high-quality materials) [1].

Advances in microsystem technology have frequently been linked to innovations in the development of advanced materials that can outperform conventional semiconductors: not only Si, but also germanium (Ge) and gallium arsenide (GaAs) [2, 3].

In order to enable wide applications in harsh environments, the goal is to develop microsystems able to go beyond the limits of those of conventional semiconductors. In the search for advanced materials to be used in MEMS devices, the wide bandgap (WBG) semiconductors are recognized as the most promising. These semiconductors possess remarkable electronic properties that Si and other conventional materials lack. WBG semiconductors have a high bandgap, more than 2.0 eV, whereas the conventional semiconductors have a small bandgap (around 1.0 eV). One impact of this is that the WBG semiconductor devices can be employed at elevated temperatures [4].

Besides the excellent electronic properties, WBG semiconductors exhibit superior physical properties, as well as chemical inertness, overcoming the limitations of traditional silicon-based platforms in harsh conditions. Thus, WBG MEMS sensing element can be directly exposed to harsh environment media, which may reduce the cost of packaging [5].

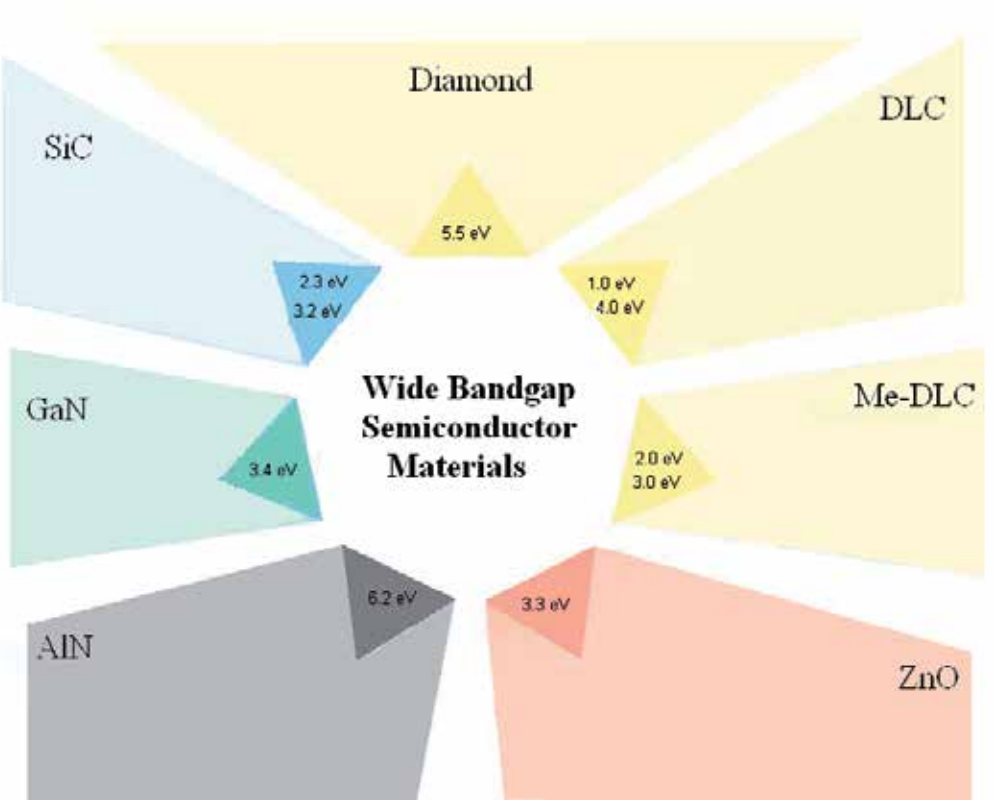

Figure 1. Wide bandgap semiconductor materials with potential for use in microsystem technology

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Other important properties of WBG semiconductors are high Young's modulus, hardness, and fracture toughness. Such characteristics are also potentially interesting for microsystem applications given that the Si has relatively low values [6].

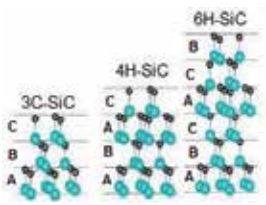
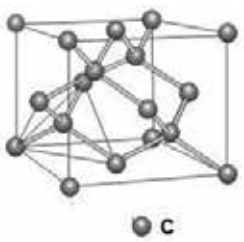
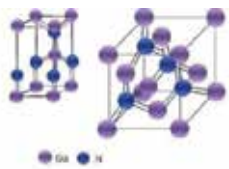
Properties	SiC	Diamond	GaN
Structural	Main crystal symmetries: cubic (zinc blende) and hexagonal (wurtzite) 	Crystal structure: cubic 	Crystal structure: hexagonal (wurtzite) and cubic (zinc blende) 
Physical	• Melting point (~ 2800ºC) • Thermal expansion coefficient at room temperature (4 x 10^{-6} K^{-1}) • Thermal conductivity at room temperature (~500 W m^{-1} K^{-1}) • Dielectric constant (9.7)	• Melting point (~4000ºC) • Thermal expansion coefficient at room temperature (1 x 10^{-6} K^{-1}) • Thermal conductivity at room temperature (2000 W m^{-1} K^{-1}) • Dielectric constant (5.7)	• Melting point (~2770ºC) • Thermal conductivity at room temperature (~170 W m^{-1} K^{-1}) • Dielectric constant (9.0)
Electronic	• Bandgap (2.3–3.2eV) • Electrical resistivity (150 Ω.cm for 3C-SiC, 10^4–10^8 Ω.cm for 6H-SiC and >10^{12} Ω.cm for 4H-SiC) • Saturated electron velocity • (2 x 10^7 cm/s) • Electric breakdown field (1.2–3MV/cm)	• Bandgap (5.45 eV, indirect gap) • Electrical resistivity (10^{13}–10^{16} Ω.cm) • Saturated electron velocity (2.7 x 10^7 cm/s) • Electric breakdown field • (10 MV/cm)	• Bandgap (3.4 eV, direct gap) • Electrical resistivity (>10^5 Ω.cm) • Saturated electron velocity (1.5 x10^7 cm/s) • Electric breakdown field • (3.5 MV/cm)
Mechanical	• Hardness (~ 30 GPa) • Young's modulus (~ 450 GPa)	• Hardness (~90GPa) and wear resistance • Young's modulus (~1050 GPa) • Strength/tensile (> 1.2 GPa) • Low compressibility • (8.3 x 10^{-3} m^2 N^{-1})	• Hardness (~10GPa) • Young's modulus (~ 220 GPa)
Optical	• Refractive index (~2.65) • Suited for structural components and mirrors for space-based or ground optical systems	• Refractive index (~2.41) • Optical transparency (UV to far IR) • Highly resistant to damage from irradiation	• Refractive index (~2.3) • Transparency at visible wavelengths coupled with advanced optoelectronic of the nitrides
Chemical	• High resistance to corrosion • Chemical inertness • Biocompatible	• High resistance to corrosion • Chemically and biologically inert	• Radiation-hardened and biocompatible material

Table 1. Properties of SiC, diamond, and GaN

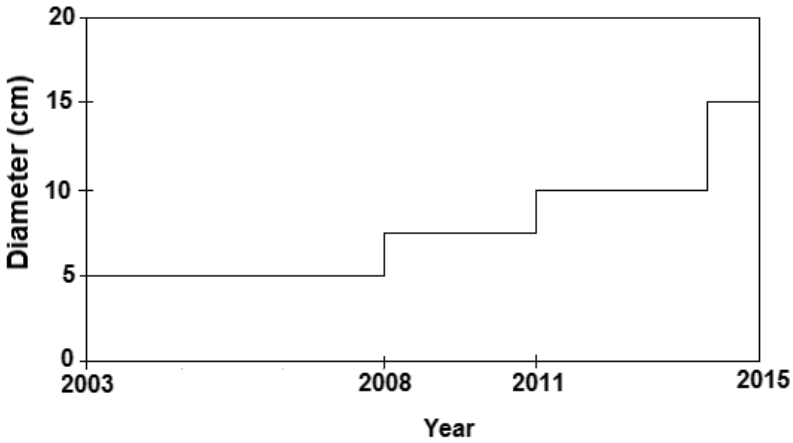


Figure 2. Recent evolution of the diameter of commercially available SiC wafer

WBG semiconductors can be grouped into three main categories: (i) carbon-based materials, (ii) nitride-based materials, and (iii) oxide-based materials. Among them, Figure 1 highlights some examples of WBG semiconductors that are being successful employed in MEMS sensors: diamond [6], diamond like-carbon (DLC) [7], metal-containing DLC (Me-DLC) [8], silicon carbide (SiC) [3], gallium nitride (GaN) [2], aluminum nitride (AlN) [9], and zinc oxide (ZnO) [10].

There is a consensus that the WBG semiconductors are the materials for harsh environment microdevices. However, there are differences and particularities among the different WBG semiconductor types. This leads us to ask which would be the best WBG semiconductors for use in microsystems. SiC, GaN, and diamond are considered with greatest potential due to their outstanding properties (see Table 1) and commercial availability of wafers [11-13]. From a material properties perspective, diamond has superior properties to SiC and GaN, except for its easy oxidation at high temperatures [5].

The technological development of SiC, diamond, and GaN material-based platforms are maturing in three directions: (i) production of wafers, (ii) techniques for micromachining, and (iii) materials integration. These platforms compete with each other. Currently, among them, SiC platform is the most established for harsh environment device applications.

Much progress in terms of quality and dimensions has been made in SiC wafer production. The 4" SiC wafers are the mainstream product on the market and recently 6" wafers were introduced, although the supply is still limited. Figure 2 shows the evolution SiC wafer size in the last years [14]. This diameter increase is crucial for reducing the cost of microdevices through scale economies and the use of Si device fabrication equipment.

In Figure 3, the price per area of SiC substrate wafer is compared with those of Si, diamond, and GaN. SiC substrate is cheaper than other WBG semiconductors [15]. However, the quality is not as good as Si wafers and the cost is significantly higher.

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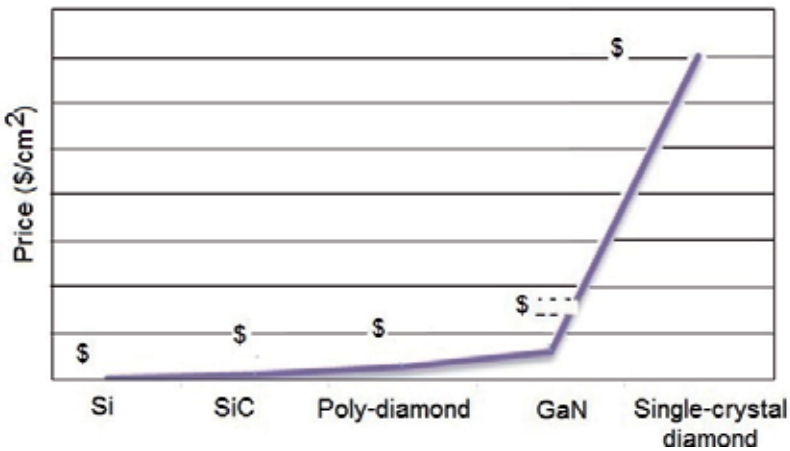

Figure 3. Comparison among the price of wafers of silicon, sapphire, silicon carbide, and gallium nitride (adapted from [15])

Another point related to SiC platform for developing MEMS devices is to establish a fabrication technology comparable to its silicon technology counterpart. One obstacle is the strong chemical stability of high quality SiC bulk, which makes its etching difficult for the fabrication of SiC MEMS structures. To overcome this drawback, the integration of SiC film with Si or SOI (silicon-on-insulator) substrates is a good alternative because it allows the fabrication of SiC-based MEMS through common Si micromachining processes.

Discussion and questions about applications of SiC thin film versus bulk material are opened. There are differences among material properties of each form. However, recent literature has shown that SiC in both forms, thin film and bulk material, play important roles in microsystem technology but each settle into its own role. There are interesting sensing devices that can be produced using both material forms.

SiC thin film has been used in different microsystem devices in different functions such as sensing layer (transduction element), buffer layer, and biocompatible coating. SiC bulk material allows the fabrication of all-SiC microsystem device (structural and sensing elements), which increase its performance especially in harsh environments. According to D. G. Jones's PhD thesis: "One vision of the future is an all-SiC sensor chip composed of crystalline SiC substrate, doped polycrystalline SiC structures, and sputtered amorphous SiC sealing layers" [16].

There is optimism about the feasibility of SiC thin film technology in microsystem applications, but the film growth on large area substrate without loss of uniformity or quality is still a challenge.

The purpose of this chapter is to give an outline of the current landscape of SiC key technologies for microsystem applications. The following SiC technologies are described addressing the bulk material and thin film: synthesis, material properties (quality), material processing, and microsystem device development.

2. SiC material issues for microsystem technology applications

Although there are over 200 known polytypes of SiC, only a few are grown with good reproducibility and attractive properties for microelectronics applications [17]. The polytypes of SiC commonly used in such applications are 3C-SiC, 4H-SiC, and 6H-SiC, which can be synthesized in thin film or wafer forms using different methods. The growth of SiC involves challenges related to the control of (i) polytype formation, (ii) defects, and (iii) doping.

The availability of high-quality SiC material with lower defect density and controlled doping is very important to ensure high fabrication yields and good device performance. For the last couple of decades, the quality of SiC wafer has been significantly improved. Likewise, the growth of high-quality SiC film on Si large wafers is becoming more mature. Unfortunately, thin-film growth methods still seek to obtain 3C-SiC films with properties comparable to those of hexagonal SiC bulk material.

Aside from material growth issues, micromachining of SiC has been the subject of intensive research in recent years for its application in MEMS devices. Several bulk and surface micromachining techniques have been studied for the fabrication of three-dimensional SiC MEMS structures. Nevertheless, despite the advances in deep dry etching methods for SiC bulk micromachining, the process is still complex. On the other hand, SiC-on-Si substrates are attractive for implementing MEMS devices because they combine the well-established Si wet bulk micromachining process with the outstanding sensing properties of SiC thin film.

In the next sections, the issues of growth and micromachining of SiC bulk and thin film will be reviewed.

2.1. Bulk (or substrate)

2.1.1. Bulk crystal growth and material quality

The crystal ingot of conventional semiconductors as Si, Ge, and GaAs are grown by melt methods, which are not suitable for SiC crystal growth because its stoichiometric melting only occurs at pressures above 10 GPa and temperatures higher than 3200 °C [18]. In addition, SiC bulk crystal growth involves challenges attributed to the physical-chemical nature of SiC such as polytypism and extreme thermodynamic properties (noncongruent melting at high temperatures) making difficult the production of semiconductor grade SiC ingots. Figure 4 compares the production of SiC wafers per ingot with ones of Si, sapphire (Al_2O_3), and GaN [19].

Thus as SiC and GaN, sapphire has high melting point and chemical inertness. However, few micromachining processes exist making fabrication of MEMS type structures difficult [20]. So, although sapphire is a promising high temperature material with lower cost, it does not compete with SiC in microsystem applications.

As illustrated in Figure 5, SiC substrates can be grown by methods based on vapor phase or solution phase. The vapor phase growth processes are the most common and are divided in

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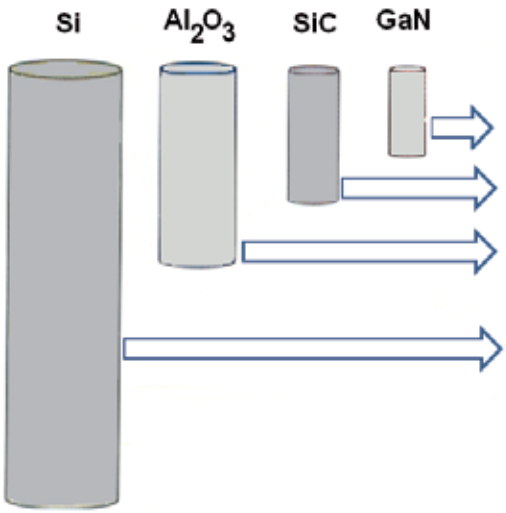

Wafers per ingot	Wafer price
< 10	x 100
< 50	x 30
< 100	x 10
>100	x 1

Figure 4. Comparison among production and price of SiC wafers with ones of Si, Al_2O_3, and GaN

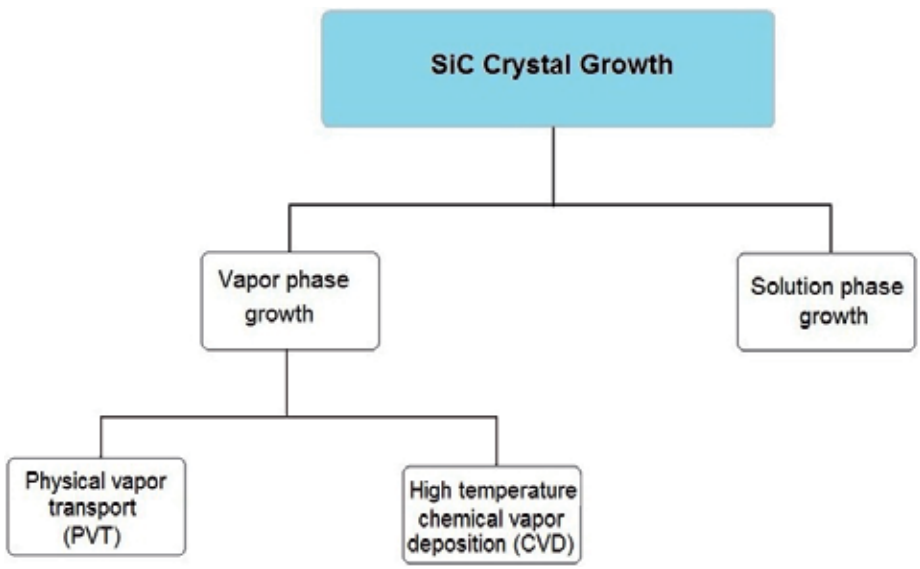

Figure 5. Main methods used for SiC substrate growth

two main types: (i) physical vapor transport (PVT) also called as seeded sublimation method or modified Lely and (ii) high temperature chemical vapor deposition (CVD). With the evolution of these processes, new techniques have emerged, namely, modified PVT method, continuous feed PVT (CF-PVT), and halide CVD [21].

Table 2 summarizes the main vapor phase processes for SiC crystal growth. The first process for growth of high-purity SiC crystal was reported by Lely in 1955. This process allowed the

Method	Description	Drawback	Year
Acheson	The process is based on reduction of silica (SiO_2) and carbon at temperatures above 2000ºC.	In general, the SiC grown by this method is contaminated and not suitable for electronic devices.	1892
Lely	Sublimation of SiC at elevated temperatures (2550–2600ºC) and normal pressure. It was the first method developed for high purity SiC crystal growth.	The control of polytype, size, and doping of the crystal is very limited. SiC crystals only up to 10 mm in diameter.	1955
Modified Lely (seeded sublimation or PVT process)	Polycrystalline SiC at the source sublimes at a high temperature (1800–2600ºC) and low pressure. It is the most mature growth process and allows the production large dimension SiC wafer with good quality.	The control of polytype and doping concentrations is difficult.	1978
HTCVD	SiC growth is carried out using conventional silicon and carbon gas precursors. It is possible to grow long ingots.	Technological challenges harder than for PVT control of the thermodynamic conditions.	1996

Table 2. Description and drawbacks of vapor phase methods for SiC crystal growth

synthesis of SiC with suitable quality for use in electronic devices, which was not possible using the previous method demonstrated by Acheson in 1892. One limitation of the Lely method is the growth of small SiC substrates only up to 10 mm in diameter.

In 1978, Tairov and Tsvetkov modified the Lely method allowing the production of large dimension SiC wafer with good quality. The modified Lely process became the main industrial method for fabrication of SiC wafer substrates of polytypes 4H-SiC and 6H-SiC with different thicknesses and doping (n-type, p-type, and semi-insulating). Regarding the 3C-SiC polytype, the CVD methods have been most used to grow it heteroepitaxially on different substrates, especially silicon. Large monocrystal 3C-SiC substrates with at least 200 micrometers thickness after removing the Si base layer are being produced [22].

Although the thermodynamic properties of SiC do not allow the solution phase bulk growth of SiC from a stoichiometric melt, it is possible to grow SiC from non-stoichiometric solutions containing Si and C. These solution growth processes have been developed based on the solubility of SiC and C in Si melt [21]. A problem is the very low carbon solubility in liquid silicon below 1800°C. It has been shown that the use of Si-metal growth flux is a good alternative to increase the carbon solubility [23]. Despite significant recent progress in solution phase growth, this method is still not well-established to the production of substrates like the PVT and CVD methods.

As pointed out in the previous sections, the wide use of SiC in semiconductor and MEMS devices is limited by high price of high-quality wafers. Controlling different types of defects has been a critical challenge for SiC wafer technology [24].

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In general, defects may compromise the structural integrity of the crystal, or alter its electrical, chemical, and thermal properties. A number of defects in SiC crystals have been reported, including different types of dislocations (mainly open-core screw dislocations called micropipes), low-angle boundaries, macro-inclusions, chemical impurities, and inhomogeneity in either dopant or polytype [25]. Among them, the micropipes are the most common obstacle to the production of high quality SiC devices. The origins of the formation of micropipes during crystal growth are not entirely known, but it seems to involve the propagations of dislocations in the nucleation phase or contaminant particles present upon crystallization [25].

With the continuous improving of wafer manufacturing processes, a significant reduction of micropipe densities has been achieved. Nowadays, there are commercial 2″ and 3″ SiC wafers with micropipe density less than 1/cm^2 and 4″ diameter with less than 10/cm^2 [14]. However, it has been observed that the quality of new larger wafers is relatively lower compared to prior generations [24]. The challenge of SiC wafer technology is increasing the wafer diameter keeping low levels of defects.

2.1.2. Bulk micromachining

Fabrication of MEMS using SiC substrate is still immature when compared to those on silicon substrates or with the SiC power devices. The high thermal and chemical stability of SiC make certain fabrication steps difficult. Etching has required particular attention because etch depths of at least 200 μm are required for bulk micromachined SiC structures [26].

Wet etching in potassium hydroxide (KOH) solution at temperatures between 70ºC and 90ºC is the most used method to fabricate Si MEMS structures due to its advantages like low cost and simple experimental procedure [27]. However, this process is not practical for SiC.

There are no simple wet-chemical etchants for SiC available suitable for device fabrication. Chemical etching is only possible under rather extreme conditions, for example, in molten KOH, NaOH, or Na_2O_2 at 450–600ºC. This process usually creates defects on the surface besides severe contamination from K or Na [28, 29].

The plasma-based dry etching has been shown as a practical way to deep etch SiC for the fabrication of MEMS. Fluorine-based plasmas have the most effective etch rate. An advantage is that the fluorinated etch products (SiF, and CF, species) are relatively volatile, and their removal from the surface is generally not the rate-limiting step [30]. Most commonly plasma sources employed in SiC etching are reactive ion etching (RIE), electron cyclotron resonance (ECR), and inductively coupled plasma (ICP). Much effort has been devoted to understanding the etch mechanisms in these processes in order optimize etching conditions such as pressure, gas flow rate, power, time, etc.

The SiC RIE process has been investigated in fluorinated gases (mainly CF_4, SF_6, and NF_3), usually mixed with oxygen using standard silicon RIE hardware [31]. Generally, SiC RIE process is highly anisotropic with little undercutting of the etch mask, leaving smooth surfaces. Typical RIE etch rate for 4H- and 6H-SiC are in the order of hundreds of angstroms per minute. In this range, the etch rates are sufficient for the fabrication of many electronic devices, but not

for MEMS sensors and some very high voltage power device structures. In such applications, SiC etch rates on the order of tens to hundreds of micrometers deep are required [31].

High density plasma dry etching techniques, such as ECR and ICP, are very promising for deep etching of SiC. The ECR process allows producing very smooth etched surfaces and the control of the degree of anisotropy by the substrate bias. ICP because of high flux with lower-ion energy enables the achievement of excellent anisotropy, low surface damage, smooth morphology, and high etch rate for SiC even at relatively low-bias voltages [32].

A challenge of dry etching processes is the mask. The dry-etch contrast ratio between SiC and typical mask materials as photoresist is low. Thereby deep dry etching requires a hard mask, typically metal such as aluminum (Al), nickel (Ni), or chromium (Cr), to obtain a high etch selectivity [33]. However, many plasma etch systems cannot tolerate the contamination caused by metal etching as a degradation in the health of internal components and electrical shorting occurs [34]. In addition, the presence of a fast-diffusing metal such as Ni within the silicon CMOS fab requires special contamination control precautions [33]. Apart from contamination, during high rate etching, micromasking defects on the etch surface often occurs causing undesirable roughening [34].

Some studies have been conducted to enable the use of non-metallic masks in SiC dry etching, for example, (i) replacing the fluorine-based plasmas by HBr/Cl_2, which allows the use of SiO_2 as etch mask, and (ii) using the AlN as mask material in etching with SF_6/O_2 plasmas [34]. Although both approaches have resulted in etch rate and selectivity lower than those reported to metal masks, a further characterization and optimization of the etch systems can make them promising in SiC MEMS fabrication.

2.2. Thin film

2.2.1. Growth

2.2.1.1. Growth of hexagonal polytypes

The main motivation for the homoepitaxial growth of 4H-SiC is to obtain thick and high quality layers to be used as active regions of power devices and switches with lower losses than conventional silicon-based devices. The 10-kV class SiC P-i-N diodes and insulated gate bipolar transistors (IGBTs) have been fabricated. Furthermore, SiC power Schottky barrier diodes (SBDs), metal-oxide-semiconductor field effect transistors (MOSFETs), and junction field-effect transistors (JFETs) have been already commercialized.

High-quality 4H-SiC epilayers with low defects density are required to fulfill the high performance of SiC power devices. The technology for the realization of bulk 4H-SiC substrates is nowadays well developed but their quality and the possibility to control doping is inferior to the one permitted by epitaxial techniques. Moreover, to realize complex devices, precise control of doping, stacking layers with controlled doping and realization of p-n junction is mandatory. The necessity of very thick epitaxial layers (up to 100 μm) comes from the high bandgap of the material: the breakdown voltage is limited by the depletion region width,

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which depends on the doping level. In order to realize diodes and switches for high-voltage and high power applications, it is necessary to have a material with very low doping concentration, which leads to a very wide depletion layer inside the junction. For this reason, a lot of efforts have been made to develop epitaxial techniques that permit the growth of very thick layers in a reasonable time, maintaining a high material quality.

The 4H-SiC homoepitaxy permits to obtain a material with far superior crystalline quality and lower defect density with respect of 3C-SiC/Si, due to the absence of lattice and thermal mismatch, far superior device performances could be obtained and the adoption of single-crystalline 4H-SiC can significantly extend the range of applicability of MEMS devices in harsh environments. The recent development of photo-electrochemical etching [35] to fabricate MEMS in 4H-SiC increased even more the interest for 4H-SiC homoepitaxy, as will be discussed in the following sections.

The 4H-SiC substrates for SiC homoepitaxy are nowadays commercially available. Due to stacking of Si and C atoms, SiC is a polar material so the substrate surface can actually end with a Si plane or a C plane depending on the crystalline orientation. Si-face substrates are more commonly used because permit to lower the residual nitrogen incorporation with respect of C-face substrates.

Usually, the homoepitaxial 4H-SiC growth is carried out on off-axis substrates, the most common misorientation being about 4° off. It has been found that (0001) vicinal surfaces, due to the presence of surface steps on the growth surface, are able to suppress unwanted polytype formation, thus increasing the crystalline quality. It has also been found that the penetration of basal plane dislocations is effectively hindered in lower off-axis substrates. However, the epilayers grown on these substrates are more prone to form step-bunching and triangular extended defects, due to the presence of terraces [36].

Most of the defects found in the epitaxial layers propagate from the substrate or originate where substrate defects emerge at the surface. It is thus mandatory to deposit SiC onto a substrate with very low defect density, and a lot of effort is thus put in decreasing the substrates defect density, while increasing its size to reduce cost per area.

The most common defects found in the epilayers are: (i) downfalls [37], usually particles formed in the gas phase then precipitated on film surface, (ii) carrots [38, 39], comets [40], or triangular defects [41], elongated defects along the step-flow growth direction, which usually indicate disturbance in the step flow growth. All these defects are known to be device killers and a great effort has been put to optimize the epitaxial growth in order to limit their propagation.

Standard SiC epitaxy is usually carried out in vapor phase epitaxy (VPE) reactors at temperatures between 1500°C and 1700°C, using silane and propane as precursor and hydrogen as carrier gas. The deposition process usually begins with an in situ H_2 etching, in order to improve the substrate surface before the deposition of the epitaxial layer [42]. Depending on reactor configuration and process parameters, etching in H_2+C_3H_8, H_2+SiH_4 or H_2+HCl were also proposed. [43]. Typical C/Si ratios are between 1 and 2, while growth rates for epilayers are usually in the range 5–10 μm/h. However, in order to realize p-i-n junctions and devices

able to block voltages of more than 4 kV, SiC thickness up to 50–100 μm are needed. With such low growth rates the epitaxial deposition needs a very long time and becomes unpractical and expensive. The main problem is that the increase of precursors flow to obtain a faster growth rate results in the formation of silicon droplets in the gas phase, which tends to deplete the nutrient phase and to precipitate on the substrate, thus reducing the epilayer quality. For this reason, the introduction of chlorinated species in the gas phase, such as HCl, methyltrichlorosilane (CH_3SiCl_3, or MTS), trichlorosilane ($SiHCl_3$, TCS), and $SiCl_4$ was investigated. The chlorinated species bind with silicon species in the gas phase because the Cl-Si bond has a lower energy with respect to the Si-Si bond. This permit to avoid the formation and precipitation of Si aggregates and to maintain a mass-transport limited regime where the growth rate is usually linearly dependent on the silane flow. TCS is a precursor of choice of several research groups, since it is safer and more stable that SiH_4 [44]. It brings to the gas mixture both Si and Cl so very high growth rate were achieved using this compound up to 100μm/h without silicon precipitates. Moreover, the use of this precursor has been shown to reduce defects such as basal plane dislocations, point defects, and single Shockley faults. Also, a smoother surface, with root means square roughness as low as 0.18 nm, was demonstrated. Another method to overcome Si reactions in the gas phase is to lower the reactor pressure up to 20–40 mbar but it is not as effective as the chlorine addition.

In order to realize SiC power device, an accurate control and optimization of doped layers is necessary. Doping concentration and uniformity over the substrate area and on all the substrate in a planetary reactor are key-issues for the performance of the devices. The N-type doping is usually carried out with nitrogen.

Nitrogen incorporation has been found to be enhanced by Si-rich gas phase, because N atoms substitute C sites in SiC lattice. P-type doping is less common in literature but is nevertheless very important for devices such as pin diodes and IGBTs. The most common dopant for the growth of p-type layers is aluminum, usually in the form of trimethyl aluminum (TMA). Aluminum tends to substitute Si in the lattice, and it was generally found to depend on the C/Si ratio: at higher values the p-type doping was found to increase. Also, it was found to decrease with the Cl/Si ratio [45].

2.2.1.2. Growth of 3C-SiC films

Cubic silicon carbide (also called 3C or β) shows similar interesting features as the other polytypes, such as wide bandgap (2.39 eV), high breakdown field (2.2×10^6 V/cm), high thermal stability and conductivity, mechanical strength, Mohs hardness of roughly 9, and a Young's modulus that ranges between 330 GPa and 700 GPa depending on the polytype and measurement technique used to acquire the data. In addition to that, 3C-SiC has some peculiar features that fostered the attention of researchers. Among the three most common polytypes (3C, 6H, 4H), the cubic one has the highest saturated drift velocity (2.5×10^7cm/s), which allows to obtain high channel currents in microwave devices [46] and it is helpful for high gain solid state devices. Owing to the higher symmetry and consequently a reduced phonon scattering, 3C-SiC has also the highest electron mobility (≈1000 cm^2/V.s) compared to the other polytypes. The mobility is directly linked to the conductivity of a semiconductor and having a high

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mobility means to be able to obtain a higher current. This will lead to faster capacitance charge. In general, a device built with a high mobility material has a better high frequency response. A high maximum current density is fundamental to increase the number of components per integrated circuit chip, to target large-scale integration. The thermal conductivity of cubic SiC is significant (3.2 W cm^{-1} K^{-1} (poly-3C)) even if compared to those of the most common metals, although slightly lower than other polytypes (3.6 W cm−1 K−1 for 6H–SiC and 3.7 W cm−1 K −1 for 4H–SiC). Additionally, cubic SiC is more and more used as a substrate for the epitaxial deposition of other materials such as gallium nitride [47] or boron nitride [48].

The feature that most determines the success of the applied research on cubic SiC is the possibility of epitaxial growth on silicon, which also has a cubic lattice, but with different constant (≈20% lattice mismatch) [49]. Cubic SiC may also be heteroepitaxially grown on 6H-SiC [50] and on TiC [51]. In addition to that, the bulk SiC contains screw dislocations that can propagate into the epitaxial layer, as in the case of 4H-SiC [52], while it is possible to find nearly defect-free silicon wafers. The availability of silicon wafers with diameter up to 17.7 inches compared to the smaller diameters of commercially available SiC, together with the extreme difficulties to obtain single crystal, large area bulk 3C-SiC crystals, pushed toward silicon the choice for the preferred substrate for 3C-SiC epitaxy. Moreover, the lowering cost of silicon wafers, even for high quality substrates, may help to bring the benefits of SiC technology to consumer devices.

There are many technological advantages using SiC on Si, like the easy integration in silicon electronics, which is already extremely developed and almost ubiquitous. Silicon and silicon carbide have also the same native insulating oxide that might be exploited for the processing and fabrication of Si-SiC-based electronic devices.

The silicon lattice constant is 5.43 Å, while in 3C-SiC it is 4.36 Å, which results in a lattice mismatch of approximately 20% and it can lead to a highly defective epitaxial film, which can be detrimental for electronic devices. The substrate thickness is much higher than the epilayer in the first stages of the growth and this leads the strain to be positioned almost completely in the deposited layer. The effect is the presence of shear stresses in crystal planes that may cause defects formation when a critical thickness of the epilayer is reached. In addition to that, the different thermal expansion (≈8% difference between Si and SiC) fosters the formation of defects during the cooling stage after the growth [53]. A brief review on the defects generated in the SiC layer and strictly correlated to the heteroepitaxy on silicon such as misfit dislocations, twins, stacking faults, threading dislocations, antiphase (or inversion) domain boundaries (APBs on Si (100)), and double positioning boundaries (DPBs on Si (111)) is presented in the next section.

In order to try to reduce the effect of the different lattice parameters between Si and SiC, a carbonization process is often used in the first stages of the epitaxial synthesis. Flowing carbon precursors as propane, methane, or ethane at high temperature over the silicon substrate is a well-known technique [54] to create a thin layer of SiC on the surface of the silicon substrate. Since the SiC lattice parameter is lower than the one of Si, in many cases atoms with bigger size like germanium [55] are added during this process.

Frequently the terms "carbonization" and "buffer layer" are mixed up in literature, but in this work we will refer to carbonization as the process performed only with the carbon precursor turning the outer layers of the silicon substrate into silicon carbide. Other precursors may be added, but not the one for silicon, as it happens in the "buffer layer" process, as reported hereafter. Another technique to ensure the relaxation of elastic energy at the interface between the substrate and the epilayer and to help to stop the propagation of the defects generated at Si-SiC interface is the introduction of a buffer layer prior to the growth. This can be made of silicon and carbon or other materials with less difference in lattice parameters. Typically, the gradual matching between the substrate and final overlayer is ensured via a continuous composition gradient of the buffer layer. A common way to reduce the strain is to pattern the silicon substrate in order to grow SiC crystal with a finite size. The first material used and the most common one to manufacture the mask is silicon oxide [56, 57], but other materials like silicon nitride or aluminum nitride also proved to be effective [58].

The difference in lattice parameter between Si substrate and SiC epilayer causes an "island" growth mode in the very first stages and then may originate many defects in the epitaxial layer, the most common being misfit dislocations, stacking faults and antiphase boundaries.

Misfit dislocations are generated at the interface between the substrate and epilayer, in order to allow the minimization of the lattice strain. The misfit dislocation leaves dangling bonds at the interface and it may propagate as a threading dislocation in the epitaxial layer often causing high leakage currents in a Si/3C-SiC device. TEM images help in understanding the phenomenon (see Figure 6 from [59]): five (111) SiC lattice planes match with four (111) silicon planes, which correspond to a 20% lattice mismatch. In the case of silicon carbide grown over silicon, the difference in the two thermal expansion coefficients contributes to create additional misfit dislocation during the cooling stage after the growth, in order to relieve the stress created at the interface between the two crystals. The voids are another typical defect at the SiC/Si interface that are formed due to outdiffusion of Si during the heating process. If the carbonization is not properly optimized and if a continuous, thick SiC layer is not formed after the low temperature carbonization, during the second heating up to the growth temperature Si outdiffusion from the substrate may occur, leaving voids of the dimension of some μm^2 at the interface [60]. These defects may degrade the electrical properties in vertical devices, where current flows in the Si substrate. Also, the presence of voids may disturb the SiC lattice arrangement above them, thus increasing the concentration of extended defects.

A two-dimensional deviation of the position of the atoms from their corresponding lattice site is called generically "planar defect." The most common types found in heteroepitaxial silicon carbide are stacking faults (SF), twins, and antiphase boundaries (APB).

Stacking faults are an anomaly in the stacking sequence of the different layers (ABCABCABC for 3C, ABABAB for 2H,...) of the crystal. This can be also considered as a local occurrence of another polytype**.** The energy associated with this kind of defects is very low, if compared to other planar defects, because this does not affect the near neighbor bonding; therefore, it is very common to observe stacking faults in cubic silicon carbide along the stacking of {111} planes. It is appropriate to remember that there is almost the same interface spacing between hexagonal and cubic planes [61].

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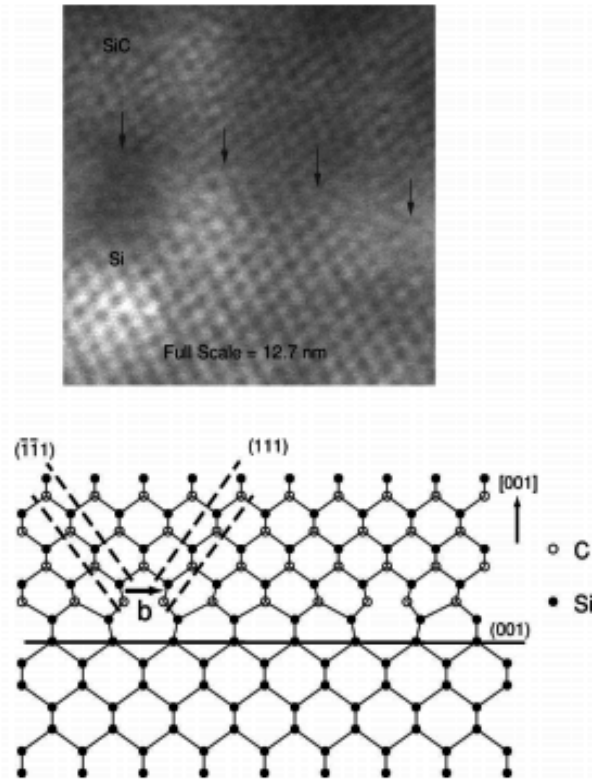

Figure 6. Lattice arrangements at the SiC/Si interface [59]

A twin is a particular defect in the stacking sequence of the planes in which the sequence at the opposite side of the defect plane is mirror images of each other. For example, in the cubic polytype, where the stacking sequence is ABCABCABCABC..., a twin may occur like this: ABCABCBACBACBA. This corresponds to a change in the crystal orientation.

As said previously, the lattice mismatch between the substrate and the epilayer causes the growth of three-dimensional islands in the first stages of the synthesis process known as "island growth mode." The genesis of antiphase boundary domains (APB) is linked to the non-perfect planarity of the substrate. In addition to the initial roughness of the silicon, which to-date can be significantly reduced, the carbonization process introduces many irregularities. During the island growth mode, islands generated in different sites of the substrate may be at different levels owing to the presence of surface steps on the substrate. During the growth and coalescence of the islands, a Si outer layer of an island may bond with a Si layer of another island, thus forming Si-Si bonds. The same phenomenon may occur with C layers of two different islands generating C-C bonds. These boundaries usually propagate along (111) planes, and when two boundaries with opposite orientation combine, they annihilate themselves and the result is the disappearance of the island (and of the APB).

It is possible to generate double position boundaries (DPB) on SiC grown on a (111) surface. This kind of defect is the result of twins that start from the epilayer-substrate interface. The epilayer may orient with respect to the substrate in two ways that are crystallographically equivalent but are rotated 60° relative to each other. When two growth nuclei with different orientations coalesce, a DPB is formed.

2.2.2. Epitaxial SiC quality

Epitaxial 3C-, 4H-, and 6H-SiC have very different properties and characteristics, mainly because of the hetero or homo-epitaxial processes necessary for their deposition. The main issues affecting SiC material quality are due to the substrate used and the growth process. The quality of grown material can be measured mainly in terms of lattice perfection (e.g., from XRD measurements), point defects, extended defects, and residual strain. Usually, the presence of crystalline defects does not hinder the performances of MEMS devices or their capabilities to work in harsh environments.

Due to the ease of fabrication on Si substrate, the polytype of choice for the realization of SiC MEMS is still 3C, and in this case there are still more variables to be considered because this polytype can be deposited in different forms such as crystalline, polycrystalline, or amorphous. These lattice structures have different mechanical properties, such as Young's modulus, which may affect MEMS fabrication.

The mechanical properties of polycrystalline 3C-SiC depend on its characteristics such as preferred orientation, stoichiometry, grain size and shape, and defect. Polycrystalline SiC films have a lower Young's modulus with respect to single crystalline SiC [62], and amorphous films growth at lower temperatures may have even lower Young's modulus values [63]. The Young's modulus of high crystalline quality of 3C-SiC/Si was found to depend on thickness [64] ranging from 1.5×10^{11} to 3.75×10^{11} Pa for thickness between 2 and 3 μm. Considering that the epitaxial quality of SiC increases with thickness due to progressive annihilation of defects and lowering of (002) XRD peak FWHM, the increase in Young's modulus with thickness could be related to lattice quality and defect density. This is one of the most important characteristics to be considered when designing MEMS and still hinder the development of microfabrication. Different growth processes may lead to completely different microstructure properties due to the presence of different type and density of lattice defects and strain content.

In the case of most common MEMS devices, the main requirements of the material are related to mechanical strength and hardness. The presence of residual stress or stress gradients inside the epitaxial layer can also hinder the process of microfabrication in different ways. The stress, originating either from lattice and thermal mismatch in 3C-SiC/Si heteroepitaxy, may cause severe macroscopic bending of the substrate, and may make photolithographic processing impossible or very difficult. At the microscopic level, stress and stress gradients may bend the microstructures or introduce unwanted and unpredictable forces to the system that may alter the behavior of the device or change the predicted resonant frequencies. Different strategies may be adopted to minimize the strain content of 3C-SiC/Si, from the carbonization process optimization or to the deposition of special buffer layers to reduce the lattice mismatch strain

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[60]. However, the presence of thermal mismatch cannot be avoided and could be limited only by reducing the growth temperature.

Reducing the deposition temperature has a tremendous effect on 3C-SiC. High quality crystalline material, with XRD FWHM peak as low 200 arcsec, is usually grown at temperatures higher than 1250–1300°C, with temperatures in the range 1350–1400°C being most commonly used. Precursors of choice are silane and propane, in hot wall VPE reactors. Lowering the growth temperature usually means to significantly degrade the surface morphology and to increase the roughness. In order to maintain a high material quality even at lower deposition temperatures, several alternative precursors have been studied and plasma enhanced techniques have been used. Most of alternative precursors include a Si-C bond in the molecule, such as tetramethylsilane, methyltrichlorosilane, monomethylsilane, hexamethyldisilane, and have lower cracking temperature. However, since for standard MEMS processes the suitable surface termination or the high crystal quality are not mandatory requirements, a trade-off between process conditions and 3C-SiC characteristic may be found. Different deposition techniques such as chemical vapor deposition (CVD), plasma enhanced CVD or sputtering are normally used to deposit polycrystalline or amorphous 3C-SiC at low temperature. Doping of poly or amorphous remains an issue because grain boundaries inhibit dopant incorporation and carrier transport. Moreover, dopant species must crack at low temperature so normally NH_3 (which is toxic) is normally used instead of N_2.

Doping can also influence important properties like crystal quality and strain. The increased doping concentration results in a slightly decreased or increased lattice constant, because N substitute C in the SiC lattice and Al substitute Si for p-type doping. Doping affects thus not only the electrical properties but also the mechanical properties, such as elastic modulus and hardness, so that it can influence the resonance frequency of microstructures. Elastic modulus and hardness of the 3C-SiC thin film may decrease from 350–400 GPa to 150–200 GPa and from 35 GPa to 20 GPa, respectively, with an increase in the nitrogen concentration [65].

2.2.3. Surface micromachining

As it was discussed previously, SiC MEMS has a tremendous potential for the realization of devices operating in harsh, biological environments and high temperatures, exceeding the capabilities of current silicon technology. The polytype of choice for the realization of SiC MEMS is still 3C, either polycrystalline or heteroepitaxial deposited on Si, SOI, or on a sacrificial layer such as SiO_2 or poly-Si. Its main limitations are still due to the low material quality (low crystallinity, high concentration of lattice defects) and the high amount of residual strain due to the heteroepitaxy. However, advances in 3C-SiC epitaxial techniques and the possibility to use well-developed silicon wet-etch techniques to realize SiC MEMS provided a convenient way to fabricate even complex devices. Suspended 3C-SiC structures are released by surface machining using both the wet and dry etching process.

Microfabrication technology on 4H-SiC is much more complicated than the 3C-SiC/Si system because of the lack of a wet etchant for 4H-SiC: conventional wet chemical etching of SiC is not possible at a practical temperature and with suitable etch rates. 4H or 6H-SiC MEMS were

fabricated by expensive and complex techniques such as wafer bonding or smart-cut technique [66], anisotropic electron cyclotron resonance (ECR) etching technique [67], or bulk micromachining [68] from the backside of the wafer. However, the possibility to combine active electronics and microsystems in a single device that could withstand extreme environments and high power is very promising.

2.2.3.1. Processing techniques

SiC can be processed with many of the techniques used also for silicon, while, owing to its mechanical hardness and chemical inertness, not all of the silicon etching techniques can be used for silicon carbide.

Oxidation

It is possible to grow stable thermal oxide layers on all SiC polytypes, as it is commonly done for silicon, but the oxidation rate is much lower. Owing its chemical stability SiC is less likely than silicon to dissociate and react with oxygen to form silicon oxide. Furthermore, CO, one of the reaction products, must diffuse out of the oxide layer for the reaction to proceed. Even if the presence of hydrogen or water vapor increases the oxidation rate, frequently, a thick oxide is required for MEMS fabrication; for this reason the deposition of polycrystalline silicon and following oxidation [69] or the direct deposition of silicon oxide is generally chosen.

Metallization

The deposition of different metallic species to achieve good ohmic or rectifying contacts on SiC has been widely investigated. Depending on the deposition parameters, but mostly on the annealing temperature, different contact behavior can be obtained ceteris paribus.

Annealed Ni for n-type SiC or Al for p-type have been extensively used to obtain ohmic contacts with low contact resistivity [70, 71], while Au [71], Ti [71], Pt [72], or Al [73] have been studied to obtain Schottky barriers. Nevertheless, using some metal that prevents the exploitation of silicon technology, as gold, the metallization should be performed outside of IC fabrication facilities because gold shows electromigration at relatively low temperatures.

SiC-coated MEMS

One can exploit the well-developed state-of-the art of silicon micromachining techniques to obtain devices with complicated design using well-known silicon etchings and covering them with monocrystalline or polycrystalline silicon carbide after the MEMS is released. It has been shown that depositing a thin SiC film over a silicon MEMS improves significantly the wear resistance, decreases the static friction, thus enhancing the device lifetime [74]. The erosion resistance typical of silicon carbide is exploited for SiC-coated MEMS operating in chemically harsh environments [75]. In prospect, the direction of MEMS development will be toward an additional size reduction. For this reason, another feature that is gathering interest is the reduction of adhesion of SiC-coated MEMS [75] thanks to the reduction of surface forces owing probably to topographical surface properties and slower oxidation rates.

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SiC on insulator substrates

There is a great interest in obtaining SiC-on-insulator (SiCOI) substrates for micromachining both for obtaining electrical insulation of the SiC layer from substrate and to use oxide as a sacrificial layer or etch stop.

Silicon-on-insulator (SOI) substrates are obtained by ion implantation of O into the subsurface region of Si wafers, or, more frequently, bonding two silicon wafers covered by oxide. The first attempts to achieve a 3C-SiC layer over silicon oxide starting from a SOI were reported by Reichert et al. [76]. This method has some challenges: the buried oxide quality must be high to withstand the elevated temperatures needed for growing monocrystalline SiC (typically high T, near silicon melting point, 1414°C, ensure better quality epitaxial SiC, but for MEMS a lower crystalline quality may be acceptable). When silicon oxide reaches high temperatures, it undergoes glass transitions [76] and starts to degrade leaving a holey structure (outdiffusion of oxygen [76]) and worsening the electrical characteristics. Another important challenge is the complete conversion of the silicon overlayer into silicon carbide, if not, an undesirable 3C-SiC-on-Si-on-SiO structure is obtained. The carbonization step, as explained in the epitaxial growth part of this chapter, may help in obtaining that, but the method is limited because the diffusion process can reach a limited thickness (around 200 nm in the Si layer). Finely tuning the growth parameters, the production of SiCOI without significant degradation of the buried layers was demonstrated [77].

The "smart cut" process was already developed for obtaining SOI [78, 79]. The process starts with two oxidized silicon substrates, called handle wafer and implant wafer. Hydrogen ions are implanted into the implant wafer under the oxide layer and buried in the silicon bulk at a low depth. After the bonding of the two wafers, an annealing is performed and the implanted hydrogen forms a void layer inside the silicon. After that it is possible to break the implant wafer along these voids leaving the thin silicon layer still bonded to the handle wafer. The same process was successfully used using 6H-SiC substrates with 1-μm-thick deposited oxide layer as implant wafer and 6H-SiC, polycrystalline SiC, and Si layers as handle wafer [77] thus obtaining SiCOI.

As for SOI, wafer bonding is also used to obtain SiCOI [77]; in this case the handle wafer is thermally oxidized silicon. A film of cubic silicon carbide is epitaxially grown on a silicon wafer, and silicon oxide is deposited on this SiC layer. The two wafer oxide surfaces are treated and bonded together, then the handle wafer is protected and the silicon is removed from the second wafer generally using wet etching techniques. The result is a 3C-SiC-on-insulator-on-silicon structure. In literature it is possible to find other wafer bonding processes to obtain SiCOI, such the polysilicon-polysilicon bonding technique [80].

3. A brief overview of the most common SiC microsystem devices

Silicon carbide exhibits piezoresistive and piezoelectric properties as well as superior thermomechanical properties at higher temperatures (>300° C) [81]. Thus, there is a growing

interest in its use as an electromechanical material to replace the silicon in a variety of potential harsh environment applications. Microsystems have become an important direction for SiC technology development. Currently, SiC is the wide bandgap semiconductor material with most potential for MEMS sensors and actuators.

The resonators are one of the most investigated SiC MEMS. SiC resonant structures can present much higher resonant frequencies compared to the same dimensioned Si or GaAs structures due to its high Young's modulus and the relatively low mass density [82]. SiC MEMS resonators have been fabricated with higher power handling capabilities and operating frequencies, compared to those of similar polysilicon-based resonators [81]. Two types of SiC-based resonators have been reported, which use: (i) SiC grown on Si (or SOI) substrates and (ii) homoepitaxial layer grown on single-crystalline 4H- or 6H-SiC substrates.

SiC resonators can be easily fabricated on Si substrates using surface micromachining fabrication technology. This fabrication process is attractive because of integration compatibility with CMOS processes, low-cost film deposition, and minimal compromises between the electrical and mechanical performances of the fabricated structures [81]. Wang et al. reported the fabrication of MEMS resonators based on SiC thin film deposited by low temperature PECVD [82]. These resonators were tested and showed a good performance for harsh environment, such as, high temperature, erosion, and high pressure. The use of mono- and polycrystalline 3C-SiC grown on Si wafers by CVD in resonators able to work at high frequencies with high quality factors has also been reported. The structure of the 3C-SiC resonator is schematized in Figure 7(a) [83].

Regarding the resonant structures made of homoepitaxial layers grown on single-crystalline 4H- or 6H-SiC substrates, their fabrication process is more difficult than that of SiC/Si MEMS. However, high resonant frequency makes 4H-SiC MEMS very attractive for high-sensitivity sensors. Adachi et al. compared the resonance characteristics of 4H-SiC cantilevers on 4H-SiC substrate with the same dimensions of 3C-SiC cantilevers fabricated on Si substrate. It was observed that the resonant frequency of the 4H-SiC cantilevers was 10 times that of 3C-SiC cantilevers [84]. The 4H-SiC cantilevers were fabricated by doping-type selective electrochemical etching of 4H-SiC and their structure is shown in Figure 7(b).

Recently, Yang et al. reported high frequency torsional resonators based on a single-crystal 6H-SiC thin layer on top of a SiO_2-on-Si wafer by using a "smart-cut" process. 6H-SiC smart technology is an alternative process to micromachining of 6H-SiC, which is not only very time consuming but also requires deposited metal masks and still lacks precision when thin films and small dimensions are required for devices [85].

Another important type of SiC MEMS is the piezoresistive sensors for harsh environment applications. In the 1990s, the first piezoresistive pressure sensors developed on 6H-SiC substrates were reported for applications up to 500ºC [86, 87]. These sensors were batch-microfabricated using a combination of photo and dark etching methods to create the diaphragm. In 2004, Ned et al. reported the fabrication of 6H-SiC pressure sensors, with optimized sensing diaphragms containing "bossed" areas, using a combination of deep reactive ion etching (DRIE) and electrochemical etching [88]. The reports on 4H-SiC pressure sensors are

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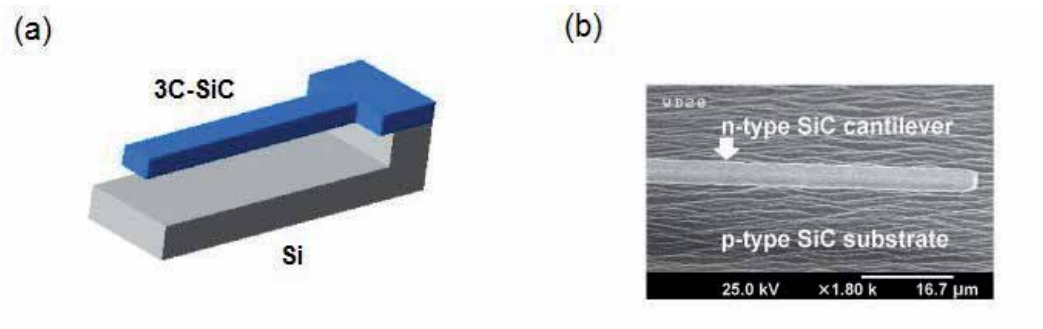

Figure 7. (a) 3C-SiC resonator structure [83] and (b) 4H-SiC micro cantilever [84]

more recent than those of 6H-SiC. In 2011, Akiyama et al. introduced a new approach for the fabrication of 4H-SiC bulk sensors using a mechanical milling (drilling) to form the membrane of the sensor. The detailed milling process done by Tecnisco (Japan) was not disclosed [89]. Earlier this year, Okojie et al. investigated 4H-SiC piezoresistive pressure sensors when operated up to 800ºC. This is the first experimental work published under piezoresistance versus temperature for 4H-SiC [90].

On the other hand, the piezoresistive properties of 3C-SiC and a-SiC films and the influence of the temperature on them have been reported by different authors as reviewed in [91]. The first studies were focused on polycrystalline 3C-SiC films. However, recent publications have demonstrated that a p-type single crystalline 3C-SiC film is a valuable material for MEMS sensors [92, 93].

The potential of SiC for gas sensors in a range of environments has also been reported [94, 95]. These sensors exhibit a simple sensing element based on metal-insulator-semiconductor (MIS) structure, typically a capacitor or a Schottky diode. The use of an insulating layer separating the metal from the SiC allows these devices to operate at temperatures in excess of 900°C [94].

4. Summary

The wide bandgap semiconductor technologies are the key to enable the development of MEMS devices for harsh environment applications. Among them, SiC technology is the most mature from the viewpoint of material quality, manufacturing, and device performance. High quality single crystal wafers are commercially available; wafer size and substrate qualities are increasing whereas wafer cost is decreasing. In the same way, thin film growth techniques have been optimized to accurately synthesize SiC with the necessary properties for its device applications such as material composition, crystal structure, suitable electrical conductivity, morphology, and mechanical characteristics. Despite these advancements in the manufacturing of SiC wafers, thick films, and thin films, there are still processing challenges especially related to doping and micromachining. SiC bulk etching techniques have been developed

seeking high throughput to realize patterned, high-aspect ratio features, such as preservation of sidewall smoothness and etching profile at high etch rates, and high selectivity. In parallel, the progresses on the growth of 3C-SiC on silicon substrates and in surface micromachining techniques have enabled the fabrication of interesting MEMS devices.

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Author details

Mariana Amorim Fraga[1*], Matteo Bosi[2] and Marco Negri[2]

*Address all correspondence to: mafraga@ita.br

1 National Institute for Space Research, Associated Laboratory of Sensors and Materials, Brazil

2 IMEM-CNR Institute, Italy

References

[1] van Rijn, C. J. M. Micro-engineered membranes. In Encyclopedia of Membrane Science and Technology. 1–42, 2013.

[2] Ramesh, P., Krishnamoorthy, S., Rajan, S., Washington, G. N. Fabrication and characterization of a piezoelectric gallium nitride switch for optical MEMS applications, Smart Mater. Struct. 21, 094003 (14pp), 2012.

[3] Jiang, L., Cheung, R. A review of silicon carbide development in MEMS applications. Int. J. Comput. Mater. Sci. Surf. Eng. 2, 225–240, 2009.

[4] Casady, J. B., Johnson R. W. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: a review. Solid-State Electron. 39 (10), 1409–1422, 1996.

[5] MEMS Journal. http://www.memsjournal.com/2007/07/silicon-carbide.html (accessed 30 November 2014).

[6] Auciello, O., Pacheco, S., Sumant, A. V., Gudeman, C., Sampath, S., Datta, A., Carpick, R. W., Adiga, V. P., Zurcher, P., Zhenqiang Ma, Yuan, Hao-Chih, Carlisle, J. A.,

Kabius, B., Hiller, J., Srinivasan, S. Are diamonds a MEMS' best friend? IEEE Microw. Mag. 8 (6), 61–75, 2007.

[7] Peiner, E., Tibrewala, A., Bandorf, R., Lüthje, H., Doering, L., Limmer, W. Diamond-like carbon for MEMS. J. Micromech. Microeng. 17, S83, 2007.

[8] Petersen, M., Heckmann, U., Bandorf, R., Gwozdz, V., Schnabel, S., Bräuer, G., Klages, C.-P. Me-DLC films as material for highly sensitive temperature compensated strain gauges. Diam. Relat. Mater. 20 (5–6), 814–818, 2011.

[9] Heidari, A., Yoon, Y-J., Lee, M. I., Khine, L., Park, M. K., Tsai, J. M. L. A novel checker-patterned AlN MEMS resonator as gravimetric sensor. Sensor. Actuat A Phys. 189, 298–306, 2013.

[10] Bhattacharyya, P., Basu, P. K., Mondal, B., Saha, H. A low power MEMS gas sensor based on nanocrystalline ZnO thin films for sensing methane. Microelectron. Reliab. 48, 1772–1779, 2008.

[11] Fraga, M. A., Furlan, H., Pessoa, R. S., Massi, M. Wide bandgap semiconductor thin films for piezoelectric and piezoresistive MEMS sensors applied at high temperatures: an overview. Microsyst. Technol. 20, 9–21, 2014.

[12] Sheng Yun Wu. Low temperature phase separation in nanowires, nanowires, Paola Prete (Ed.). InTech, 2010. Available from: http://www.intechopen.com/books/nanowires/low-temperature-phase-separation-in-nanowires.

[13] May, P. W. CVD diamond: a new technology for the future? Endeavour 19 (3), 101–106, 1995.

[14] SiC market 2013 Report by YoleDeveloppement. http://pt.slideshare.net/Yole_Developpement/yole-sic-market-report (accessed 10 January 2015).

[15] Diamond Materials for Semiconductor Applications 2013 Report by YoleDeveloppement. http://pt.slideshare.net/Yole_Developpement/yole-diamond-forsemiconductor-applicationsreportnov2013sample (accessed 10 January 2015).

[16] Jones, D. G. Line-of-sight sealed silicon carbide diaphragms for harsh environment sensors. PhD thesis, University of California, Berkeley, 2007.

[17] Reddy, H. D., Volinsky, A. A., Frewin, C. L., Locke, C., Saddow, S. E. Mechanical properties of 3C-SiC films for MEMS applications. Mater. Res. Soc. Symp. Proc. 1049, 2008.

[18] Glass, R. C., Henshall, D., Tsvetkov, V. F., Carter, Jr., C. H. SiC seeded crystal growth. Phys. Status Solidi B 202 (1), 149–162, 1997.

[19] Silicon Carbide lecture by Toomas Rang. isc.dcc.ttu.ee/ieee/ws/WS2003/SiC%20Sagadi.ppt (accessed 20 November 2014).

[20] Griffin, B. A., Habermehl, S. D., Clews, P. J. Development of an aluminum nitride-silicon carbide material set for high-temperature sensor applications. Proc. SPIE9113, Sensors for Extreme Harsh Environments, 91130A, 2011.

[21] Wijesundara, M. B. J., Azevedo, R. G. SiC Materials and processing technology silicon carbide microsystems for harsh environments. MEMS Ref. Shelf 22, 33–95, 2011.

[22] Cheng, L. SiC thin-films on insulating substrates for robust MEMS applications. PhD thesis, University of Cincinnati, 2003.

[23] Ferro, G., Chaussende, D., Jacquier, C. VLS growth of SiC epilayers. In Wide band gap materials and new developments, M. Syväjarvi and R. Yakimova (Eds.). Research Signpost, 91–116, 2006.

[24] Lobod, M. Design Considerations for SiC-based Power Electronics. http://powerelectronics.com/discrete-power-semis/design-considerations-sic-based-power-electronics.

[25] Newman, D. K. Boule shaping of single crystal silicon carbide by wire electrical discharge machining. Master thesis, The University of Utah, 2010.

[26] Hossain, T. K., MacLaren, S., Engel, J. M., Liu, C., Adesida, I., Okojie, R. S. The fabrication of suspended micromechanical structures from bulk 6H-SiC using an ICP-RIE system. J. Micromech. Microeng. 16 (4), 751, 2006.

[27] Zhuang, D., Edgar, J. H. Wet etching of GaN, AlN, and SiC: a review. Mater. Sci. Eng. R Rep. 48, 1–46, 2005.

[28] Dorp, D. H. van, Weyher, J. L., Kelly, J. J. Anodic etching of SiC in alkaline solutions. J. Micromech. Microeng. 17, S50–S55, 2007.

[29] Kimoto, T., Cooper, J. A. Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications. Singapore, Willey, 2014.

[30] Hong, J., Shul, R. J., Zhang, L., Lester, L. F., Cho, H., Hahn, Y. B., Hays, D. C., Jung, K. B., Pearton, S. J., Zetterling, C. -M., Östling, M. Plasma chemistries for high density plasma etching of SiC. J. Electron. Mater. 28 (3), 196–201, 1999.

[31] Chen, Wai-Kai. The VLSI Handbook. Boca Raton, CRC Press, 1999, 1788 pages, ISBN 9780849385933.

[32] Jiang, L., Cheung, R., Brown, R., Mount A. Inductively coupled plasma etching of SiC in SF_6/O_2 and etch-induced surface chemical bonding modifications. J. Appl. Phys. 93 (3) 1376–1383, 2003.

[33] http://micromagazine.fabtech.org/archive/04/07/shovlin.html (accessed 10 February 2015).

[34] Senesky, D. G., Pisano, A. P. Aluminum nitride as a masking material for the plasma etching of silicon carbide structures. IEEE 23rd International Conference on Micro Electro Mechanical Systems (MEMS), 2010 Wanchai, Hong Kong, pp. 352–355.

[35] Feng Zhao, Islam, M. M., Chih-Fang Huang, Photoelectrochemical etching to fabricate single-crystal SiC MEMS for harsh environments. Mater. Lett. 65, 409–412, 2011.

[36] Ha, S., Mieszkowski, P., Skowronski, M., Rowland, L. B. Dislocation conversion in 4H silicon carbide epitaxy. J. Cryst. Growth 244 (3–4), 257–266, October 2002.

[37] Chen, B., Matsuhata, H., Sekiguchi, T., Ichinoseki, K., Okumura, H. Surface defects and accompanying imperfections in 4H–SiC: optical, structural and electrical characterization. Acta Mater 60, 51–58, 2012.

[38] Lee, K. Y., Capano, M. A. The correlation of surface defects and reverse breakdown of 4H-SiC Schottky barrier diodes. J. Electron. Mater. 36, 272–276, 2007.

[39] Hassan, J., Henry, A., McNally, P. J., Bergman, J. P. Characterization of the carrot defect in 4H-SiC epitaxial layers. J. Cryst. Growth 312, 1828–1837, 2010.

[40] Tomita, T., Matsuo, S., Okada, T., Kimoto, T., Mitani, T., Nakashima, S. Structures of comets in a homoepitaxially grown 4H-SiC film studied by DUV micro-Raman spectroscopy. Mater. Sci. Forum 527–529, 339–342, 2006.

[41] Shrivastava, A., Muzykov, P., Pearman, B., Angel, S. M., Sudarshan, T. S. CL/EBIC-SEM techniques for evaluation of impact of crystallographic defects on carrier lifetime in 4H-SiC epitaxial layers. Mater. Sci. Forum 600–603, 139–142, 2009.

[42] Wada, K., Kimoto, T., Nishikawa, K., Matsunami, H. Epitaxial growth of 4H–SiC on 4° off-axis (0 0 0 1) and (0 0 0 1) substrates by hot-wall chemical vapor deposition. J. Cryst. Growth 291, 370–374, 2006.

[43] Dong, L., Guosheng Sun, Jun Yu, Liu Zheng, Xingfang Liu, Feng Zhang, Guoguo Yan, Xiguang Li, Zhanguo Wang. Growth of 4H-SiC epilayers with low surface roughness and morphological defects density on 4° off-axis substrates. Appl. Surf. Sci. 270, 301–306, 2013.

[44] La Via, F., Izzo, G., Mauceri, M., Pistone, G., Condorelli, G., Perdicaro, L., Abbondanza, G., Calcagno, L., Foti, G., Crippa, D. 4H-SiC epitaxial layer growth by trichlorosilane (TCS). J. Cryst. Growth 311, 107, 2008.

[45] Yun Li, Zhifei Zhao, Zhiming Zhu, Zhonghui Li. Aluminum doping property in SiC epilayers grown at high growth rate using chloride-based CVD. J. Mater. Sci Mater. Electron. – published online January 2015.

[46] Shenai, K., Scott, R. S., Baliga, B. J. Optimum semiconductors for high-power electronics. IEEE Trans. Electron. Devices 36 (9), 1811–1823, 1989.

[47] Okumura, H., Ohta, K., Feuillet, G., Balakrishnan, K., Chichibu, S., Hamaguchi, H., Hacke, P., Yoshida, S. Growth and characterization of cubic GaN. J. Cryst. Growth 178 (1–2), 113–133, June 1997.

[48] Mirkarimi, P. B., Medlin, D. L., McCarty, K. F., Barbour, J. C. Growth of cubic BN films on β-SiC by ion-assisted pulsed laser deposition. Appl. Phys. Lett. 66 (21), 2813, May 1995.

[49] Nishino, S., Powell, J. A., Will, H. A. Production of large-area single-crystal wafers of cubic SiC for semiconductor devices. Appl. Phys. Lett. 42 (5), 460, March 1983.

[50] Neudeck, P., Powell, J. A. Homoepitaxial and heteroepitaxial growth on step-free SiC Mesas. In Silicon Carbide – Recent Major Advances, W. J. Choyke, H. Matsunami, G. Pensl (Eds.). Springer-Verlag, Berlin Heidelberg, 2003, p. 179.

[51] Eklund, P., Högberg, H., Hultman, L. Epitaxial TiC/SiC multilayers. Phys. Status Solidi Rapid Res. Lett. 1, 113, 2007.

[52] Ohno, T., Yamaguchi, H., Kuroda, S., Kojima, K., Suzuki, T., Arai, K. Direct observation of dislocations propagated from 4H–SiC substrate to epitaxial layer by X-ray topography. J. Cryst. Growth 260 (1–2), 209–216, January 2004.

[53] Levinshtein, M. E., Rumyantsev, S. L., Shur, M. S. Properties of advanced semiconductor materials: GaN, AIN, InN, BN, SiC, SiGe. Wiley, New York, 2001, p. 216.

[54] Nishino, S., Powell, J. A., Will, H. A. Production of large-area single-crystal wafers of cubic SiC for semiconductor devices. Appl. Phys. Lett. 42 (5), 460, March 1983.

[55] Masri, P., Moreaud, N., Laridjani, M. R., Calas, J., Averous, M., Chaix, G., Dollet, A., Berjoan, R., Dupuy, C. The physics of heteroepitaxy of 3C–SiC on Si: role of Ge in the optimization of the 3C–SiC/Si heterointerface. Mater. Sci. Eng. B 61–62, 535–538, 1999.

[56] Ohshita, Y., Ishitani, A. Low-temperature and selective growth of β-SiC using the SiH2Cl2/C3H8/H2/HCl gas system. J. Appl. Phys. 66 (9), 4535, 1989.

[57] Gupta, A., Jacob, C. Selective epitaxy and lateral overgrowth of 3C-SiC on Si – a review. Prog. Cryst. Growth Charact. Mater. 51 (1–3), 43–69, 2005.

[58] Saddow, S. E., Carter, G. E., Geil, B., Zheleva, T. S., Melnychuck, G., Okhuysen, M. E., Mazzola, M. S., Vispute, R. D., Derenge, M. A., Ervin, M. H., Jones, K. A. Lateral epitaxial overgrowth and pendeo epitaxy of 3C-SiC on Si substrates. Mater. Sci. Forum, 338–342, 245–248, 2000.

[59] Long, C., Ustin, S. A., Ho. W. Structural defects in 3C–SiC grown on Si by supersonic jet epitaxy. J. Appl. Phys. 86, 2509, 1999.

[60] Ferro, G. 3C-SiC heteroepitaxial growth on silicon: the quest for holy grail. Crit. Rev. Solid State Mater. Sci. 40, 56–76, 2015.

[61] Zheng, X., Qu, B., Wang, Y., Dai, Z., Han, J., Yang, H., Liang, J. Comprehensive analysis of microtwins in the 3C–SiC films on Si(001) substrates. J. Cryst. Growth, 233 (1–2), 40–44, 2001.

[62] Werner, M., Krotz, G., Moller, H., Eickhoff, M., Gluche, P., Adamschik, M., Johnston, C., Chalker, P. R. High—temperature Sensors Based on SiC and Diamond Technology. Sensors Update. 5, 141, 1999.

[63] Loboda, M. J., Seifferly, J. A., Dall, F. C. Plasma-enhanced chemical vapor deposition of *a*-SiC:H films from organosilicon precursor. J. Vac. Sci. Technol. A, Vac. Surf. Films, 12 (1), 90–96, 1994.

[64] Anzalone, R., Camarda, M., Canino, A., Piluso, N., La Via, F., D'Arrigo, G. Defect influence on heteroepitaxial 3C-SiC Young's modulus. Electrochem. Solid-State Lett. 14 (4), H161–H162, 2011.

[65] Locke, C., Kravchenko, G., Waters, P., Reddy, J. D., Du, K., Volinsky, A. A, Frewin, C. L., Saddow, S. E. 3C-SiC films on Si for MEMS applications: mechanical properties. Mater. Sci. Forum 615–617, 633–636, 2009.

[66] Cong, P., Young, D. J.Single crystal 6H-SiC MEMS fabrication based on smart-cut technique. J. Micromech. Microeng. 15, 2243, 2005.

[67] Huang, X. M. H., Feng, X. L., Prakash, M. K., Kumar, S., Zorman, C. A., Mehregany, M., et al. Mater. Sci. Forum. Fabrication of suspended nanomechanical structures from bulk 6H-SiC substrates. 1531, 457–460, 2004.

[68] Hossain, T. K., MacLaren, S., Engel, J. M., Liu, C., Adesida, I., Okojie, R. S. The fabrication of suspended micromechanical structures from bulk 6H-SiC using an ICP-RIE system. J. Micromech. Microeng. 16, 751, 2006.

[69] Tan, J., Das, M. K., Cooper, J. A. Melloch, M. R. Metal–oxide–semiconductor capacitors formed by oxidation of polycrystalline silicon on SiC. Appl. Phys. Lett. 70 (17), 2280, April 1997.

[70] Porter, L. M., Davis, R. F. A critical review of ohmic and rectifying contacts for silicon carbide. Mater. Sci. Eng. B 34 (2–3), 83–105, November 1995.

[71] Morkoc, H., Strite, S., Gao, G. B., Lin, M. E., Sverdlov, B., Burns, M. Large-band-gap SiC, III-V nitride, and II-VI ZnSe-based semiconductor device technologies. J. Appl. Phys. 76 (3), 1363, August 1994.

[72] Eriksson, J., Roccaforte, F., Reshanov, S., Giannazzo, F., Lo Nigro, R., Rainier, V., Ferro, G., Siffert, P. Evolution of the electrical characteristics of Pt/3C-SiC Schottky contacts upon thermal annealing. In 2010 wide bandgap cubic semiconductors: from growth to devices: Proceedings of the E-MRS Symposium* F*, 2010, vol. 1292, no. 1, pp. 75–78.

[73] Dai, C.-C., Liu, X.-C., Zhou, T.-Y., Zhuo, S.-Y., Shi, B., Shi, E.-W. Effects of annealing temperature on the electrical property and microstructure of aluminum contact on n-type 3C—SiC. Chinese Phys. B 23 (6), 066803, June 2014.

[74] Ashurst, W. R., Wijesundara, M. B. J., Carraro, C., Maboudian, R. Tribological impact of SiC encapsulation of released polycrystalline silicon microstructures. Tribol. Lett. 17 (2), 195–198, August 2004.

[75] Rajan, N., Zorman, C. A., Mehregany, M., DeAnna, R., Harvey, R. Performance of 3C-SiC thin films as protective coatings for silicon-micromachined atomizers. Thin Solid Films 315 (1–2), 170–178, March 1998.

[76] Reichert, W., Obermeier, E., Stoemenos, J. β-SiC films on SOI substrates for high temperature applications. Diam. Relat. Mater. 6 (10), 1448–1450, August 1997.

[77] Chassagne, T., Ferro, G., Wang, H., Stoemenos, Y., Peyre, H., Contreras, S., Camassel, J., Monteil, Y., Ghyselen, B. Improved SiCOI structures elaborated by heteroepitaxy of 3C-SiC on SOI. Mater. Sci. Forum 389–3, 343–346, 2002.

[78] Bruel, M. Silicon on insulator material technology. Electron. Lett. 1995, 31 (14), 1201–1202.

[79] Bruel, M. Application of hydrogen ion beams to silicon on insulator material technology. Nucl. Instrum. Method Phys. Res. B 108, 1996.

[80] Vinod, K. N., Zorman, C. A., Mehregany, M. A novel SiC on insulator technology using wafer bonding. In Proceedings of International Solid State Sensors and Actuators Conference (Transducers '97), 1997, vol. 1, pp. 653–656.

[81] Nabki, F. Silicon carbide micro-electromechanical resonators for highly integrated frequency synthesizers. PhD thesis, McGill University, 2009.

[82] Yang, Y. T., Ekinci, K. L., Huang, X. M., Schiavone, L. M., Roukes, M. L., Zorman, C. A., Mehregany, M. Monocrystalline silicon carbide nanoelectromechanical systems. Appl. Phys. Lett. 78, 162–164, 2001.

[83] Placidi, M., Godignon, P., Mestres, N., Abadal, G., Ferro, G., Leycuras, A., Chassagne, T. Fabrication of monocrystalline 3C-SiC resonators for MHz frequency sensors applications. Sens. Actuat. B 133, 276–280, 2008.

[84] Adachi, K., Watanabe, N., Okamoto, H., Yamaguchi, H., Kimoto, T., Suda, J. Single-crystalline 4H-SiC micro cantilevers with a high quality factor. Sensor. Actuat. A Phys. 197, 122–125, 2013.

[85] Yang, R., Wang, Z., Lee, J., Ladhane, K., Young, D. J., Feng, P-X. L. 6H-SiC microdisk torsional resonators in a "smart-cut" technology. Appl. Phys. Lett. 104, 091906, 2014.

[86] Okojie, R. S., Ned, A. A., Kurtz, A. D., Carr, W. N. The Ninth Annual International Workshop on Micro Electro Mechanical Systems, MEMS '96, San Diego, 1996.

[87] Okojie, R. S., Ned, A. A., Kurtz, A. D. Operation of α(6H)-SiC pressure sensor at 500°C. International Conference on Solid State Sensors and Actuators, TRANSDUCERS, Chicago, 1997.

[88] Ned, A. A., Kurtz, A. D., Beheim, G., Masheeb, F., Stefanescu, S. Improved SiC Leadless Pressure Sensors for High Temperature, Low and High Pressure Applications. Twenty-First Transducer Workshop Lexington, Maryland, 2004.

[89] Akiyama, T., Briand, D., de Rooij, N. F. Piezoresistive n-type 4H-SiC pressure sensor with membrane formed by mechanical milling. Proceedings of IEEE Sensors 2011, pp. 222–225.

[90] Okojie, R. S., Lukco, D., Nguyen, V., Savrun, E. 4H-SiC piezoresistive pressure sensors at 800 °C with observed sensitivity recovery. IEEE Electron Device Lett. 36 (2), 174–176, 2015.

[91] Fraga, M. A., Pessoa, R. S., Maciel, H. S., Massi, M. Recent developments on silicon carbide thin films for piezoresistive sensors applications. In Silicon Carbide - Materials, Processing and Applications in Electronic Devices, Dr. Moumita Mukherjee (Ed.). InTech, 2011. Available from: http://www.intechopen.com/books/silicon-carbide-materials-processing-and-applications-in-electronic-devices/recent-developments-on-silicon-carbide-thin-films-for-piezoresistive-sensors-applications.

[92] Phan, H.-P., Tanner, P., Dao, D. V., Wang, L., Nguyen, N.-T., Zhu, Y., Dimitrijev, S. Piezoresistive effect of p-type single crystalline 3C-SiC thin film. IEEE Electron. Device Lett. 35, 399–401, 2014.

[93] Phan, H-P, Dao, D.V., Tanner, P., Wang, L., Nguyen, N.-T., Zhu, Y., Dimitrijev, S. Fundamental piezoresistive coefficients of p-type single crystalline 3C-SiC. Appl. Phys. Lett. 104, 111905, 2014.

[94] Wright, N. G., Horsfall, A. B., Vassilevski, K. Prospects for SiC electronics and sensors. Materials Today, 11, 16–21, 2008.

[95] Hunter, G. W., Xu, J., Neudeck, P. G., Lukco, D., Trunek, A., Spry, D., Artale, M., Lampard, P., Sierra Lobo, D. A., Makel, D., Makel, B. W. Silicon carbide gas sensors for propulsion emissions and safety applications. http://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20090014005.pdf (accessed 20 February 2015).

Chapter 2

3C-SiC — From Electronic to MEMS Devices

Jean-François Michaud, Marc Portail and
Daniel Alquier

Additional information is available at the end of the chapter

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Abstract

Since decades, silicon carbide (SiC) has been avowed as an interesting material for high-power and high-temperature applications because of its significant properties including its wide bandgap energy and high temperature stability. SiC is also professed as an ideal candidate for microsystem applications due to its excellent mechanical properties and chemical inertia, making it suitable for harsh environments. Among the 250 different SiC polytypes, only 4H, 6H and 3C-SiC are commercially available. The cubic structure, 3C-SiC, is the only one that can be grown on cheap silicon substrates. Hence, 3C-SiC is more interesting than any other polytype for reducing fabrication costs and increasing wafer diameter. This huge property has been evidenced for more than 30 years using chemical vapor deposition. Despite this key achievement and the growing interest for silicon carbide, no 3C-SiC-based devices can be found on the market whereas 4H-SiC-based devices are more and more largely commercialized. Even so, important headways have been reached for electrical and microelectromechanical systems (MEMS) applications. Therefore, the purpose of this chapter is to address concerns related to electronic applications and MEMS fabrication of 3C-SiC-based devices, trying to give a broad overview on specific issues and challenging solutions.

Keywords: Doping, Defects, Implantation, Etching, MEMS

1. Introduction

Silicon carbide (SiC) is a material presenting different crystalline structures called polytypes. Indeed, more than 250 structures are referenced in the literature [1]. Each polytype is characterized by its own atomic stacking sequence, which can result in cubic, hexagonal or rhombo-

hedral structures, but each structure consists of 50% carbon atoms bonded with 50% silicon atoms. However, among the different polytypes, only two hexagonal structures (4H-SiC and 6H-SiC) and the cubic one (3C-SiC) are commercially available. As the properties are closely related to the crystalline arrangement, they differ from one polytype to another but the tendencies are similar. Silicon carbide presents a high breakdown field (2-4 MV/cm) and a high energy bandgap (2.3-3.2 eV), largely higher than for silicon. As a result, silicon carbide is commonly referred to as a wide bandgap material. The combination of these two properties is a great advantage for the design of electrical devices presenting a low on-state resistance and a low leakage current. In addition, SiC also presents a high saturated electron velocity, which is a crucial parameter for high-frequency applications. Moreover, the silicon carbide thermal conductivity is around three times higher than that observed for silicon. Then, SiC is a material presenting high thermal capability. This property can be very helpful for devices subjected to high temperature and compares favorably to challenging wide bandgap materials such as gallium nitride. Furthermore, SiC is also known as a biocompatible material [2], which is deeply valued for biologic applications [3], and is resistant to high-radiative environments [4]. Within this frame, the cubic polytype of SiC (3C-SiC) is the only one that can be grown on a host substrate with the huge opportunity to grow only the silicon carbide thickness required for the targeted application. The possible growth on silicon substrate has long remained a real advantage in terms of scalability regarding the reduced diameter of commercially available hexagonal SiC. To date, the growth of 3C-SiC on silicon has been demonstrated on 150 mm Si wafers [5]. Since the pioneering works of Nishino *et al.* in the early 1980s, who demonstrated an efficient method to grow 3C-SiC on silicon [6], a large amount of data concerning growth mechanisms has been established by many groups and paved the route for the large dissemination of this material [6-11]. However, despite the fact that the realization of 3C-SiC/Si epilayers appears very promising for taking benefit of outstanding properties of SiC at a low cost, the low crystalline quality of these epilayers in comparison to what is obtained on hexagonal bulk SiC wafers have hampered their use for device fabrication. Nevertheless, the positive trade-off between the cost advantage and a real opportunity for scalability versus reduced quality compared to hexagonal polytypes maintains interest in 3C-SiC for diverse applications.

To summarize, silicon carbide is a promising material with high potential for designing high-power and high-temperature electrical devices, as clearly described in some review papers [12-15].

2. 3C-SiC for electronic applications

2.1. Doping

2.1.1. In situ doping

As explained previously, the great advantage of the cubic polytype is the possibility to grow 3C-SiC films on cheap silicon substrates. Then, in order to consider the elaboration of any 3C-SiC-based device, it is necessary to master its growth. For more than 30 years,

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this theme has been deeply investigated and will not be detailed here. For more detailed information, one could consult some papers as the idea of this contribution is rather to discuss the important progresses accomplished for electrical applications [16, 17].

In order to consider the elaboration of electrical devices, it is necessary to master some technological steps. Among them, doping is probably the most important. Doped layers can be obtained directly during the epitaxial growth of silicon or silicon carbide films. This *in situ* doping presents a major advantage for providing, in a single process, a finalized heterostructure.

The doping-related issues of SiC epilayers have been addressed in the literature in the same time as growth developments because doping incorporation can have a strong impact on growth conditions. For SiC, different dopants can be used, such as nitrogen or phosphorus for n-type doping and boron or aluminum for p-type doping. The choice of dopant is motivated by their low dopant ionization energy. For nitrogen and phosphorus, these energies are around 50 meV, which is in the same order of magnitude as the one observed for donor dopants classically used with silicon, phosphorus and arsenic. However, p-type doping is much more complicated in SiC in comparison with Si. Usually, silicon p-type doping is obtained using boron, which presents an ionization energy around 45 meV. This value is around 6 times lower than the shallowest acceptor dopants observed in SiC using aluminum. As a consequence, SiC p-type doping is a permanent challenge.

In case of nitrogen doping, a quite largely accepted scheme exists and is relevant for many cases (different SiC polytype, SiC polarity (for hexagonal polytypes), or SiC crystalline orientation). It is well known that nitrogen incorporates SiC by substituting with carbon atoms, leading to a N/C site competition effect [18]. A direct consequence is the possibility to tune, to a large extent, the dopant concentration. It can be noticed that most of the published works deal with the incorporation of nitrogen within hexagonal SiC polytypes. For them, the SiC polarity is shown to play an important role [19, 20]. Nitrogen is preferentially incorporated onto a carbon face and can be reduced by increasing the C/Si ratio regarding the site competition effect. In case of the 3C-SiC epilayer, the incorporation of dopant has been less discussed. The presence of extended defects within the epilayer makes the interpretation in the sole term of site competition effect more complicated but some similarities with hexagonal polytypes exist. Regarding the impact of crystalline orientation of the epilayer, it has been shown that both (100) and (111) oriented epilayers present a similar level of nitrogen incorporation, but a different incorporation behavior when C/Si ratio is modified during growth. If (100) oriented epilayers do not present a modification of the incorporation with a C/Si increase, this one is reduced on (111) epilayers with C/Si increase, highlighting a possible influence of the reactor environment in which growth is done as well as a different surface atomic structure between the two crystalline orientations. It is also of interest to point out that doping level acts on the residual stress within 3C-SiC/Si epilayer. Compressive to tensile residual strain states have been reported in accordance to the nitrogen concentration and must be considered when these epilayers are expected to be used for the design of MEMS where stress is an important parameter to take into account [21]. This highlights the special care we must take when considering doping issues in 3C-SiC. It is also important to mention that nitrogen doping does

not imply any memory effect during the growth, allowing the formation of abrupt highly/low doped 3C-SiC heteroepilayers, relevant for the design of devices such as Schottky diodes. In addition, different mechanisms governing the aluminum doping remain a matter of debate. If it is expected that aluminum incorporates in place of silicon atoms, a large dispersion of the experimental results obtained by various groups attests either to some misunderstanding of the mechanism or highlights the influence of the specificity of each growth reactor [19, 22-24]. For instance, Forsberg *et al.* have shown that, regarding the specific attachment of one aluminum atom to one carbon atom via a single bond, the dependence of aluminum incorporation differs from Si to C polarity for hexagonal polytypes. They also report on a constant incorporation on C face and an increasing incorporation with C/Si increase [22]. Other groups have communicated their own results on the topic but often with more or less pronounced dissimilarities [19, 23, 24]. We can highlight that, in most cases, the role of uncontrolled flux of carbon in the reactor, due to graphite surfaces of the vessel, can have a nonnegligible impact on growth and could be partly responsible for the discrepancies reported in results. However, this parameter is inherent to a given growth reactor, making a direct comparison between different groups difficult. To our knowledge, very few groups have reported on Al incorporation into 3C-SiC epilayers [25]. A last point to mention is the fact that chemical precursors used for p doping induce a large memory effect in the growth chamber, which makes it difficult to realize abrupt p/n junctions in a single growth process. The addition of chloride-based gases has been recently proposed to circumvent this drawback and could be helpful for the realization of high-quality bipolar devices [26]. Finally, it is important to mention that using this method, it is not possible to obtain dissimilar planar doping levels. To localize the doping regions, other methods are required.

2.1.2. Implantation

In silicon technology, localized doping can be achieved by means of ion implantation or diffusion processes. In contrast, in silicon carbide technology, due to the extremely low dopant diffusion, ion implantation is the only method available. In order to get n-type highly doped regions, both nitrogen (N) and phosphorus (P) implantations were studied in the literature [27-29].

By means of ion implantation, «impurities» can be selectively introduced into the silicon carbide layer at a thickness depending on the energy. Then, due to the lack of diffusion, obtaining a deep abrupt junction requires multiple-step implantation known as a «box-like» profile, as illustrated in Fig. 1.

The other significant implantation parameter is the dose as it induces the doping level of the implanted material. However, due to the collisions between incorporated ions and the silicon carbide crystal lattice, the implantation step leads to the generation of point and extended defects. In addition, the implanted species are classically in interstitial sites in the crystal lattice. As a consequence, the implanted ions cannot bond with the SiC atoms and thus they cannot participate in the electrical conduction. For both reasons, it is mandatory to provide energy to the targeted material, aiming to recover the crystal lattice (if possible) and to allow the implanted species to locally diffuse for occupying a substitutional site. This energy is provided

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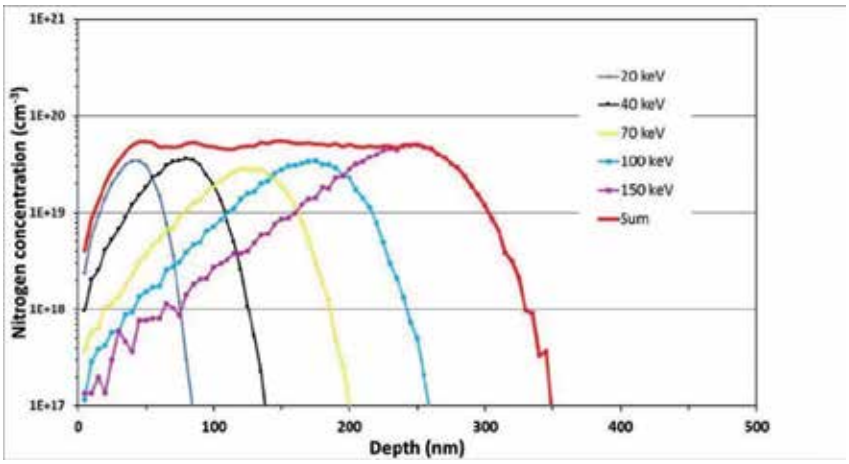

Figure 1. Example of a multienergies implantation required obtaining a nitrogen box-like profile in 3C-SiC with a 5 × 10^{19} cm^{-3} concentration doping level, simulated by SRIM.

by means of an annealing. However, as 3C-SiC is grown on silicon substrates, the post-implantation annealing temperature is limited by the melting point of silicon (around 1410°C). Then, the feasibility of obtaining SiC on cheap Si substrates, which is a huge advantage to elaborate cost-effective devices, is also a «bonus» challenging parameter, in comparison with the 4H and 6H-SiC polytypes, which have to be considered. In fact, this parameter has to take into account the dose calculation as, in some cases, a high dose that is expected to lead to a high doping level could induce an amorphization of the implanted region. In such conditions, even a post-implantation annealing for several hours at 1350°C is not sufficient to entirely recover the crystal lattice [30]. To circumvent this problem, two tracks have been explored, essentially on 4H-SiC. The first one consists of performing the implantation in temperature [31, 32]. This leads to a notable constraint of the defects induced by the implantation step but it involves the use of «original» implanters. The other track was based on a statement considering the size of the species: in the periodic table referencing the chemical elements, nitrogen (N) and carbon are neighbors. The same observation can be made with phosphorus (P) and silicon. As a consequence, it is generally admit that after implantation, N atoms occupy preferentially the SiC carbon sites and P atoms occupy the silicon sites. Based on this statement, co-implantation of both species has been investigated in 4H-SiC and the results were promising [33, 34]. To our knowledge, such a study has never been experimentally completed in 3C-SiC except by our groups [35]. Actually, in 2011, we investigated 3C-SiC doping using nitrogen, phosphorus implantations or their co-implantation. As expected from a physical point of view, crystal damages increased when increasing the atomic mass of the implanted species. However, surprisingly, co-implantation did not demonstrate any interest in comparison with single nitrogen implantation. The defects induced by the higher mass of phosphorus were probably not entirely recovered consecutively to the post-implantation annealing.

Anyway, whatever the implantation conditions, defects are still induced. Then, this step is always associated with a post-implantation annealing. As previously mentioned, due to the

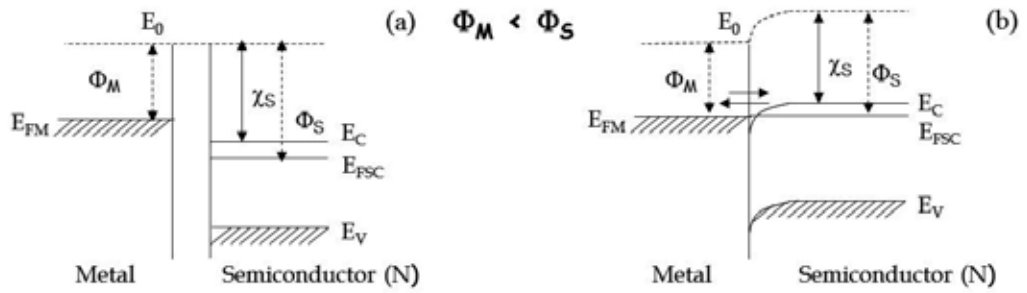

Figure 2. Energy band diagram for a metal and an n-type semiconductor, in the case $\phi_m < \phi_s$, before contact (a) and after contact (b).

presence of the silicon substrate, the temperature is limited to 1400°C, which is several hundred degrees below the temperature commonly used for post-implantation annealing on 4H-SiC substrates. However, even if the temperature is lower, a degradation of the surface can be observed according to the post-implantation annealing temperature. Due to that, as on 4H-SiC polytypes, samples can be annealed with a carbon-cap layer based on pyrolized photoresist [36-39]. This layer is then removed by annealing under oxygen, typically at 800°C. Using this method, it is possible to anneal 3C-SiC samples without any degradation of the surface [35], whereas such a degradation was observed with no capping layer [30]. Another method has been also investigated, using a silane overpressure during the annealing in order to prevent desorption of silicon atoms from the silicon carbide film [40, 41]. Nevertheless, the appropriate gas parameters are strictly related to the design of the furnace then it is very difficult to transpose them from a study to another one. Thus, to our knowledge, this method has been deserted to the detriment of the carbon cap layer process.

2.2. Metal-semiconductor contacts

The wide bandgap of 3C-SiC is a huge benefit for the achievement of electronic devices but the use of an electrical device requires the ability to control current flow, which is closely related to the electrical contacts. When a semiconductor material and a metal are brought into contact, an ohmic or a rectifying contact can be formed. For an ohmic contact, a linear and symmetric current-voltage characteristic is observed for negative and positive applied voltages, which allows current flow through the electrical device. The resistance for such a contact is negligible in comparison to the bulk one. In contrast, a rectifying contact allows the current to flow for only one voltage regime (negative or positive). The formation of an ohmic contact needs the injection of electrons from the metal to the semiconductor material. As a consequence, the metal work function ϕ_m has to be lower than the one for the semiconductor material ϕ_s, as illustrated in Fig. 2 for an n-type semiconductor.

The work function of most metals used in microelectronics field is about 4.5-5 eV, whereas the 3C-SiC electron affinity χ_s is 4 eV. As a consequence, the condition $\phi_s > \phi_m$ is difficult to attain and, hence, the contacts on 3C-SiC are «naturally» rectifying after the metal deposition. To circumvent this problem, the common method considered for wide bandgap material is to get

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a highly doped epilayer beneath the contact. According to the process flow, the high doping level can be obtained directly on *in situ* heavily doped material or on implanted layers but, in both cases, the common idea is to favor the current flow by tunneling through the thin barrier.

For a more detailed explanation, a complete description of the metal-semiconductor contacts can be found in the literature, for example, see [42].

Contact annealing and specific contact resistance

As explained previously, the contacts on highly doped material can present an ohmic behavior as-deposited. However, in most cases, the resistivity of the contact and therefore the specific contact resistance (SCR), is not appropriate to consider electrical applications. As a consequence, the metals are generally annealed posteriorly to the deposition. The aim of annealing is to induce a reaction between the metal and the semiconductor material. For example, titanium reacts with SiC in order to form silicide or carbide phases, presenting suitable electrical characteristics. The annealing itself can be very different from one study to another according to temperature, duration, atmosphere (argon, nitrogen, vacuum), heating ramp, and so on.

SCR values are widely used to characterize a contact. This parameter, which can be obtained by means of transfer length method (TLM) [43] or circular-TLM [44], is preferred over the contact resistance that is closely linked to the surface of the contact. Obtaining ohmic contacts on 3C-SiC with a SCR value as low as possible has been the holy grail of numerous studies for the past two decades [45, 46]. Indeed, it is commonly admitted that a specific contact resistance around 10^{-6} Ω cm^2 is targeted for the elaboration of electrical devices. To obtain ohmic contacts on 3C-SiC, different metals have been considered: Al, Ni, Cr, Pt, Mo, Ti... as well as metal association: Ti/Al, Al/Au, Ti/Ni... essentially on n-type 3C-SiC materials. SCR is also commonly considered to compare different post-implantation annealing conditions, as it is an indirect gauge of the electrical activation.

Nowadays, thanks to the large efforts achieved on this concern, a contact with a 10^{-6} Ω cm^2 SCR value can be «easily» obtained on 3C-SiC material with a high doping level (>10^{19} cm^{-3}). However, until now, no 3C-SiC-based electrical devices can be found on the market. This suggests that the achievement of an ohmic contact, which has long been considered as the main issue to overcome before considering the elaboration of an electrical device, is not the only locking parameter. Actually, this absence can be explained by the high density of defects.

As explained previously, obtaining Schottky contacts is less challenging as the contacts are naturally rectifying on SiC. Metals usually involved for such contacts on 3C-SiC are gold, nickel, aluminum and platinum, in most cases without annealing. However, special care is needed concerning the temperature behavior of as-deposited contacts, as SiC-based electronic devices are generally considered capable of working in these temperatures.

2.3. Role of defects

Since decades, many efforts have been done to improve the crystalline quality of 3C-SiC grown on Si substrate using CVD, but defects are still present. Indeed, intrinsic stress is created during

the deposition process due to the lattice mismatch between 3C-SiC (4.36 Å) and Si (5.43 Å). In addition, thermoelastic stress is introduced during the post-deposition growth, due to the 8% difference in the thermal expansion coefficients of both materials. The resulting stress, which induces the formation of different planar or extended defects in 3C-SiC, is a major parameter leading to a noticeable degradation of the final crystalline quality of the epilayer. Furthermore, the specific nucleation stage adopted to grow SiC on Si, namely, the carburization stage, induces the formation of interfacial voids between SiC and Si, which could limit the interest of this system for the fabrication of devices that require interface abruptness or vertical transport. Finally, the residual stress state of the epilayer must be taken into consideration.

Hereafter, we will give a brief overview on the different kinds of defects encountered in 3C-SiC/Si epilayers grown by chemical vapor deposition. Many published works provide further details. We will also discuss the influence each defect can have on the potential development of electronic and mechanical devices.

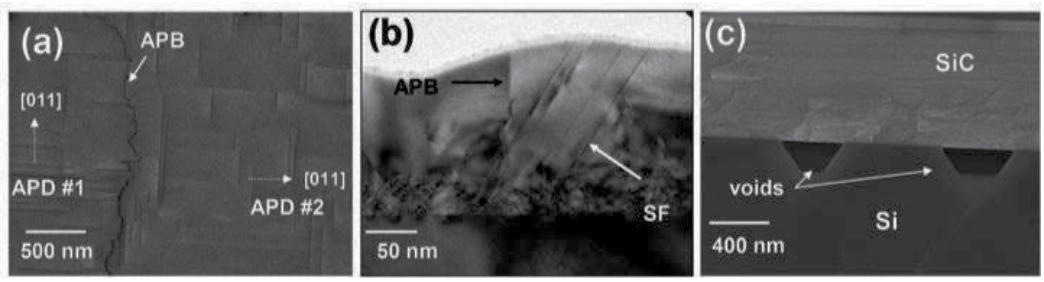

Figure 3. (a) Plane view SEM image of 1-μm-thick 3C-SiC(100) epilayers; dark lines are antiphase boundaries; (b) cross-section TEM of 3C-SiC(100) epilayer where antiphase boundary (denoted APB) and stacking faults (denoted SF) are visible; and (c) cross-section SEM of 3C-SiC(100) evidencing the presence of voids at the SiC/Si interface.

Two kinds of defects within epitaxial 3C-SiC films, as illustrated in Fig. 3 (a, b), are widely documented. Antiphase boundaries are the first kind of defects encountered in 3C-SiC(100) epitaxial layers. They are planar defects formed at the geometrical separation of two 3C-SiC grains differing from each other by a 90° rotation in the Si(100) growth plane [47]. These antiphased domains (APDs) being formed by the presence of steps on the Si surface, these steps being constituted by an odd number of Si atomic steps. The nucleation of 3C-SiC on two different Si terraces leads to the formation of two SiC grains growing along the (100) direction but presenting an opposite atomic stacking arrangement along a <111> direction [47]. These two grains coalesce by forming a defective plane called antiphase boundary (APB). Different authors have studied the mechanisms of propagation and annihilation of these defects. It is admitted that when APBs are propagating along a {111} plane, a «natural» annihilation of APBs by mutual intersection occurs when the 3C-SiC is thickened [48, 49]. Nevertheless, it has also been mentioned that some APBs can propagate vertically along the (100) growth direction [50]. In that case, the thickening of the epilayer does not allow the reduction of their density [51]. The influence of APBs on the electrical properties of 3C-SiC epilayers is poorly documented but they are supposed to be electrically active, as demonstrated by Song *et al.*, who have

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reported their electrical activity [52] (Some details about these measures will be given in the following section). Furthermore, they constitute preferential etching sites when 3C-SiC surfaces are exposed to hydrogen [53]. A second kind of defect of importance is linked to the formation of stacking faults along the <111> planes. Indeed, the formation of two grains of 3C-SiC, differing from one another by a 60° in-plane rotation, is energetically identical but leads to the formation of twinned domains (also called double positioning domains) [54]. In 3C-SiC(100) oriented epilayers, twins are visible as inclined domains respectively to the (100) growth direction. They annihilate mutually by increasing the film thickness. Twins are also present in 3C-SiC(111) oriented layers where they can also be observed parallel to the growth direction (basal double positioning domains) [55]. It is important to notice that most of the published works dealing with 3C-SiC growth on silicon substrates highlight the intrinsic character of such defects and point out the fact that, except by increasing the film thickness, a drastic reduction of their density by only changing growth parameters is not possible. Some authors have proposed different extrinsic routes for effectively reducing the defect densities. In most cases, they require either the suppression of the silicon substrate or the use of specifically patterned Si substrates (undulant substrates) or both (switchback epitaxy) [56-58]. They appear very efficient in solving, to a large extent, the presence of extended defects in 3C-SiC(100) oriented epilayers.

The formation of interfacial voids between the silicon substrate and the 3C-SiC epilayer is another kind of defect, which has a potential impact for the design of 3C-SiC/Si epilayer-based electrical or mechanical devices. Indeed, the formation of 3C-SiC on silicon substrates requires the realization of a first carbonization stage that forms a buffer 3C-SiC layer serving as a seed for the further growth of the epilayer. In most cases, this carbonization stage is performed using a carbon-containing precursor and during this stage some of the silicon substrate is consumed to form the SiC seed [59-62]. This consumption leads to the formation of more or less large cavities (voids) developing at the SiC/Si interface, as can be seen on Fig. 3(c) with noticeable densities ($10^6/10^8$ cm^{-2}). The direct consequence is that SiC/Si is never totally abrupt and can be a real concern for electric vertical transport. Thus, the reduction of the void densities remains a key issue especially for the achievement of electronic devices. This requires extended investigations for identifying the experimental key parameters that govern their formation. Some of them have already been discussed but are not totally efficient for the complete removal of the voids [63-66]. However, Bosi *et al.* have recently underlined the great impact of the thermal ramp used between carbonization and growth stages. They have demonstrated the fabrication of void-free epilayers by playing on that parameter [67]. This could be of great impact for solving the interface issue.

Finally, the residual stress in 3C-SiC/Si epilayers must be addressed. The residual stress comes from the opposite or additive effect of the intrinsic stress, arising during the growth of the epilayer, and the thermal stress induced during the cooling down process and regarding the large thermal expansion coefficient mismatch between SiC and Si. The residual stress is strongly dependent on the surface orientation as well as the growth parameter. In case of 3C-SiC(100) growth, the residual stress can be either compressive or tensile whereas it has always been observed tensile in case of 3C-SiC(111) epilayers. This has a direct consequence on when

such epilayers can be used to fabricate mechanical devices. Our groups have illustrated this issue by reporting on the opposite deflections of cantilevers made from either 3C-SiC(100) or 3C-SiC(111) epilayers [68], as presented in Fig. 4.

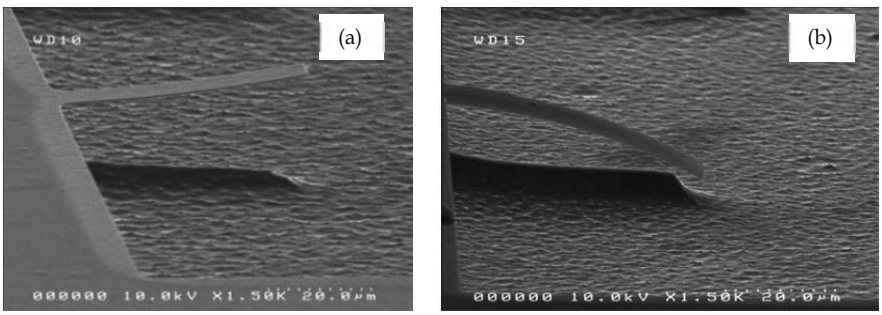

Figure 4. Typical SEM images of 3C-SiC cantilevers formed on the basis of (a) (100) oriented and (b) (111) oriented films.

We will conclude this part by mentioning that grown epilayers present a quite important roughness (R_q roughness in the range of some nm), which is not well suited for additional technological processes such as contacting. In order to achieve sufficient low surface roughness, 3C-SiC epilayers require additional chemical mechanical polishing (CMP), which allows us to significantly reduce the R_q roughness in typical ranges below 0.5 nm [69].

From the abovementioned developments, one can say that a broad knowledge of the different kinds of defects in 3C-SiC epilayers exist but, in comparison, few works have been reported on their influence on the electrical degradation they imply. In 2009, Eriksson *et al.* investigated the electrical characteristics of Au/3C-SiC Schottky diodes as a function of the contact area (Fig. 5) [70]. They observed that the Schottky barrier height increased upon reducing the contact area and, for the smallest diodes, the value approached the ideal barrier height value. As the defect density is deeply related to the size of the 3C-SiC Schottky diodes, this behavior clearly highlights the influence of the defect towards the electrical characteristics of power devices. However, the electrical influence of the extended defects in 3C-SiC was imprecise.

In order to highlight the role of the defects from an electrical point of view, a 3C-SiC sample presenting different doping level was investigated by means of scanning spreading resistance microscopy (SSRM) [52]. The sample presented successive 1-μm-thick layers with a nitrogen doping level ranging from 10^{17} cm^{-3} to 5×10^{18} cm^{-3}, separated by nonintentionally doped layers. As illustrated in Fig. 6(a), the defects are not present in atomic force microscopy (AFM) topography, whereas these are clearly evidenced on the SSRM cartography in Fig. 6(b). This result evidenced, for the first time, the electrical activity of the extended defects in 3C-SiC. Moreover, the inset in Fig. 6(a) highlighted the defect activity is higher than the electrical activity of a 5×10^{18} cm^{-3} nitrogen-doped 3C-SiC epilayer.

The electrical activity of extended defects in 3C-SiC is a major concern for electronic device functioning. Indeed, due to the fact that the current flows preferentially through these defects,

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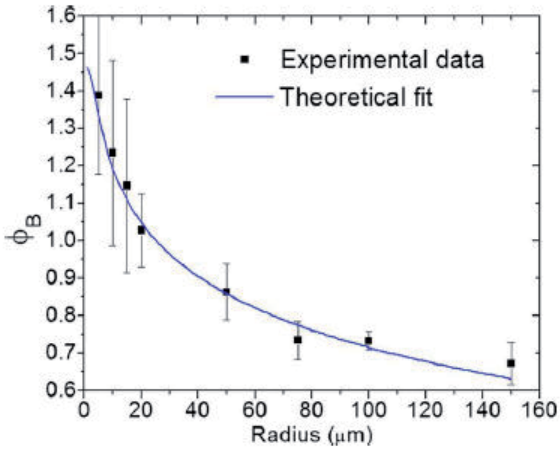

Figure 5. Experimental Schottky barrier height values extracted from I-V measurements as a function of the contact radius of Au/3C-SiC Schottky diodes. The results show that the Schottky barrier height increases upon reducing the contact area and, for the smallest diodes, the value approaches the ideal barrier height value. This result was explained by the defects in 3C-SiC, from [70].

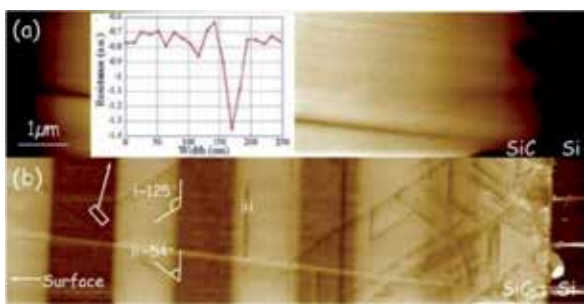

Figure 6. Atomic force microscopy topography (a) and scanning spreading resistance microscopy (b) of a 3C-SiC sample presenting a nitrogen doping level from 10^{17} cm^{-3} to 5×10^{18} cm^{-3}. The inset corresponds to the SSRM signal of the white rectangular area, from [52].

the electrical performances are severely degraded, leading in particular to high leakage currents and low breakdown voltages. As a consequence, even if some major progresses have been completed on 3C-SiC in the field of electronic device elaboration, this kind of application remains too challenging. To address electrical applications using 3C-SiC, a drastic reduction of the defects or of their electrical activity is compulsory.

3. MEMS fabrication: A new challenge for 3C-SiC?

As explained previously, due to the electrical activity of the extended defects in 3C-SiC, this silicon carbide polytype is not yet suitable for the elaboration of electronic devices. However, for microelectromechanical systems (MEMS) applications, silicon carbide presents very

attractive physical and chemical properties (hardness, inertness, melting point, operative temperature, etc.) which open a large field of applications [71-75]. These unique properties are particularly adapted to elaborate microsystems with full satisfactory characteristics and offer the possibility of overcoming those observed on devices using silicon or silicon-based material, which are widely used materials in this field. For example, among the notable properties, silicon carbide biocompatibility is particularly suitable for medical applications [3].

3.1. Silicon carbide etching

The elaboration of MEMS devices requires the mastery of some technological steps. For example, in most cases, an etching stage is required. As shown previously, silicon carbide is a material presenting many properties. Nonetheless, some of them are also drawbacks to elaborate microsystems. This is particularly the case for its chemical inertness. Actually, due to this feature, wet etching of crystalline silicon carbide is extremely difficult as SiC is totally inert to all aqueous etching solutions at room temperature [76]. To our knowledge, the lowest etching temperature referenced in the literature was mentioned by Chu and Campbell in 1965 [77]. They succeeded in etching SiC at 180°C by means of H_3PO_4. The use of other solutions like KOH is also feasible but it requires higher temperatures [78]. In addition, wet etching is often isotropic and, due to the severe conditions required for silicon carbide etching, difficult to localize. Consequently, due to the huge difficulties of wet silicon carbide etching, many efforts were enforced to develop a more user-friendly method. This is the case for plasma etching, which has since been the subject of intense research for decades.

Historically, reactive ion etching (RIE) using a capacitively coupled plasma (CCP) reactor was massively investigated during the 1980s-1990s. In this configuration (usually just called RIE), a RF electromagnetic field is applied between the two electrodes located on both sides of the reactor. Then electrons are accelerated by the high-frequency electric field and ionize the molecules of the gas, leading to a plasma. Consequently, the ions produced can react with the material to etch. For that matter, this behavior is the source of the RIE appellation. Typically, this chemical reaction is isotropic, leading to sloped sidewall profiles. In contrast, according to ion energy, a sputtering effect of the material can also be observed, which mainly results in an anisotropic etching, then to vertical sidewalls. The two effects coexist and the predominance of one effect compared with the other depends on the etching parameters (power, pressure, etc.). As a consequence, in a «simple» RIE reactor, the ion energy is closely linked to their density [79]. Therefore, in the 1990s, another configuration was developed with the emergence of inductively coupled plasma (ICP) reactors. In such a reactor, the plasma, generated by a RF magnetic field as previously shown (RIE power), is also contained inside the chamber, which is encircled by an inductive coil (ICP power). The great advantage of this configuration, in comparison with a RIE reactor, is the possibility to independently control the ion energy (with the RIE power) and their densities (with the ICP power). It enables a wide process flexibility varying from a «pure» RIE plasma to a «pure» ICP plasma.

Silicon carbide plasma etching has been largely investigated. However, as previously mentioned, silicon carbide is a material that is difficult to etch. This is also the case using plasma etching. Then, the success of SiC plasma etching involves the use of severe conditions, which are rarely compatible with the masking materials. For example, photoresist, which is a classical

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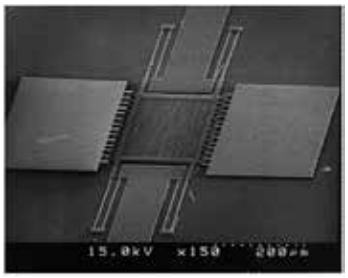
masking material for plasma etching, only operates for thin SiC layers according to the etching selectivity, classically around 1. Silicon dioxide films have also been investigated to act as a mask for plasma etching but it requires thick layers, typically several microns [80, 81]. As a consequence, due to the poor selectivity of these materials, a metallic mask is usually preferred. Among them, aluminum has been largely investigated and results to a selectivity at least one order of magnitude higher than the one observed with photoresist [82, 83]. Unfortunately, the use of an aluminum mask induces a micromasking effect [84]. This phenomenon, which can lead to a grass-like surface of the SiC film, is explained by the formation of Al_2O_3, which is a nonvolatile species [82]. Thus, nickel is widely used as a hard mask instead of aluminum as it presents the interesting detail of being chemically inert towards the chemical species of the plasma. Then, as nickel is only etched by ion bombardment, no micromasking effect is observed using such a metal, except if the mask design is not spaced out enough, which prevents the evacuation of nonvolatile species, as explained in [85].

In terms of chemistry, silicon carbide plasma etching has been largely investigated using fluorinated gases as it is generally admitted that fluor atoms react with both silicon and carbon to form, respectively, SiF_x and CF_y species [86]. These volatile species are then eliminated by pumping. In some studies, an additional gas, which could be argon or oxygen, is added to the fluorinated gas. Argon is attributed to promoting physical sputtering and also to increasing the dissociation of the plasma gas into reactive species, which therefore increase the etch rate [87]. In contrast, the role of oxygen is controversial. Some authors suggest that oxygen atoms participate directly in the etching of the SiC film by the formation of CO and CO_2 species [88]. Other authors suggest that oxygen, for a typical fraction of 20%, helps to dissociate the fluorinated gas then produces more fluor atoms [71]. However, for higher fractions, it leads to a dilution of the fluorinated gas and then to a decrease of the etching rate [89]. This behavior was also observed by Jiang *et al.* [90]. Beheim *et al.* also observed an increase of the micro-trenching effect in all processes where O_2 was incorporated [91]. This behavior was hypothesized by the formation of a SiF_xO_y layer that could have a greater tendency to charge than SiC. As a consequence, the charges on the sidewalls lead to the deflection of the incident ions, resulting in a microtrenching phenomenon. This same behavior has been observed by other groups [92, 93]. In addition, a small amount of oxygen, typically less than 10%, can be also added to the SF_6 gas in order to react with a nickel mask. The aim is to promote the formation of a nickel oxide, which is more resistant to the plasma treatment [68]. It can be helpful for the plasma etching of thick silicon carbide layers as it increases selectivity. In conclusion, the benefit of using oxygen for silicon carbide plasma etching is still debated. Nevertheless, even if the full mechanisms involved in SiC plasma etching are not perfectly identified, this step, compulsory to consider the elaboration of MEMS devices, is now mastered with typical etching rate at around 1 μm/min.

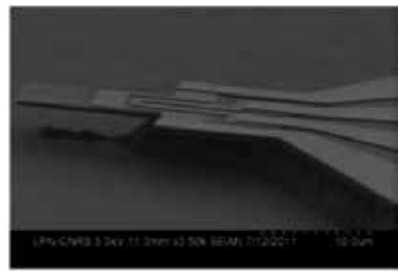
3.2. MEMS devices and mechanical properties

As already discussed, due to its physical and chemical properties, 3C-SiC is a very promising material to elaborate MEMS devices. Some examples of already completed 3C-SiC-based microsystems are presented in Fig. 7.



Lateral resonator [94]

Vertical resonator [83]



Nanocantilever [95]

Figure 7. Examples of 3C-SiC MEMS devices, from the literature.

For most applications, the idea is to take advantage of the SiC physical properties. For example, the resonant frequencies of the vertical resonators presented in Fig. 7 were around 40% higher than those obtained with an equivalent Si device and the quality factor was twice higher [83]. In addition, using 3C-SiC allows to achieve MEMS devices easier. Indeed, state of the art silicon-based technology is not compatible with conditions encountered by most devices. To become sufficient, some silicon-based devices require the use of cooling system or radiation shielding. These extra items add volume and weight to the initial MEMS devices which is in contradiction with the miniaturization targeted using MEMS devices. Moreover, for specific applications in the field of spatial or aeronautics, an increase of the weight leads to a severe rise of the cost [96]. Considering the silicon carbide physical properties, these problematics should be bypassed using 3C-SiC-based MEMS devices.

As 3C-SiC is grown on silicon, MEMS elaboration generally requires partial etching of the substrate. To do that, two ways are possible as, as opposed to silicon carbide, silicon can be easily etched by means of wet etching. Indeed, different wet-etching solutions have been used such as potassium hydroxide (KOH) mixtures [97, 98] or HF:HNO_3/H_2O combination with [99] and without the adjunction of acetic acid [83]. This feasibility fully benefits from SiC's chemical inertia. However, it is also possible to directly etch the silicon substrate by means of plasma etching [80]. Indeed, according to the design of the microsystem, this step can even be completed in the same run that the plasma etching of the SiC film as both materials require fluorinated gases to be etched. It must also be noted that a modification of the plasma parameters can be helpful to favor the isotropic etching of the silicon substrate, in order to liberate the microsystems, as presented in Fig. 4.

For each vibrating system, the Young's modulus is a key parameter. As a consequence, many research works were focused on this mechanical property. To determine the Young's modulus, two main methods are used, nanoindentation [100-102] and the resonant frequency measurement of clamped-free cantilevers. The first method consists of penetrating the SiC material by using a hard tip whose mechanical properties are known. Usually, the geometry of the indenter is known with high precision, which is the case for the Berkovic tip presenting a three-sided pyramid geometry. The indenter tip progressively penetrates the investigated material with the applications of increasing load. During the indentation process, depth penetration is

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recorded as a function of the applied load, resulting in a load vs. displacement curve [103]. As this method cannot be used to provide an elastic modulus value in a particular direction, nanoindentation is more fitting for polycrystalline materials [104]. The second method, mainly used for the determination of 3C-SiC mechanical properties, consists of determining the resonance frequency of clamped-free cantilevers, as illustrated in Fig. 8.

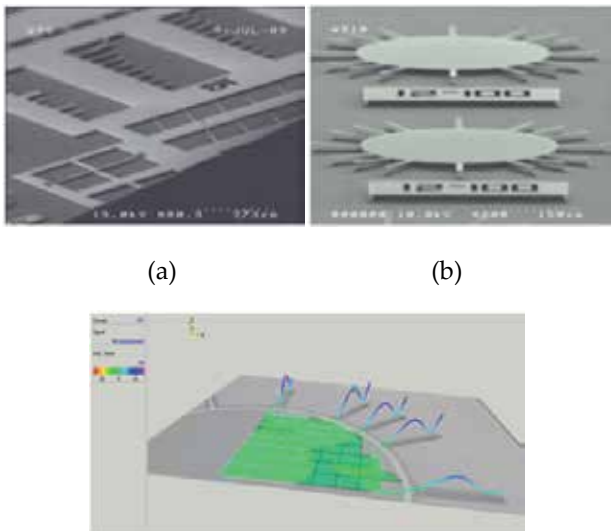

Figure 8. (a) Multiple size cantilevers enabling Young's modulus extraction (b) 'Sun' cantilevers and associated vibration (c) measured by Polytec MSA 500 Laser Doppler Vibrometer (vibration mode 2).

This parameter, which can be directly determined using optical vibrometers, is used to calculate the Young's modulus as the resonance frequency of a clamped-free beam, for the mode n, is a function of device geometry and material properties as presented in the following equation [105]:

$$f_n = \frac{(\lambda_n)^2}{2\pi\sqrt{12}} \frac{h}{L^2} \sqrt{\frac{E}{\rho}} \tag{1}$$

where λ_n is a constant depending of the mode ($\lambda_1 = 1.875$, $\lambda_2 = 4.694$), h and L are, respectively, the thickness and the length of the beam, E the Young's modulus and ρ the cantilever material density (3.2 g cm^{-3} for SiC). Indeed, as mentioned previously, the use of this method has highlighted the fact that 3C-SiC (100) cantilevers are bended downwards whereas 3C-SiC (111) cantilevers are bended upwards, which is clearly visible on submicron-thick cantilevers, and reveal opposite residual stress effects [68, 106].

Equation (1) assumes that the cantilever is free at one end and fixed to the bulk material at the other. Nonetheless, consecutive to the etching of the silicon substrate used to release the beams, an undercutting of the attachment region can be obtained. Consequently, the anchorage point is not totally fixed. As an example, for cantilevers presenting a 20-μm width, an over-etching of more than 10 μm can be observed. The consequence is an increase of the cantilever effective length [107], lowering the vibration frequency and leading to an underestimation of the Young's modulus. Then, in order to prevent a mistaken value of the Young's modulus, only «long» cantilevers should be considered, that means cantilevers presenting a length of around one order of magnitude higher than the over-etch value, as presented in Fig. 9.

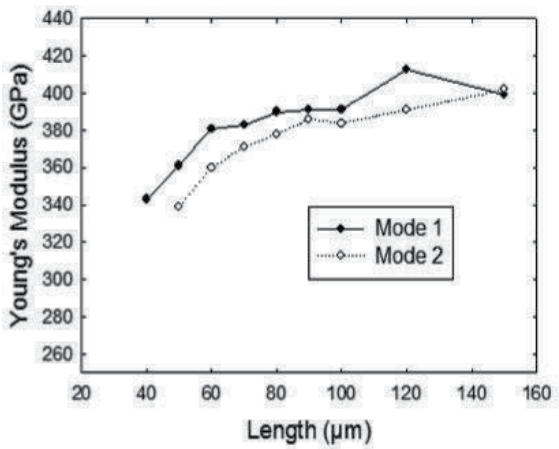

Figure 9. Calculated values of the Young's modulus as a function of the cantilever length for a 0.5-μm-thick (111) 3C-SiC sample. The results are presented for vibration modes 1 and 2, on 10-μm-wide cantilevers.

In the literature, the values presented for the 3C-SiC Young's modulus are quite dispersed; however, a 450 GPa value for the 100 orientation, is usually acknowledged. However, since 1992, Tong *et al.* [108] have suggested that defect density could play a role in Young's modulus. As the crystalline quality is closely dependent of the 3C-SiC deposition method, the dispersion could be explained by the defect density. In 2009, Mastropaolo *et al.* investigated single crystal and polycrystalline 3C-SiC for MEMS applications [81]. In their work, cantilever resonators were fabricated from the two types of materials using films deposited by CVD. Experimental resonance frequencies were used to calculate the Young's modulus. Based on this method, they determined a Young's modulus of 446 and 246 GPa for a 2.3-μm-thick single crystalline (100) 3C-SiC epilayer and for a 1.4-μm-thick polycrystalline material, respectively. That same year, Locke *et al.* also investigated the Young's modulus of 3C-SiC by means of nanoindentation [102]. For a 2.3-μm-thick (100) 3C-SiC single crystalline material, they obtained a Young's modulus of 433 GPa, which was in good agreement with the results obtained by Mastropaolo *et al.* They also studied this parameter for (111) 3C-SiC films and obtained a value higher than 500 GPa. However, the Young's modulus determined on a polycrystalline material, evaluated to 457 GPa, was quite different from the one observed by Mastropaolo *et al.*, whereas, in both

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cases, the thickness of the 3C-SiC layers was similar. Based on these studies, it was then difficult to clearly determine the influence of the defects towards the mechanical properties of 3C-SiC films.

In 2010, our groups also investigated the Young's modulus of 3C-SiC films by means of the resonance frequencies of clamped-free cantilevers, but for thin 3C-SiC epilayers (<550 nm) as submicron 3C-SiC layers are required for specific applications, for example, in the field of atomic force microscopy, as presented in Fig. 7(c) [95]. For (100) and (111) 3C-SiC oriented films, the Young's modulus has been evaluated to 350 GPa [68]. This result was in contradiction with the literature data obtained on thicker 3C-SiC materials. As a consequence, complementary analyses of Young's modulus on thicker layers (then on less defective material), and on polycrystalline material (highly defective) were performed. The same experimental protocol lead to a Young's modulus evaluation of 450 GPa for a 2-μm-thick (100) 3C-SiC layer and close to 500 GPa for a 1-μm-thick (111) layer. For polycrystalline material, the Young's modulus was evaluated to 100-150 GPa. This behavior was attributed to the defect density and the evidence that the mechanical properties of 3C-SiC films were severely affected by the defect density, which has been suggested since 1992, was finally highlighted.

More recently, Anzalone *et al.* also studied the defect influence on heteroepitaxial 3C-SiC Young's modulus [109]. They found Young's modulus values from 217 to 425 GPa for (100) 3C-SiC films with a thickness ranging from 2.04 to 3.13 μm, confirming that Young's modulus is strictly related to the defect density and, therefore, to the film's thickness. In 2012, the same group also investigated the dependence of mechanical properties of 3C-SiC film with defect densities artificially induced by ion implantation [110]. The main conclusion of this paper was the correlation between the Young's modulus and the defects induced by the implantation step.

To conclude on this part, even if the defect density is not deeply detrimental for the functioning of MEMS devices, as defects can affect the 3C-SiC mechanical properties, their influence has to be taken into account.

3.3. What's next for 3C-SiC-based MEMS?

The high 3C-SiC Young's modulus is not the only interesting property for MEMS applications. The chemical inertia and the temperature resistance of this material are also huge benefits to achieve microsystems that can operate in harsh environments.

In 2013, Michaud *et al.* succeeded in achieving a single crystalline 3C-SiC membrane on a 3C-SiC pseudo-substrate [111], using an original 3C-SiC/Si/3C-SiC stack grown on a 100 silicon substrate, as presented in Fig. 10. The process was based on the use of the sandwiched silicon film acting as a sacrificial layer. Such a structure could be the starting point for the achievement of complete SiC-based MEMS devices. Indeed, this result seems promising as, in 2014, Anzalone *et al.* also investigated the use of a Si/3C-SiC/Si heterostructure [112]. For example, using a thick 3C-SiC epilayer, the silicon substrate could be completely etched in order to obtain a self-supporting monocrystalline 3C-SiC structure. Such a feasibility could be very helpful for medical applications or for devices functioning in harsh environments for which the presence

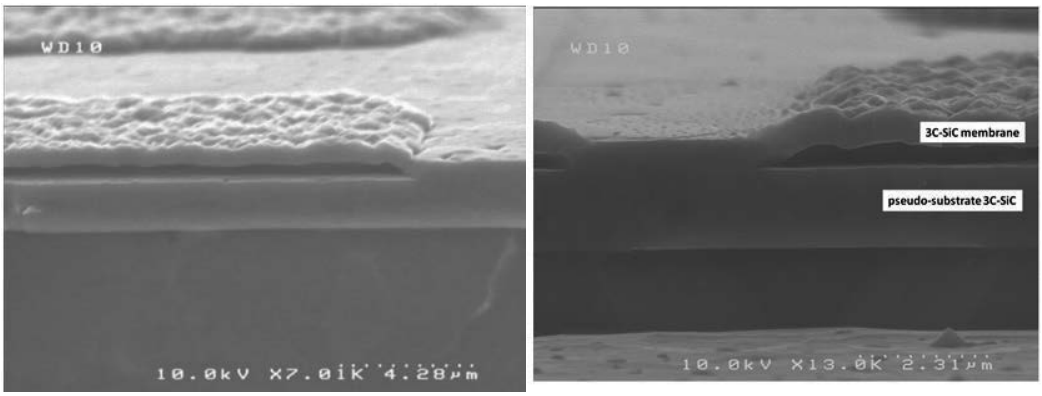

Figure 10. Single crystalline 3C-SiC membrane on a 3C-SiC pseudo-substrate, from [111].

of a silicon substrate is restraining. In addition, thanks in large part to the efforts engaged in controlling the doping level of 3C-SiC films, new MEMS devices could be achievable with, for example, the use of a highly doped layer acting as an electrode.

4. Conclusion

For decades, silicon carbide has been the subject of intensive research activities. This material exists in more than 250 identified structures called polytypes, but only 4H, 6H and 3C-SiC are commercially available. Among these polytypes, only the cubic one, 3C-SiC, can be grown on silicon substrates. This feasibility is a huge benefit to reducing the cost of the devices but, whereas SiC-based devices are more and more present in the market, 3C-SiC-based ones are lacking. However, important headways have been reached for electrical and MEMS applications using this material. Then, the purpose of this chapter was to summarize the noticeable results obtained on this material.

For electrical considerations, large efforts have been done to control the doping level by means of ion implantation, which is a crucial issue to consider in the achievement of any electrical device. Indeed, beyond the necessity to get localized doped layer for electrical applications, doping is also mandatory to obtain ohmic contacts on 3C-SiC. This was probably the most significant issue investigated in the literature last two decades. Fortunately, due to the large efforts engaged for this problematic, specific contact resistance around 10^{-6} Ω cm^2 are now «easily» obtained on 3C-SiC, which is a suitable value to consider the elaboration of electrical devices. However, for the moment, 3C-SiC-based electrical devices are still absent from the market, whereas the success of a fit ohmic contact and SiC local doping have long been considered as the main issues to overcome. Actually, this absence is explained by the high defect density, which has been proved quite recently by means of spreading scanning resistance microscopy. As a consequence, a drastic reduction of the defects or of their electrical activity is mandatory to expect elaborating noteworthy electronic devices.

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In contrast, for microsystem applications, the high defect density combined with its electrical activity does not seem to be a challenging issue. Actually, some examples of microsystems like nanocantilevers or resonators have been already obtained using 3C-SiC. For such applications, the physical and mechanical properties are very motivating as they outshine those of silicon or silicon-based materials typically involved in the field of MEMS devices. These achievements have been accessible at the cost of large efforts on plasma etching. Indeed, this problem has been largely investigated in the last few decades, with probably the same interest as that of obtaining an ohmic contact for electrical applications. Even if a comprehension of the plasma etching mechanisms is not fully acquired, inductively coupled plasma etching is now a well-mastered technology. In addition, the feasibility to grow 3C-SiC/Si/3C-SiC stack on 100 silicon substrates, demonstrated recently, could open the way for the achievement of new MEMS devices, operating, for example, in harsh environments. As a consequence, for this application field, 3C-SiC is still a promising material with a huge potential remaining to be explored.

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Author details

Jean-François Michaud[1*], Marc Portail[2] and Daniel Alquier[1]

*Address all correspondence to: jean-francois.michaud@univ-tours.fr

1 University Francois Rabelais of Tours, GREMAN, BP, Tours Cedex 2, France

2 CRHEA CNRS-UPR10, Valbonne, France

References

[1] T. Daulton, T. Bernatowicz, R. Lewis, S. Messenger, F. Stadermann and S. Amari. Polytype distribution in circumstellar silicon carbide. Science 296 (2002) 1852.

[2] S.E. Saddow, C.L. Frewin, M. Reyes, J. Register, M. Nezafati and S. Thomas. 3C-SiC on Si: A biocompatible material for advanced bioelectronic devices. ElectroChemical Society Transactions 61(7) (2014) 101.

[3] S.E. Saddow. Silicon Carbide Biotechnology: A Biocompatible Semiconductor for Advanced Biomedical Devices and Applications. Elsevier Science (2011).

[4] F. Navaa, E. Vittone, P. Vanni, G. Verzellesi, P.G. Fuochi, C. Lanzieri, M. Glaser. Radiation tolerance of epitaxial silicon carbide detectors for electrons, protons and gamma-rays. Nuclear Instruments and Methods in Physics Research A 505 (2003) 645.

[5] A. Severino, C. Bongiorno, N. Piluso, M. Italia, M. Camarda, M. Mauceri, G. Condorelli, M.A. Di Stefano, B. Cafra, A. La Magna, F. La Via. High quality 6 inch (111) 3C-SiC films grown on off axis (111) Si substrates. Thin Solid Films 518 (2010) S165.

[6] S. Nishino, J.A. Powell, H.A. Will. Production of large-area single-crystal wafers of cubic SiC for semiconductor devices. Applied Physics Letters 42 (1983) 460.

[7] S. Nishino, H. Suhara, H. Ono, H. Matsunami. Epitaxial growth and electric characteristics of cubic SiC on silicon. Journal of Applied Physics 61 (1987) 4889.

[8] P. Liaw, R.F. Davis, Epitaxial growth and characterization of beta-SiC thin films. Journal of Electrochemical Society: Solid State Science and Technology 132 (1985) 642.

[9] A.J. Steckl, J.P. Li. Epitaxial growth of beta-SiC on Si by RTCVD with C_3H_8 and SiH_4. IEEE Transactions on Electron Devices 39 (1992) 64.

[10] N. Nordell, A. Schöner, S.G. Andersson. Design and performance of a new reactor for vapour phase epitaxy of 3C, 6H and 4H SiC. Journal of Electrochemical Society 143 (1996) 2910.

[11] O. Kordina, L.O. Björketun, A. Henry, C. Hallin, R.C. Glass, L. Hultman, J.E. Sundgren, E. Janzen. Journal of Crystal Growth 154 (1995) 303.

[12] M.L. Locatelli and S. Gamal. Silicon carbide against silicon: a comparison in terms of physical properties, technology and electrical performance of power devices. Journal de Physique III 3 (1993) 1101.

[13] J.B. Casasy and R.W. Johnson. Status of silicon carbide (SiC) as a wide-bandgap semiconductor for high-temperature applications: A review. Solid-State Electronics 39(10) (1996) 1409.

[14] P.G. Neudeck. Silicon Carbide Electronic Devices in Encyclopedia of Materials: Science and Technology (2001).

[15] O. Kordina and S.E. Saddow. Silicon Carbide Overview in Advances in Silicon Carbide Processing and Applications. Artech House, Inc. (2004).

[16] M. Eickhoff, H. Möller, J. Stoemenos, S. Zappe, G. Kroetz, M. Stutzmann. Influence of crystal quality on the electronic properties of n type 3C-SiC grown by low temperature low pressure chemical vapour deposition. Journal of Applied Physics 95 (2004) 7908.

[17] G. Ferro. 3C-SiC heteroepitaxial growth on silicon: the quest for holy grail. Critical Reviews in Solid State and Materials Sciences 40(1) (2015) 56.

[18] D.J. Larkin, P.G. Neudeck, J.A. Powell, L.G. Matus. Site competition epitaxy for superior silicon carbide electronics. Applied Physics Letters 65 (1994) 1659.

[19] K. Kojima, S. Kuroda, H. Okumura, K. Arai. Influence of lattice polarity of nitrogen and aluminum doping on 4H-SiC epitaxial layer. Microelectronic Engineering 83 (2006) 79.

[20] T. Kimoto, T. Hirao, S. Nakazawa, H. Shiomi, H. Matsunami. Homoepitaxial growth of 4H-SiC(03-38) and nitrogen doping by chemical vapour deposition. Journal of Crystal Growth 249 (2003) 208.

[21] M. Zielinski, M. Portail, T. Chassagne, S. Juillaguet, H. Peyre. Nitrogen doping of 3C-SiC thin films grown by CVD in a resistive heated horizontal hot wall reactor. Journal of Crystal Growth 310 (2008) 3174.

[22] U. Forsberg, O. Danielsson, A. Henry, M.K. Linnarson, E. Janzen. Aluminum doping of epitaxial silicon carbide. Journal of Crystal Growth 253 (2003) 340.

[23] H. Pedersen, F.C. Beyer, A. Henry, E. Janzen. Acceptor incorporation in SiC epilayers grown at high growth rate with chloride based CVD. Journal of Crystal Growth 311 (2009) 3364.

[24] R. Arvinte, M. Zielinski, T. Chassagne, M. Portail, A. Michon, P. Kwasnicki, S. Juillaguet, H. Peyre. Investigation of aluminum incorporation in 4H-SiC epitaxial layers. Materials Science Forum 806 (2015) 45.

[25] G. Wagner, M. Schmidbauer, K. Irmscher, P. Tanner, R. Fornari. P type doping of epitaxial 3C-SiC layers on silicon (001). Materials Science Forum 615-617 (2009) 165.

[26] S. Li, K. Kojima, Y. Ishida, S. Saito, S. Yoshida, H. Tsuchida, H. Okumura. Suppressing Al memory effect on CVD growth of 4H-SiC epilayers by adding hydrogen chloride gas. Japanese Journal of Applied Physics 53 (2014) 04EP07.

[27] R. Lossy, W. Reichert, E. Obermeier. Characterization of 3C-SiC doped by nitrogen implantation. Materials Science and Engineering B 46 (1997) 156.

[28] E. Taguchi, Y. Suzuki, M. Satoh. Electrical Properties of N ion implanted layer in 3C-SiC(100) grown on self-standing 3C-SiC substrate. Materials Science Forum 556-557 (2007) 579.

[29] J. Wan, M.A. Capano, M.R. Melloch. Formation of low resistivity ohmic contacts to n-type 3C-SiC. Solid-State Electronics 46 (2002) 1227.

[30] A.E. Bazin, J.F. Michaud, C. Autret-Lambert, F. Cayrel, T. Chassagne, M. Portail, M. Zielinski, E. Collard and D. Alquier. Ti-Ni ohmic contacts on 3C-SiC doped by nitrogen or phosphorus implantation. Materials Science and Engineering B 171 (2010) 120.

[31] A. Heft, E. Wendler, T. Bachmann, E. Glaser, W. Wesch. Defect production and annealing in ion implanted silicon carbide. Materials Science and Engineering B 29 (1995) 142.

[32] V. Khemka, R. Patel, N. Ramungul, T.P. Chow, M. Ghezzo, J. Kretchmer. Characterization of phosphorus implantation in 4H-SiC. Journal of Electronic Materials 28 (1999) 167.

[33] R. Rurali, P. Godignon, J. Rebollo, E. Hernandez, P. Ordejon. First-principles study of n-type dopants and their clustering in SiC. Applied Physics Letters 82 (2003) 4298.

[34] S. Blanqué, R. Pérez, P. Godignon, N. Mestres, E. Morvan, A. Kerlain, C. Dua, C. Brylinski, M. Zielinski, J. Camassel. Room temperature implantation and activation kinetics of nitrogen and phosphorus in 4H-SiC crystals. Materials Science Forum 457 (2004) 893.

[35] X. Song, J. Biscarrat, J.F. Michaud, F. Cayrel, M. Zielinski, T. Chassagne, M. Portail, E. Collard and D. Alquier. Structural and electrical characterizations of n-type implanted layers and ohmic contacts on 3C-SiC. Nuclear Instruments and Methods in Physics Research B 269 (2011) 2020.

[36] K.V. Vassilevski, N.G. Wright, I.P. Nikitina, A.B. Horsfall, A.G. O'Neill, M.J. Uren, K.P. Hilton, A.G. Masterton, A.J. Hydes and C.M. Johnson. Protection of selectively implanted and patterned silicon carbide surfaces with graphite capping layer during post-implantation annealing. Semiconductor Science and Technology 20 (2005) 271.

[37] K.A. Jones, M.C. Wood, T.S. Zheleva, K.W. Kirchner, M.A. Derenge, A. Bolonikov, T.S. Sudarshan, R.D. Vispute, S.S. Hullavarad and S. Dhar. Comparison of graphite and BN/AlN annealing caps for ion implanted SiC. Materials Science Forum 556-557 (2007) 575.

[38] K.A. Jones, M.C. Wood, T.S. Zheleva, K.W. Kirchner, M.A. Derenge, A. Bolonikov, T.S. Sudarshan, R.D. Vispute, S.S. Hullavarad and S. Dhar. Structural and chemical comparison of graphite and BN/AlN caps used for annealing ion implanted SiC. Journal of Electronic Materials 37 (2008) 917.

[39] S.G. Sundaresan, N.A. Mahadik, S.B. Qadri, J.A. Schreifels, Y.L. Tian, Q. Zhang, E. Gomar-Nadal and M.V. Rao. Ultra-low resistivity Al^{+} implanted 4H-SiC obtained by microwave annealing and a protective graphite cap. Solid-State Electronics 52 (2008) 140.

[40] I. Sankin, J.B. Casady, J.B. Dufrene, W.A. Draper, J. Kretchmer, J. Vandersand, V. Kumar, M.S. Mazzola and S.E. Saddow, On Development of 6H-SiC LDMOS Transistors Using Silane-ambient Implant Anneal, Solid-State Electronics 45 (2001) 1653.

[41] S.E. Saddow, J.R. Williams, T.I. Smith, M.A. Capano, J.A. Cooper, M.S. Mazzola, A.J. Hsieh and J.B. Casady. High temperature implant activation in 4H and 6H-SiC in a silane ambient to reduce step bunching. Materials Science Forum 338-342 (2000) 901.

[42] S. Sze and Kwok K. Ng. Physics of Semiconductor Devices, Third Edition. John Wiley & Sons (2007).

[43] W. Shockley. Research and investigation of inverse epitaxial UHF power transistors. Report No. Al-TOR-64-207, A.F.A.L., Wr.-Patt. A. F. B., Ohio (1964).

[44] G.K. Reeves and H.B. Harrison. Obtaining the specific contact resistance from transmission line model measurements. IEEE Electron Device Letters 3 (5) (1982) 111.

[45] L.M. Porter and R.F. Davis. A critical review of ohmic and rectifying contacts for silicon carbide. Materials Science and Engineering B 34 (1995) 83.

[46] F. Roccaforte, F. La Via and V. Raineri. Ohmic contacts to SiC. International Journal of High Speed Electronics and Systems 15 (2005) 781.

[47] P. Pirouz, C.M. Chorey, J.A. Powell. Antiphase boundaries in epitaxially grown β-SiC. Applied Physics Letters 50 (1987) 221.

[48] Y. Ishida, T. Takahashi, H. Okumura, S. Yoshida. Investigation of antiphase domain annihilation mechanism in 3C-SiC on Si substrates. Journal of Applied Physics 94 (2003) 4676.

[49] K. Yagi and H. Nagasawa. Crystallinity of 3C-SiC films grown on Si substrates. Materials Science Forum 264-268 (1998) 191.

[50] E.K. Polychroniadis, D. Balloud, S. Juillaguet, G. Ferro, Y. Monteil, J. Camassel, J. Stoemenos. Comparative evaluation of free standing 3C-SiC crystals. Materials Science Forum 483-485 (2005) 229.

[51] Y. Li, L.J. Giling. A closer study on the self-annihilation of antiphase boundaries in GaAs epilayers. Journal of Crystal Growth 163 (1996) 203.

[52] X. Song, J.F. Michaud, F. Cayrel, M. Zielinski, M. Portail, T. Chassagne, E. Collard and D. Alquier. Evidence of electrical activity of extended defects in 3C-SiC grown on Si. Applied Physics Letters 96 (2010) 142104.

[53] C. Coletti, C.L. Frewin, S.E. Saddow, M. Hetzel, C. Virojanadara, U. Starke. Surface studies of hydrogen etched 3C-SiC(001) on Si(001). Applied Physics Letters 91 (2007) 061914.

[54] C. Long, S.A. Ustin, W. Ho. Structural defects in 3C-SiC grown on Si by supersonic jet epitaxy. Journal of Applied Physics 86 (1999) 2509.

[55] S Roy, M. Portail, T. Chassagne, J.M. Chauveau, P. Vennégues, M. Zielinski. Transmission electron microscopy investigations of microtwins and double positioning domains in (111) 3C-SiC in relation with the carbonization conditions. Applied Physics Letters 95 (2009) 081903.

[56] H. Nagasawa, K. Yagi, T. Kawahara. 3C-SiC hetero-epitaxial growth on undulant Si(001) substrate. Journal of Crystal Growth 237-239 (2002) 1244.

[57] K. Yagi, T. Kawahara, N. Hatta, H. Nagasawa. Switch back epitaxy as a novel technique for reducing stacking faults in 3C-SiC. Materials Science Forum 527-529 (2006) 291.

[58] J. Yun, T. Takahashi, S. Kuroda, Y. Ishida, H. Okumura. Reduction of defects propagation into 3C-SiC homoepilayers by reactive ion etching of 3C-SiC heteroepilayer substrate. Journal of Crystal Growth 308 (2007) 50.

[59] G. Ferro, Y. Monteil, H. Vincent, V. Thevenot, Min Duc Tran, F. Cauwet, J. Bouix. Atomic force microscopy growth modelling of SiC buffer layers on Si(100) and quality optimization. Journal of Applied Physics 80 (1996) 4691.

[60] L.O. Björketun, L. Hultman, I.P. Ivanov, Q. Wahab, J.E. Sundgren. Interfacial void formation during vapour phase growth of 3C-SiC on Si(001) and Si(111) substrates—Characterization by transmission electron microscopy. Journal of Crystal Growth 182 (1997) 379.

[61] C.J. Mogab, H.J. Leamy. Conversion of Si to epitaxial SiC by reaction with C_2H_2. Journal of Applied Physics 45 (1974) 1075.

[62] A Gupta, J. Sengupta, C. Jacob. An atomic force microscopy and optical microscopy study of various shaped void formation and reduction in 3C-SiC films grown on Si using chemical vapour deposition. Thin Solid Films 516 (2008) 1669.

[63] V. Cimalla, J. Pezoldt, G. Eichhorn. A growth model for the carbonization of silicon surfaces. Materials Science and Engineering B 46 (1997) 190.

[64] W. Attenberger, J. Lindner, V. Cimalla, J. Pezoldt. Structural and morphological investigations of the initial solid source molecular beam epitaxy of SiC on (111)Si. Materials Science and Engineering B 61 (1999) 544.

[65] A. Severino, G. D'Arrigo, C. Bongiorno, S. Scalese, F. La Via, G. Foti. Thin crystalline 3C-SiC layers growth through carbonization of differently oriented Si substrates. Journal of Applied Physics, 102 (2007) 023518.

[66] M. Portail, M. Zielinski, T. Chassagne, S. Roy, M. Nemoz. Comparative study of the role of the nucleation stage on the final crystalline quality of (111) and (100) silicon carbide films deposited on silicon substrates. Journal of Applied Physics 105 (2009) 083505.

[67] M. Bosi, G. Attolini, M. Negri, C. Frigeri, E. Buffagni, C. Ferrari, T. Rimoldi, L. Cristofolini, L. Aversa, R. Tatti, R. Verucchi. Optimization of a buffer layer for cubic silicon carbide growth on silicon substrates. Journal of Crystal Growth 383 (2013) 84.

[68] J.F. Michaud, S. Jiao, A.E. Bazin, M. Portail, T. Chassagne, M. Zielinski and D. Alquier. Micromachining of thin 3C-SiC films for mechanical properties investigation. Materials Research Society Symposium Proceedings 1246 (2010) 213.

[69] M. Zielinski, C. Moisson, S. Monnoye, H. Mank, T. Chassagne, S. Roy, A.E. Bazin, J.F. Michaud, M. Portail. Recent advances in surface preparation of silicon carbide and other wide band gap materials. Materials Science Forum 645-648 (2010) 753.

[70] J. Eriksson, M.H. Weng, F. Roccaforte, F. Giannazzo, S. Leone, V. Raineri. Toward an ideal Schottky barrier on 3C-SiC. Applied Physics Letters 95 (2009) 081907.

[71] Silicon Carbide (SiC) Microelectromechanical Systems (MEMS) for Harsh Environments, edited by R. Cheung, Imperial College Press (2006).

[72] M. Mehregany and C.A. Zorman. SiC MEMS: opportunities and challenges for applications in harsh environments. Thin Solid Films 355-356 (1999) 518.

[73] P.M. Sarro. Silicon carbide as a new MEMS technology. Sensors and Actuators 82 (2000) 210.

[74] P. Godignon. SiC materials and technologies for sensors development. Materials Science Forum 483-485 (2005) 1009.

[75] N.G. Wright and A.B. Horsfall. SiC sensors: a review. Journal of Physics D: Applied Physics 40 (2007) 6345.

[76] V.J. Jennings. The etching of silicon carbide. Materials Research Bulletin 4 (1969) S199.

[77] T.L. Chu and R.B. Campbell. Chemical etching of silicon carbide with hydrogen. Journal of the Electrochemical Society 112 (1965) 955.

[78] D. Zhuang and J.H. Edgar. Wet etching of GaN, AlN, and SiC: a review. Materials Science and Engineering R 48 (2005) 1.

[79] C. Cardinaud, M.C. Peignon, P.Y. Tessier. Plasma etching: principles, mechanisms, application to micro- and nano-technologies. Applied Surface Science 164 (2000) 72.

[80] A. Henry, E. Janzen, E. Mastropaolo and R. Cheung. Single crystal and polycrystalline 3C-SiC for MEMS applications. Materials Science Forum 615-617 (2009) 625.

[81] E. Mastropaolo, R. Cheung, A. Henry and E. Janzén. Fabrication of beam resonators from hot-wall chemical vapour deposited SiC. Microelectronic Engineering 86 (2009) 1194.

[82] M. Lazar, H. Vang, P. Brosselard, C. Raynaud, P. Cremillieu, J.-L. Leclercq, A. Descamps, S. Scharnholz and D. Planson. Deep SiC etching with RIE. Superlattices and Microstructures 40 (2006) 388.

[83] M. Placidi, P. Godignon, N. Mestres, G. Abadal, G. Ferro, A. Leycuras and T. Chassagne. Fabrication of monocrystalline 3C-SiC resonators for MHz frequency sensors applications. Sensors and Actuators B 133 (2008) 276.

[84] M. Mehregany, C.A. Zorman, N. Rajan and C.H. Wu. Silicon carbide MEMS for harsh environments. Proceedings of the IEEE 86(8) (1998) 1594.

[85] M. Lazar, F. Enoch, F. Laariedh, D. Planson and P. Brosselard. Influence of the masking material and geometry on the 4H-SiC RIE etched surface state. Materials Science Forum 679-680 (2011) 477.

[86] P.H. Yih, V. Saxena and A.J. Steckl. A review of SiC reactive ion etching in fluorinated plasmas. Physica Status Solidi (b) 202 (1997) 605.

[87] L. Jiang and R. Cheung. Impact of Ar addition to inductively coupled plasma etching of SiC in SF_6/O_2. Microelectronic Engineering 73-74 (2004) 306.

[88] W.S. Pan and A.J. Steckl, Reactive ion etching of SiC thin films by mixtures of fluorinated gases and oxygen. Journal of the Electrochemical Society 137 (1990) 212.

[89] J.H. Xia, Rusli, S.F. Choy, R. Gopalakrishan, C.C. Tin, S.F. Yoon and J. Ahn. CHF_3-O_2 reactive ion etching of 4H-SiC and the role of oxygen. Microelectronic Engineering 83 (2006) 381.

[90] L. Jiang, R. Cheung, R. Brown and A. Mount. Inductively coupled plasma etching of SiC in SF_6/O_2 and etch-induced surface chemical bonding modifications. Journal of Applied Physics 93 (2003) 1376.

[91] G.M. Beheim and L.J. Evans. Control of trenching and surface roughness in deep reactive ion etched 4H and 6H SiC. Materials Research Society Symposium Proceedings 911 (2006) B10-15.

[92] D. Ruixie, Y. Yintang and H. Ru. Microtrenching effect of SiC ICP etching in SF_6/O_2 plasma. Journal of Semiconductors 30 (2009) 16001.

[93] H. Ru, Y. Yin-Tang and F. Xiao-Ya. Microtrenching geometry of 6H-SiC plasma etching. Vacuum 84 (2010) 400.

[94] W. Chang and C. Zorman. Determination of Young's moduli of 3C (110) single-crystal and (111) polycrystalline silicon carbide from operating frequencies. Journal of Materials Science 43 (2008) 4512.

[95] R. Boubekri, E. Cambril, L. Couraud, L. Bernardi, A. Madouri, M. Portail, T. Chassagne, C. Moisson, M. Zielinski, S. Jiao, J.-F. Michaud, D. Alquier, J. Bouloc, L. Nony, F. Bocquet, C. Loppacher, D. Martrou and S. Gauthier. Electrothermally driven high-frequency piezoresistive SiC cantilevers for dynamic atomic force microscopy. Journal of Applied Physics 116 (2014) 054304.

[96] M.B.J. Wijesundara and R. Azevedo. Silicon carbide microsystems for harsh environments. MEMS Reference Shelf 22. Springer (2011).

[97] R. Anzalone, C. Locke, A. Severino, D. Rodilosso, C. Tringali, G. Foti, S.E. Saddow, F. La Via and G. D'Arrigo. Residual stress measurement on hetero-epitaxial 3C-SiC films. Materials Science Forum 615-617 (2009) 629.

[98] R. Anzalone, M. Camarda, G. D'Arrigo, C. Locke, A. Canino, N. Piluso, A. Severino, A. La Magna, S.E. Saddow and F. La Via. Advanced stress analysis by micro-struc-

tures realization on high quality hetero-epitaxial 3C-SiC for MEMS application. Materials Science Forum 679-680 (2011) 133.

[99] N. Moronuki, M. Kojima and A. Kakuta. Single-crystal SiC thin-film produced by epitaxial growth and its application to micro-mechanical devices. Thin Solid Films 516 (2008) 5344.

[100] S. Sundararajan and B. Bhushan. Micro/nanotribological studies of polysilicon and SiC films for MEMS applications. Wear 217 (1998) 251.

[101] B. Pecholt and P. Molian. Nanoindentation of laser micromachined 3C-SiC thin film micro-cantilevers. Materials and Design 32 (2011) 3414.

[102] C. Locke, G. Kravchenko, P. Waters, J.D. Reddy, K. Du, A.A. Volinsky, C.L. Frewin and S.E. Saddow, 3C-SiC Films on Si for MEMS applications: Mechanical properties. Materials Science Forum 615-617 (2009) 633.

[103] W.C. Oliver and G.M. Pharr. Measurement of hardness and elastic modulus by instrumented indentation: Advances in understanding and refinements to methodology. Journal of Materials Research 19 (2004) 3.

[104] K.M. Jackson, J. Dunning, C.A. Zorman, M. Mehregany and W.N. Sharpe Jr. Mechanical properties of epitaxial 3C silicon carbide thin films. Journal of Micromechanical Systems 14(4) (2005) 664.

[105] Robert D. Blevins, in: Formulas for Natural Frequency and Mode Shape. Krieger Publishing Company (1979).

[106] M. Zielinski, J.F. Michaud, S. Jiao, T. Chassagne, A.E. Bazin, A. Michon, M. Portail and D. Alquier. Experimental observation and analytical model of the stress gradient inversion in 3C-SiC layers on silicon. Journal of Applied Physics 111 (2012) 53507.

[107] D. Herman, M. Gaitan and D. DeVoe. MEMS test structures for mechanical characterization of VLSI thin films, in: Proceedings of the Annual Meeting of the Society for Experimental Mechanics, Portland (2001).

[108] L. Tong, M. Mehregany and L.G. Matus. Mechanical properties of 3C silicon carbide. Applied Physics Letters 60 (1992) 2992.

[109] R. Anzalone, M. Camarda, A. Canino, N. Piluso, F. La Via and G. D'Arrigo. Defect influence on heteroepitaxial 3C-SiC Young's modulus. Electrochemical and Solid-State Letters 14(4) (2011) H161.

[110] R. Anzalone, N. Piluso, A. Marino, A. Sciuto and G. D'Arrigo. Very low dose ion-implantation effect on heteroepitaxial 3C-SiC mechanical properties. Physica Status Solidi A 209 (2012) 2235.

[111] J.F. Michaud, M. Portail, T. Chassagne, M. Zielinski and D. Alquier. Original 3C-SiC micro-structure on a 3C-SiC pseudo-substrate. Microelectronic Engineering 105 (2013) 65.

[112] R. Anzalone, M. Camarda, A. Severino, N. Piluso and F. La Via. Curvature evaluation of Si/3C-SiC/Si hetero-structure grown by chemical vapor deposition. Materials Science Forum 778-780 (2014) 255.

Chapter 3

Impact of Dielectric Formation and Processing Techniques on the Operation of 4H-SiC MOSFETs

Lucy Martin, Hua-Khee Chan, Ming-Hung Weng and Alton Horsfall

Additional information is available at the end of the chapter

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Abstract

The mobility of carriers in the channel of silicon carbide is significantly lower than in equivalent silicon devices. This results in a significant increase in on-state resistance in comparison to theoretical predictions and is hindering the uptake of silicon carbide technology in commercial circuits. The density of interface traps at the interface between silicon carbide and the dielectric film is higher and this is often considered to be the primary reason for the low mobility. In this work, we show that the mobility is dominated by the surface roughness of the silicon carbide, especially when the transistor is operating in the strong inversion regime, by careful examination of the characteristics of lateral transistors designed to form complimentary MOS functions.

Keywords: Surface roughness, mobility, complementary metal–oxide semiconductor, flat band, 1/*f* noise

1. Introduction

The main objective of this study is to aid in the advancement and commercialisation of a CMOS process to enable the production of signal-level 4H-SiC MOSFETs for high-temperature digital and analog applications. Therefore, we report on the electrical characterisation and performance of 4H-SiC n- and p-channel MOSFETs that have been fabricated using different, commercially relevant dielectric process treatments. The samples labelled as HV06, CR25 and CR27 were fabricated using the process conditions detailed in Table 1. The aim of this work is to establish which oxidation process technique provides the best characteristics for a complementary CMOS process.

2. Overview of the theoretical MOSFET

The metal–oxide semiconductor field-effect transistor (MOSFET) is one of the most important devices for integrated circuits in microprocessors and semiconductor memories, as well as being a very important power device. Due to this, it is becoming increasingly important to understand and advance the characteristics of 4H-SiC MOSFETs for both power device applications and signal-level devices. MOSFETs have several attractive features, which make them ideal for use in analog switching, high-input-impedance amplifiers, microwave amplifiers and digital integrated circuits.

The features include the following:

1. Higher input impedance than bipolar transistors, which allows the input impedance to be more readily matched to the standard microwave system.
2. Negative temperature coefficient at high current levels – more uniform temperature distribution over the device area and prevents the FET from thermal runaway or second breakdown that can occur in the bipolar transistors.
3. The device is thermally stable, even when the active area is large or when many devices are connected in parallel.
4. FETs do not suffer from minority carrier storage as there is no forward-biased p–n junction and consequently have higher large-signal switching speeds.

The MOSFET is usually referred to as a majority carrier or unipolar device because the current in a MOSFET is predominantly transported by carriers of one polarity. As shown in Figure 1, a MOSFET is a four-terminal device made up of a source, drain, gate and substrate or body. Figure 1 shows an n-channel MOSFET, which is made up of a p-type substrate into which two n+ regions are formed, the source and drain and a gate electrode which is usually made of doped polysilicon or metal and is separated from the substrate by a thin insulating film known as the gate dielectric.

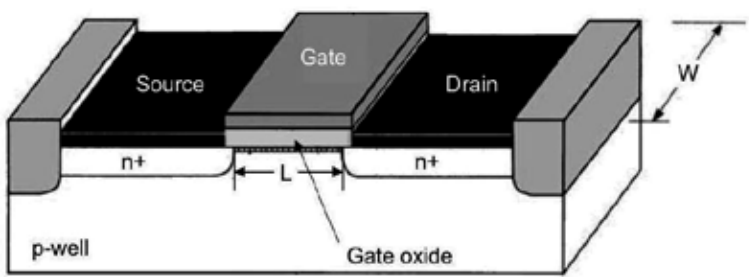

Figure 1. Schematic representation of a simple n-MOSFET

When a low voltage is applied to the gate electrode that is insufficient to form an inversion layer at the surface, there is no conduction in the channel, which corresponds to two p–n

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junctions situated back to back. This results in a high resistance and electrical isolation between the source and drain contacts. If a sufficiently large bias is applied to the gate electrode, a surface inversion layer will be formed between the source and drain, which will form a conductive channel through which a current can flow. The conductance of the channel can be modulated by varying the voltage applied to the gate electrode. Conduction in n-channel devices is based on the flow of electrons, and the channel becomes more conductive with increasing positive bias on the gate, whilst p-channel devices are controlled by hole conduction and are more conductive with a more negative gate bias. Enhancement-mode (or normally off) devices have a low transconductance at zero gate bias and require an applied gate voltage to form a conductive channel. Their counterpart, depletion-mode (or normally on) devices, are conductive when a zero bias is applied to the gate of the device, and a gate voltage must be applied to turn the channel off. Devices can either have a surface inversion channel or a buried channel. Buried channel devices are based on bulk conduction and are, therefore, free of surface effects such as scattering and surface defects resulting in better carrier mobility. The physical distance between the gate and the channel is larger and also dependent on gate bias, leading to lower and variable transconductance.

In a long-channel MOSFET, at low drain voltage and for a given gate voltage, the drain current is given by

$$I_{DS} = \frac{W}{L} q \mu_{inv} \left| Q_{inv} \right| V_{DS} \tag{1}$$

where W and L are the gate width and length, q is the electron charge, μ_{inv} the average mobility of the carriers in the inversion layer, V_{DS} the drain voltage and Q_{inv} the average charge in the inversion layer.

The field effect mobility μ_{FE} is defined as

$$\mu_{FE} = \frac{L}{WC_i V_{DS}} \left(\frac{\delta I_{DS}}{\delta V_{GS}} \right) \tag{2}$$

where C_i is the insulator capacitance per unit area and V_{GS} is the gate voltage.

In 4H-SiC MOSFETs, the values of the field effect mobility extracted from the V_{GS} –I_{DS} characteristics will not correspond to the true inversion mobility due to the large density of interface charge. A knowledge of Q_{inv} as a function of V_{GS}, which can be extracted from the measured V_{GS} –I_{DS} characteristics, can allow the immobile interface charge to be calculated, which includes contributions from both Q_f and Q_{it}. A change in gate voltage δV_{GS} results in a change in Q_{it} and a change in δQ_{inv} in the inversion layer as the surface Fermi level moves away from the intrinsic level towards the conduction band edge [1]. This can be summarised through the use of equation 3:

$$\delta V_{GS} = -\frac{q}{C_i}\left(\delta Q_{it} + \delta Q_{inv}\right) \tag{3}$$

By combining equations 2 and 3, an expression that relates the experimental field effect mobility and the inversion carrier mobility can be derived [2]:

$$\mu_{FE} = \mu_{FE}\frac{\left[1 + \frac{Q_{inv}}{\mu_{inv}}\frac{\delta\mu_{inv}}{\delta Q_{inv}}\right]}{1 + \frac{\delta Q_{it}}{\delta Q_{inv}}} \tag{4}$$

3. Carrier mobility and scattering mechanisms in 4H-SiC

The conductivity (σ) of a semiconductor can be varied by the introduction of n- or p-type dopants and can be represented by equation 5:

$$\sigma = qn\mu \tag{5}$$

where μ is the carrier mobility, q the charge of an electron and n the number of carriers in the material.

The carrier mobility is principally how quickly an electron or hole can move through a semiconductor under the influence of an applied electric field and is affected by the frequency of collisions with lattice defects and impurities. The probability of scattering is inversely proportional to the carrier mean free time and the mobility. A carrier moving through a semiconductor crystal can be scattered by a vibration of the lattice, which increases for high temperatures when the thermal agitation of the lattice becomes higher. Scattering can also be due to lattice defects (e.g. ionised impurities) and is prominent at low temperatures since atoms are less thermally agitated and the thermal motion of the carriers is also slower. Higher scattering arises because a slow moving carrier is likely to be scattered more significantly by an interaction with a charged ion than a carrier with a larger velocity. If the carrier mobility in a material is reduced, the conductivity of the material will reduce and hence the resistivity will increase and channel current will reduce. As it is widely known that 4H-SiC MOSFETs exhibit low channel mobility and hence low current, it is of great importance to analyse the mechanisms that are contributing to the reduced channel mobility.

As previously reported [3-5], the total inversion carrier mobility in 4H-SiC MOSFETs can be described by the sum of four mobility terms using Matthiessen's rule which is often incorporated in simulation tools, such as the Synopsys suite by means of the Lombardi mobility model [6,7]:

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$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \tag{6}$$

As previously stated, the measured field effect mobility will not correspond to the true inversion mobility due to the presence of interface trapped charges. However, the main interest in silicon carbide technology is in the development of devices with higher functionality, and so the experimental device characteristics of the modelled mobility mechanisms will be equated to the field effect mobility using equation 7. Therefore, each of the scattering mechanisms considered here (μ_{AC}, μ_{SR} and μ_C) will result in a mobility which is lower than the value of each that would combine to form the true inversion mobility:

$$\mu_{FE} \propto \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right] \tag{7}$$

whereμ_B is the carrier mobility in the bulk semiconductor, μ_{AC} the acoustic phonon mobility, μ_{SR} the surface roughness mobility and μ_C the mobility related to carrier scattering at trapped charge at the silicon carbide–oxide interface.

At low electric fields, the carrier mobility in a semiconductor is a function of the temperature and the total doping concentration, which is referred to as the bulk or low-field mobility, μ_B. To represent this phenomena, an empirical model was developed by Caughey and Thomas which is described through the use of equation 8 [8, 9]:

$$\mu_B = \frac{\mu_{max}\left(\frac{300}{T}\right)^{\alpha} - \mu_{min}}{1 + \left(\frac{D}{N_{ref}}\right)^{\beta}} \tag{8}$$

where N_{ref}, μ_{min}, μ_{max}, α and β are fitting parameters, T the temperature and D the total doping concentration.

The second term in equation 7 is the acoustic phonon mobility, μ_{AC}. Both surface phonon and bulk phonon scattering have been modelled previously [10-12]. Each shows a temperature dependence and both surface and bulk phonon scatterings increase with an increase in temperature. Previous research has indicated that phonon scattering has a strong effect on surface mobility in SiC MOSFETs at high gate biases and high temperatures [13], and Potbhare et al. showed that surface phonon mobility does not play an important role at temperatures below 200°C [14]. The carrier mobility related to phonon scattering can be determined using equation 9:

$$\mu_{AC} = \frac{B}{E} + \frac{CN_A^{\alpha 1}}{TE^{\frac{1}{3}}} \tag{9}$$

where B and C are fitting parameters, E the perpendicular electric field, N_A the total doping concentration, T the temperature and $\alpha 1$ a factor that indicates the dependency of the mobility term μ_{AC} on the impurity concentration.

Surface roughness scattering is due to the scattering of mobile carriers by imperfections in the SiC surface and is known to cause severe degradation of the surface mobility at high electric fields [8, 15, 16]. The carrier mobility determined from surface roughness scattering may be calculated using equation 10:

$$\mu_{SR} = \frac{D_1}{E^{\gamma 1}} \tag{10}$$

where E is the perpendicular electric field and D_1 and $\gamma 1$ are fitting parameters.

Coulomb scattering is a result of carrier interactions with ionised impurities, which are most commonly a product of interface traps at the semiconductor–dielectric interface. Coulomb scattering is believed to dominate carrier mobility at low electric fields and is calculated using equation 11 [4]:

$$\mu_C = NT^{\alpha 2} \frac{Q_{inv}^{\beta 2}}{Q_{trap}} \tag{11}$$

where Q_{inv} is the inversion charge per unit area, $\beta 2$ a fitting parameter, Q_{trap} the trapped charge per unit area at the silicon carbide–oxide interface and T the temperature. For the analysis reported here, the exact values of Q_{trap} and $\beta 2$ were unknown, and so a simplified formula was derived that has the same functional form but could be fitted to the measure MOSFET field effect mobility characteristics [17], which is given in equation 12:

$$\mu_C = \left(E - \lambda\right)^{\Phi} \tag{12}$$

where E is the perpendicular electric field, λ the electric field offset at which the mobility becomes nonzero and Φ a fitting parameter which describes the gradient of the increasing mobility.

Figure 2 shows a schematic plot of the contributions of the three scattering mechanisms that have been discussed here: μ_{AC}, μ_{SR} and μ_C. For MOSFETs fabricated using 4H-SiC, the bulk mobility contribution to equation 7 term (μ_B) is far higher than the other scattering mechanisms,

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resulting in a negligible impact on the field effect mobility characteristics of the devices. For this reason, $\mu_B$is omitted from further analysis and is not included in Figure 2. As shown in Figure 2, Coulomb scattering dominates the field effect mobility under low electric fields, with surface roughness scattering dominating under high electric fields as carriers are strongly attracted to the semiconductor surface under high applied biases and therefore have more interactions with the surface.

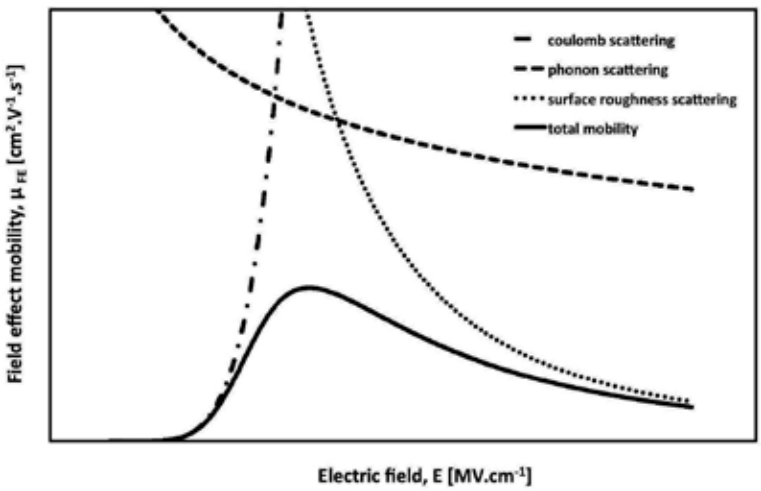

Figure 2. Schematic representation of the field effect mobility in an n-type MOSFET channel

4. Current status of the technology

The current status of MOSFET technology is still plagued by low channel mobility and oxide reliability issues due to issues with the 4H-SiC/dielectric interface, which is believed to be due to an unoptimised dielectric formation and post-oxidation anneal procedure. There has been a significant amount of research into the effects of varying the post-oxidation anneal conditions, including the use of hydrogen, oxygen, nitrogen and phosphorus anneal environments, which have previously been used to passivate interface traps in silicon technology. This has led to advances in the capabilities of the technology, and MOSFET field effect mobilities of over $100\ cm^2 \cdot V^{-1} \cdot s^{-1}$ have been reported in n-channel MOSFETs formed in Al-implanted regions, after performing a post deposition anneal in $POCl_3$ [18].

5. Fabrication techniques and process variations

Complementary metal–oxide semiconductor (CMOS) devices fabricated using the three gate dielectrics summarised in Table 1 were examined using electrical characterisation techniques.

The remaining process steps utilised in their fabrication were identical. The main aim of this investigation is to highlight the benefits and potential issues of each processing technique on the electrical performance of the devices under test.

The CMOS test structures reported here were fabricated on a 100 mm, Si face, 4° off axis, 4H SiC n^+ wafer with a doped epitaxial layer. N- and p-type regions and the source and drain regions were formed by ion implantation. The implants were annealed at high temperature with the surface protected by a carbon cap. A thick field oxide and a thin gate dielectric region were then formed and doped polysilicon gate electrodes. Nickel-based contacts were then formed on the doped regions and a refractory metal interconnect was deposited and patterned. Next, a thin nickel top layer was applied to protect the pads from oxidation during probe testing at elevated temperatures. Finally, an oxide layer was deposited for final passivation and scratch protection, and openings were made for bond pads. A schematic of the device cross section is shown in Figure 3.

Sample	Initial process	Dielectric	Post-oxidation anneal
HV06		Dry oxidation at 1200 C	O_2 950 C N_2 1200 C
CR25	Dry oxidation at 1200C with phosphorous anneal and strip	Deposited undoped oxide	H_2O 875 C N_2 1100 C
CR27		Dry oxidation stub oxide Deposited phosphorous doped	Steam 950 C

Table 1. Summary of the dielectric process conditions

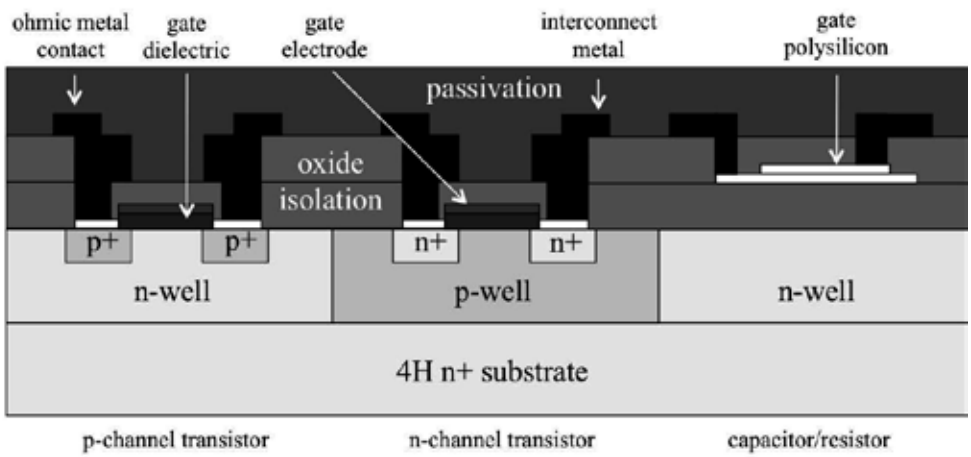

Figure 3. Schematic cross section of the completed transistor structures

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6. Temperature-dependent electrical characteristics of 4H-SiC MOSFETs

In the following subsections, the current-voltage characteristics are extracted and explored for the three different dielectric samples (HV06, CR25 and CR27) on both n-channel and p-channel 4H-SiC MOSFETs. This involved the extraction of the field effect mobility μ_{FE}, subthreshold slope (SS) and threshold voltage V_{TH} from the measured V_{GS} –I_{DS} characteristics across a temperature range of 298 K to 498 K with 50 K increments in order to understand the effect of the dielectric processing treatment on the MOSFET characteristics. The extracted field effect mobility for each of the samples is also fitted to the theoretical model for mobility using equation 6 in order to predict the mobility-limiting mechanisms for each of the MOSFETs and the impact of temperature on the mobility-limiting mechanisms involved. All of the electrical characteristics discussed in this chapter were extracted using a Keithley 4200 SCS Parameter Analyser.

7. Temperature-dependent electrical characteristics of n-channel 4H-SiC MOSFETs

The data shown in Figures 4, 5 and 6 show the V_{GS} –I_{DS} and V_{GS} -$log(I_{DS})$ characteristics for a typical 400x1.5 μm n-channel MOSFET for HV06, CR25 and CR27, respectively, measured from 298 K to 498 K. The drain bias in each of the measurements was 500 mV. Each of the samples shows a similar trend and there is an increase in drain current, a reduction in threshold voltage and a change in the subthreshold slope with increasing temperature. The data for HV06 in Figure 4 shows a much higher off-state leakage current, with subthreshold drain currents consistently around 0.1 nA, whereas the data for both CR25 (Figure 5) and CR27 (Figure 6) show reverse leakage current of approximately 1 pA. The off-state conduction could be due to counter doping in the channel region, which could be a product of the threshold-adjust implant [19]. This counter doping could have also been increased as an unwanted effect during the 1200 C to the N_2O post-oxidation anneal that was performed on the dielectric as described in Table 1.

The increase in current with temperature observed in Figures 4.a, 5.a and 6.a for the three samples is due to the decrease of occupied interface traps with an increasing temperature, which is an agreement with the density of interface traps data extracted from capacitor test structures fabricated monolithically with the MOSFETs. As the density of interface traps decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the channel. This finding also supports previous work conducted in the field [14].

The observed reduction in threshold voltage with temperature is also evident for each of the transistors across the temperature range and values extracted using linear interpolation of the I_{DS} –V_{GS} characteristics are summarised in Figure 7. The threshold voltage can be calculated using equation 13:

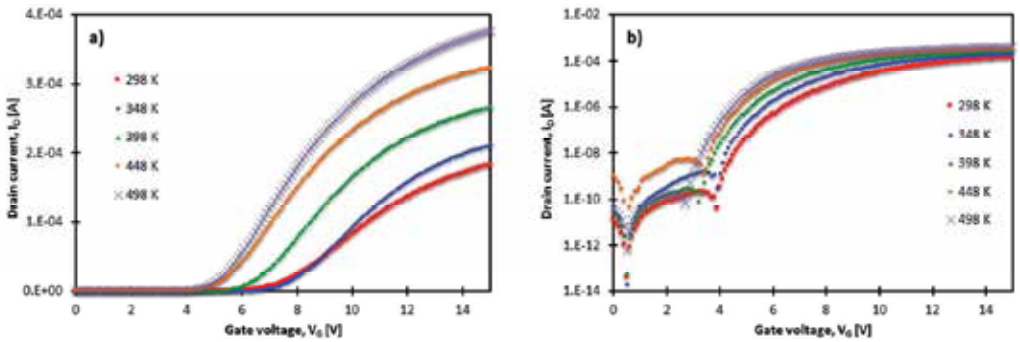

Figure 4. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process HV06

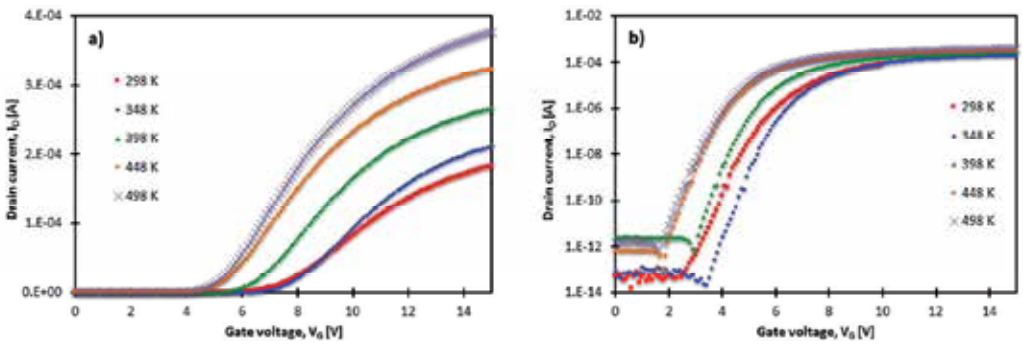

Figure 5. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process CR25

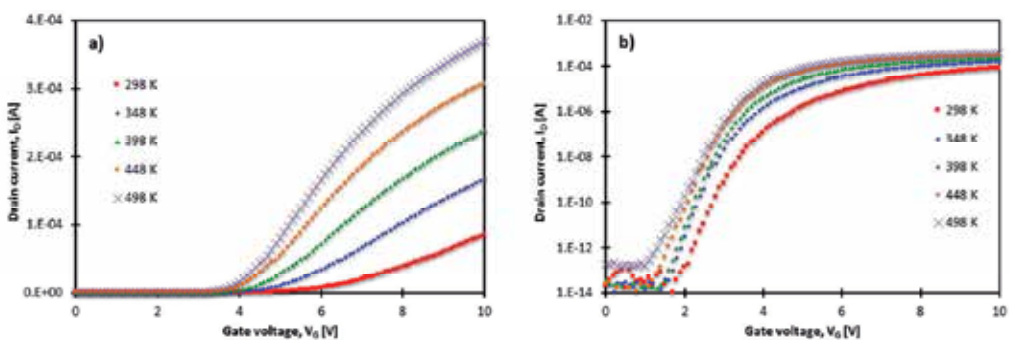

Figure 6. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 400x1.5 μm n-channel MOSFET as a function of temperature for dielectric process CR27

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$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{2\varepsilon_o \varepsilon_s q N_A 2\phi_B}}{C_i} \tag{13}$$

The observed shift in threshold voltage with temperature is due to the reduction in the surface band bending required for inversion, which is due to the increase in intrinsic carrier concentration and the decrease in band gap energy with an increase in temperature as described previously [20].

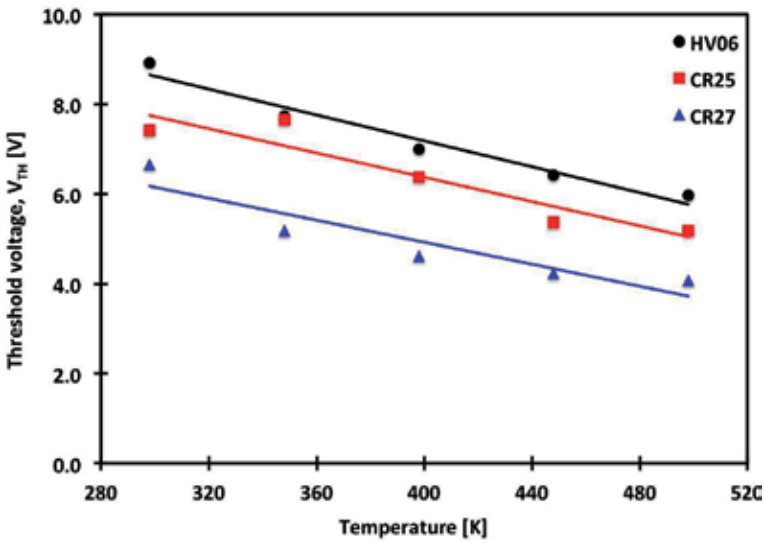

Figure 7. Variation of MOSFET threshold voltage with temperature

However, a change at the interface and within the depletion layer can also act to modify the gate voltage as V_{FB} is dependent on the amount of charge trapped at the silicon carbide–oxide interface, as shown by equation 14:

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{it}}{C_i} \tag{14}$$

where ϕ_{ms} is the metal–semiconductor work function difference.

The data in Figure 8 shows the variation in subthreshold slope (*SS*) as a function of temperature for each of the dielectrics studies. As shown by the data, both HV06 and CR27 show an increase in *SS* with temperature, whereas CR25 shows a decrease in *SS*. An increase in the subthreshold slope with increasing temperature is expected, as *SS* is proportional to kT/q. The decrease of *SS* with temperature that is witnessed for CR25 suggests that there is a change in the interface

trapped charge at the semiconductor dielectric interface as subthreshold slope is also dependent on the interface trap capacitance (C_{it}) as detailed in equation 15:

$$SS = ln(10)\left(\frac{kT}{q}\right)\left(\frac{C_i + C_D + C_{it}}{C_i}\right) \tag{15}$$

where C_D is equal to the capacitance of the depletion region in the semiconductor formed under the oxide layer [21].

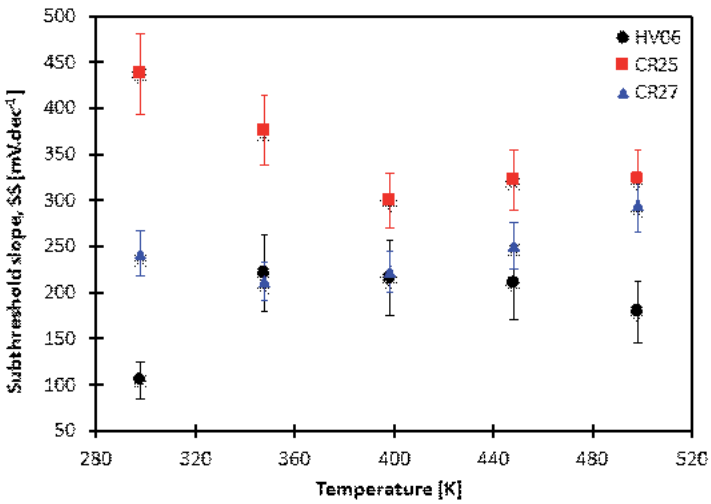

Figure 8. Variation of extracted subthreshold slope with temperature, for 400x1.5 μm n-channel MOSFETs

This observed in subthreshold slope with temperature is in agreement with the change in interface trap density with temperature that was witnessed in capacitor test structures for both the CR25 n-type and p-type MIS capacitors that were analysed using Terman analysis. This change is most likely due to the change in D_{it} with temperature, which was observed at both the conduction band and valence band edges in the semiconductor for both the n-type and p-type CR25 MIS capacitors, respectively. The data in Figure 9 shows a plot of D_{it} as a function of temperature as extracted from the subthreshold slope of each of the MOSFET devices using equation 15. As can be observed from the data, the change in D_{it} for CR25 is significantly higher than that observed in either HV06 or CR27, decreasing from 3×10^{12} to 1.5×10^{12} cm^{-2} eV^{-1} between 298 and 498 K.

The data in Figures 10(a), 11(a) and 12(a) show the variation in field effect mobility with electric field (μ_{FE} -*E*) for a 400×1.5μm n-channel MOSFET measured between 298 and 498 K taken from samples HV06, CR25 and CR27, respectively. The field effect mobility was extracted from the V_{GS} –I_{DS} data sets shown in Figures 4(a), 5(a) and 6(a) by means of equation 2. All data sets exhibit a similar trend, with increasing maximum field effect mobility with increasing

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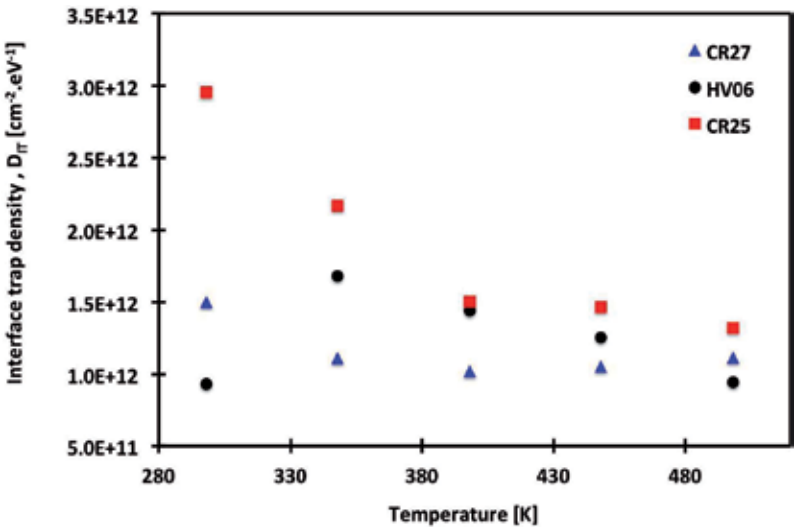

Figure 9. Variation of extracted interface trap density (D_{it}) from the subthreshold slope of 400x1.5 μm n-channel MOSFETs

temperature. The data in Figure 12(a) for sample CR27 shows the highest field effect mobility across the temperature range out of the three samples as supported by the data in Figure 16, which shows the peak field effect mobility of each device against temperature.

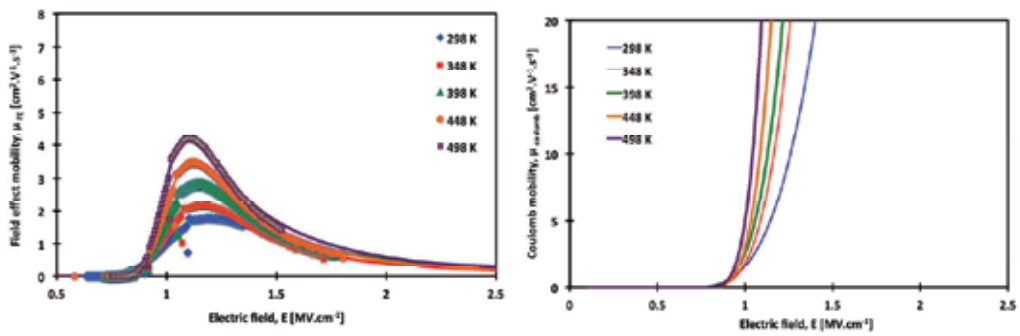

Figure 10. (a) μ_{FE} -E and (b)μ_C-E characteristics of 400x1.5 μm HV06 n-channel MOSFET at different temperatures

Figures 10(b),11(b) and 12(b) show the Coulomb mobility values that were fitted to the measured characteristics using equation 11. As shown by the data, all of the devices show an increase in Coulomb mobility with increasing temperature, which suggests that the effect of Coulomb scattering reduces with an increase in temperature. The data sets also show that the electric field at which the mobility increases from zero (the λ parameter in equation 12) does not show a significant variation with temperature; however, the Φ term used to describe the change in mobility with electric field does, especially for the HV06 data.

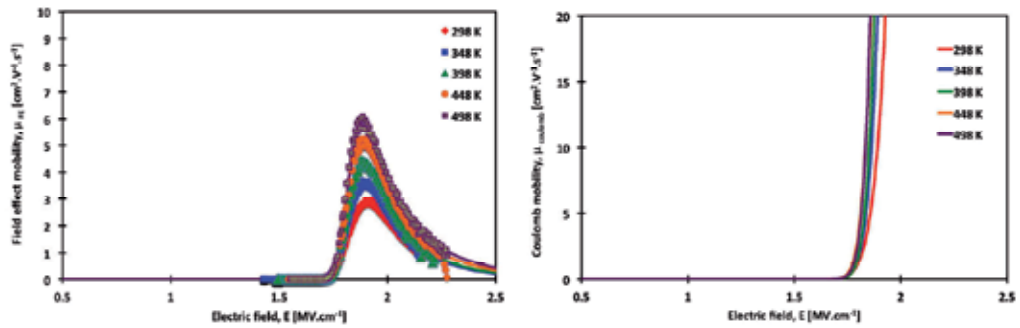

Figure 11. (a) μ_{FE} -E and (b) μ_C -E characteristics of 400x1.5 µm CR25 n-channel MOSFET at different temperatures

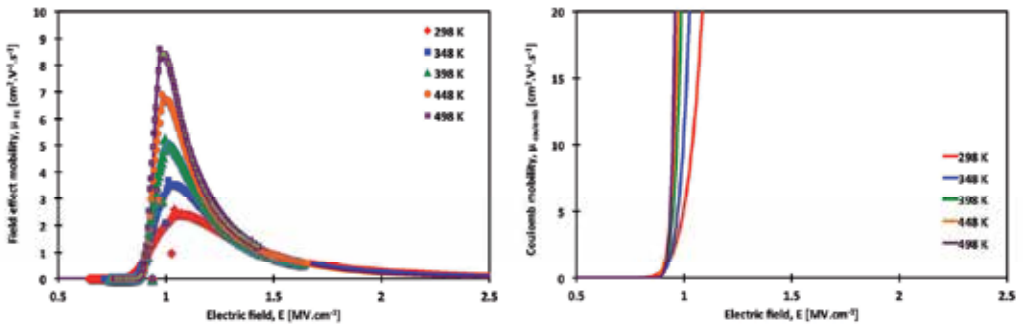

Figure 12. (a) μ_{FE} -E and (b)μ_C-E characteristics of 400x1.5 µm CR27 n-channel MOSFET at different temperatures

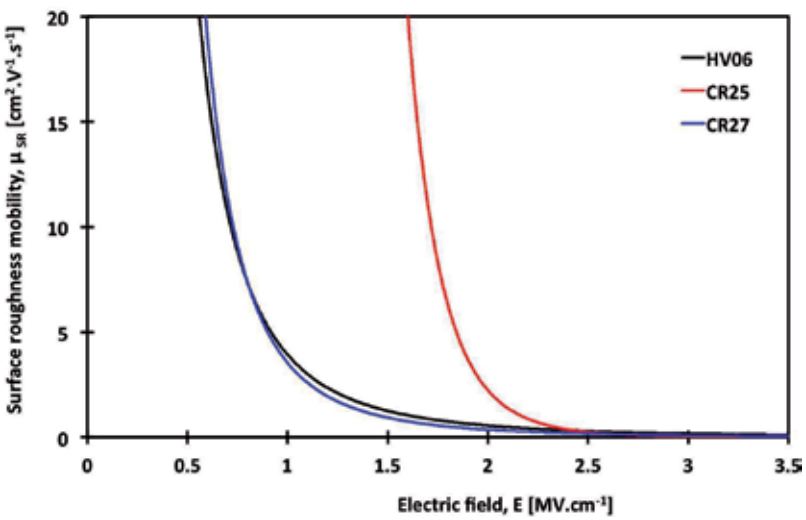

Figure 13. Surface roughness mobility (μ_{SR}) as a function of electric field for 400×1.5 µm n-channel MOSFETs at 298 K

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At high electric fields, the extracted values of μ_{FE} for each of the devices is severely limited by surface roughness scattering as shown by the data in Figures 10(a), 11(a) and 12(a). The data in Figure 13 shows the extracted μ_{SR} as a function of electric field for each of the samples at 298 K. This clearly identifies that the observed surface roughness mobility varies dependent on the dielectric under investigation. HV06 and CR27 show the lowest surface roughness mobility, which suggests that surface roughness scattering is higher within those devices. CR25 shows the highest surface roughness mobility, which suggests that the process techniques used in the fabrication of this sample produce the highest quality dielectric-semiconductor interface out of the 3 samples investigated. The data in Figures 14(a), 14(b) and 14(c) show the values of μ_{SR} fitted to each of the extracted MOSFET μ_{FE} characteristics between 298 and 498 K. The negligible temperature dependence observed in the high field regime for all three of the devices supports previously reported observations on 4H-SiC MOSFETs and shows that the experimental μ_{SR} has the same functional form as equation 10.

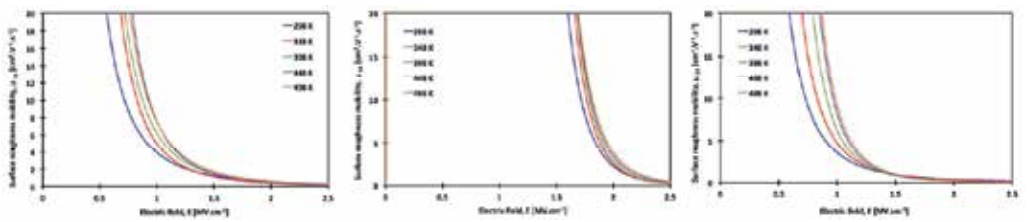

Figure 14. μ_{SR} -E characteristics of a 400×1.5 μm n-channel MOSFET from (a) HV06, (b) CR25 and (c) CR27 samples

The data shown in Figure 15 shows the theoretical acoustic phonon mobility (μ_{AC}) fitted to each sample using equation 9. The values of the fitting parameters were identical for each of the samples studied, for both n-channel and p-channel devices, and were based on values reported in the literature [5, 8]. The value of B is 1.0×10^6 cm s^{-1}, C is 3.23×10^6 K cm s^{-1} and α is 0.0284. As shown by the data in Figure 15, the modelled acoustic phonon mobility is consistently above 150 cm^2 V^{-1} s^{-1} across the entire investigated electric field and temperature range. As this is significantly higher than both μ_{SR} and μ_C, it has a negligible effect on the experimentally measured field effect mobility in each of the devices. The experimentally determined characteristics are consistently dominated at low and high electric fields by Coulomb and surface roughness scattering, respectively, as shown by the data in Figures 10(a), 11(a), 12(a) and 14.

The data in Figure 16 shows the variation in the peak field effect mobility with temperature for the three dielectrics studies. It is apparent that sample HV06 consistently shows the lowest channel mobility, whilst CR27 shows the most significant variation with temperature, giving the highest mobility at temperatures above 350 K. The main limiting factor that is witnessed across all of the samples is that of severely low surface roughness mobility, which acts to dominate the device mobility characteristics from electric fields above 1 MV cm^{-1}. The extracted surface roughness mobility reported here for all three dielectric processes is approximately an order of magnitude lower than other 4H-SiC MOSFETs that have previously been reported,

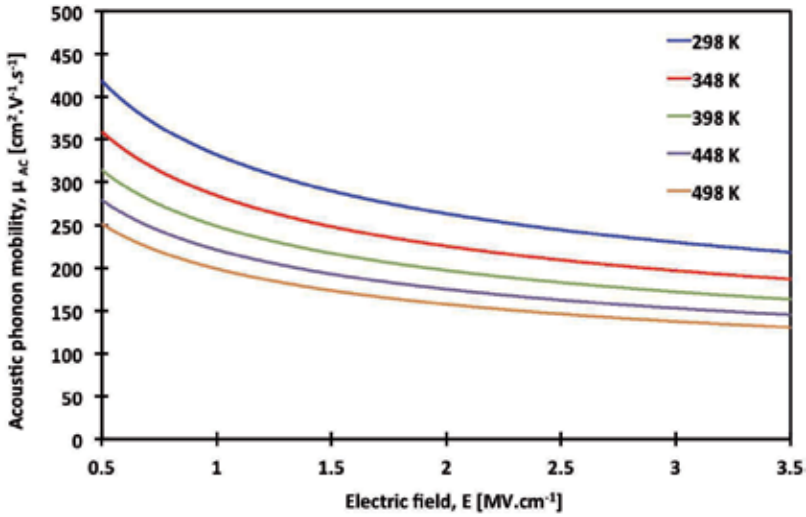

Figure 15. Predicted μ_{AC} -E characteristics of a 400×1.5 μm n-channel MOSFET

which showed field effect mobility of consistently over 20 cm^2 V^{-1} s^{-1} at high electric fields [8, 22-25].

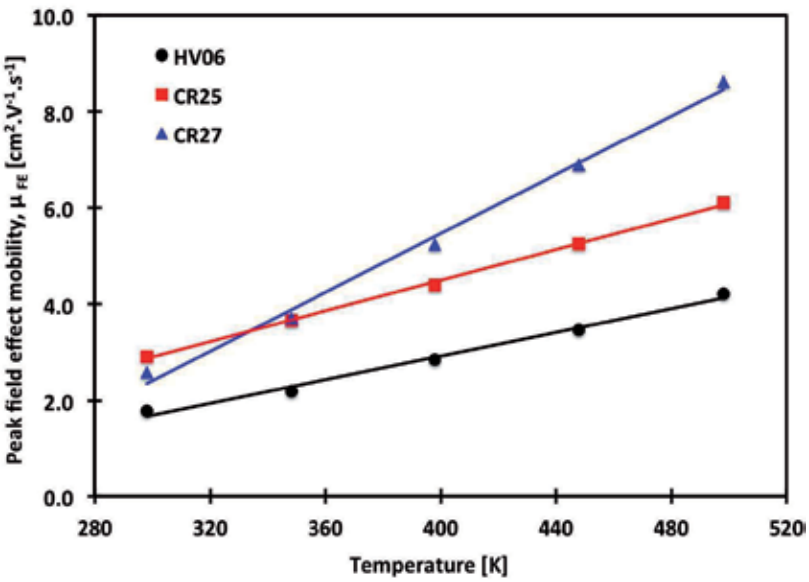

Figure 16. Variation of peak field effect mobility (μ_{FE}) with temperature for a 400×1.5 μm n-channel MOSFET

The data in Table 2 shows the fitting parameters used to generate the mobility plots for the n-channel FETs reported here.

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HV06	Acoustic phonon		Surface roughness		Coulomb
Temp	B	C	D1	γ1	θ
298	1×10^{7}	3.2×10^{6}	3.0×10^{17}	2.81	3.20
348	1×10^{7}	3.2×10^{6}	5.0×10^{22}	3.67	3.40
398	1×10^{7}	3.2×10^{6}	1.9×10^{22}	3.58	3.58
448	1×10^{7}	3.2×10^{6}	7.4×10^{24}	4.00	3.70
498	1×10^{7}	3.2×10^{6}	5.8×10^{22}	3.65	4.28
CR25	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^{7}	3.2×10^{6}	2.3×10^{62}	9.84	5.88
348	1×10^{7}	3.2×10^{6}	2.5×10^{70}	11.1	7.00
398	1×10^{7}	3.2×10^{6}	9.3×10^{70}	11.2	7.92
448	1×10^{7}	3.2×10^{6}	8.8×10^{65}	10.4	6.32
498	1×10^{7}	3.2×10^{6}	4.1×10^{62}	9.84	8.23
CR27	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^{7}	3.2×10^{6}	1.9×10^{20}	3.29	5.11
348	1×10^{7}	3.2×10^{6}	6.1×10^{24}	4.02	5.65
398	1×10^{7}	3.2×10^{6}	5.8×10^{30}	4.99	6.42
448	1×10^{7}	3.2×10^{6}	1.5×10^{34}	5.54	6.23
498	1×10^{7}	3.2×10^{6}	1.3×10^{34}	5.53	8.98

Table 2. Fitting parameters to the mobility models used to describe the behaviour of n-channel MOSFET structures

8. Temperature-dependent electrical characteristics of p-channel 4H-SiC MOSFETs

The data in Figures 17, 18 and 19 show the V_{GS} –I_{DS} and V_{GS} -*log*(I_{DS}) characteristics for a 1600×1.5 μm p-channel MOSFET from the HV06 sample and an 8000×1.5 μm CR25 and CR27 p-channel MOSFET, respectively, measured from 298 to 498 K. The drain bias in each of the measurements was 500 mV. The data for each of the samples exhibits a similar trend, showing an increase in drain current with increasing temperature, a change in threshold voltage and a change in the subthreshold slope across the measured temperature range. In contrast to the n-channel data shown in Figures 4(b), 5(b) and 6(b), all p-channel samples exhibit a very low reverse leakage current of below 1 pA as shown in Figures 17(b), 18(b) and 19(b).

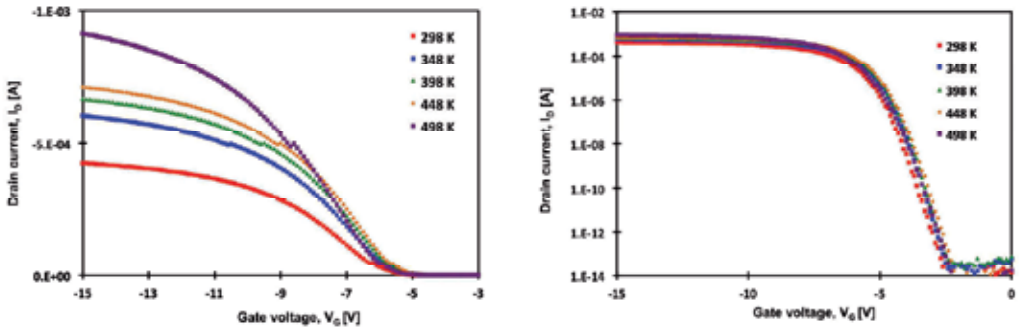

Figure 17. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of a 1600×1.5 μm p-channel MOSFET from sample HV06

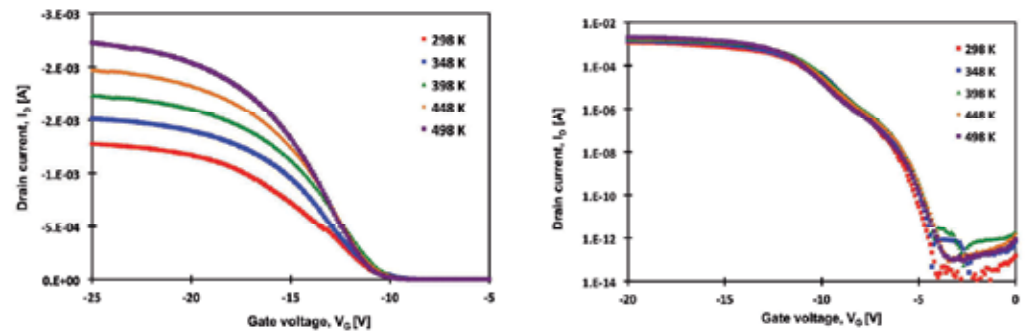

Figure 18. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR25

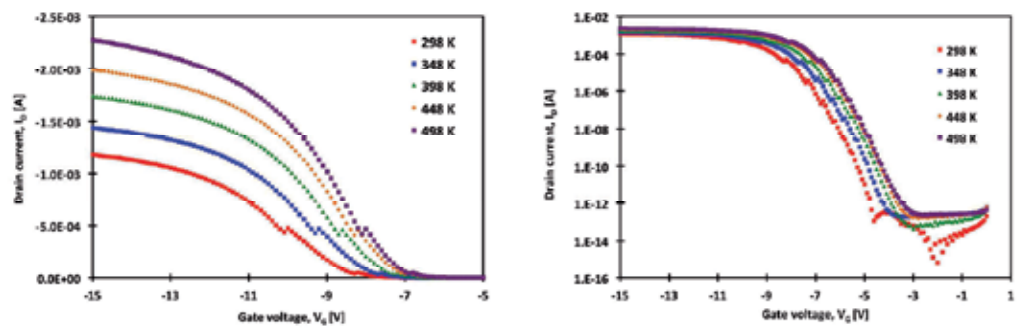

Figure 19. (a) V_{GS} –I_{DS} and (b) V_{GS} -log(I_{DS}) characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR27

The change in threshold voltage with temperature is also shown for each of the transistors across the temperature range by the data in Figure 20. The threshold voltage of a MOSFET can be calculated using equation 13 [21], and as with the n-channel devices, CR27 shows a reduction (i.e. becoming closer to zero) in V_{TH} with increasing temperature due to the reduction

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in the surface band bending required for inversion. This observation is identical to that observed in the n-channel data and is due to the increase in intrinsic carrier concentration and the decrease in band gap energy with increasing temperature. The data for HV06 shows a minimal change in V_{TH} with increasing temperature. However, in contrast, the data for CR25 shows an increase in V_{TH} with temperature. This could be due to a change in the interfacial charge or a change in the charge within the depletion layer, which can also act to modify the gate voltage as V_{FB} is dependent on the charge trapped at the silicon carbide–oxide interface. This is likely to be due to the increase in D_{it} with temperature that was witnessed in monolithically fabricated MOS capacitor structures and the effects of mobile oxide charge present within the dielectric.

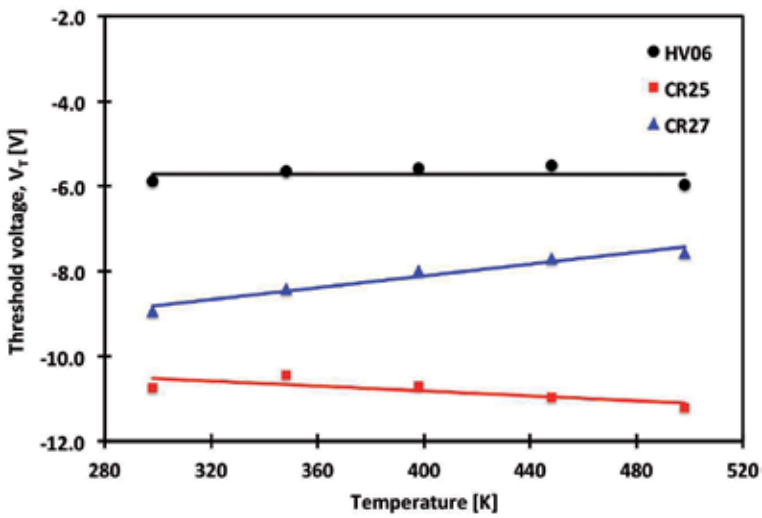

Figure 20. Threshold voltage as a function of temperature for 1.5 μm gate length p-channel MOSFETs

The increase in current with temperature that can be observed from the data shown in Figures 17(a), 18(a) and 19(a) for the three dielectrics studied is due to the decrease of occupied interface traps with an increase in temperature, which is an agreement with D_{it} values extracted from capacitor-based test structures fabricated monolithically with the MOSFETs. As the density of interface traps (D_{it}) decreases with increasing temperature, at a given gate voltage, more carriers are available for conduction in the MOSFET channel, as observed in previous reports in the literature [14].

The data in Figure 21 shows the variation in subthreshold slope (*SS*) with temperature for each of the samples. As shown, all three samples show an increase in *SS* with temperature. An increase in *SS* with temperature is expected, since *SS* is proportional to kT/q. The variation in *SS* with temperature is also influenced by the density of interface trapped charge (D_{it}) at the silicon carbide–oxide interface as *SS* is also dependent on the interface trap capacitance (C_{it}) as outlined in equation 14. This is in agreement with the trend witnessed for the equivalent n-channel MOSFET samples with the exception of sample CR25. The n-channel equivalent

sample for CR25 showed a decrease in *SS* with temperature, whereas the p-channel device exhibits an increase in *SS* for increasing temperature, and the observed change is much smaller than that of the n-channel device. This is related to the experimentally measured variation in D_{it} over the measured temperature range on monolithically fabricated capacitor test structures.

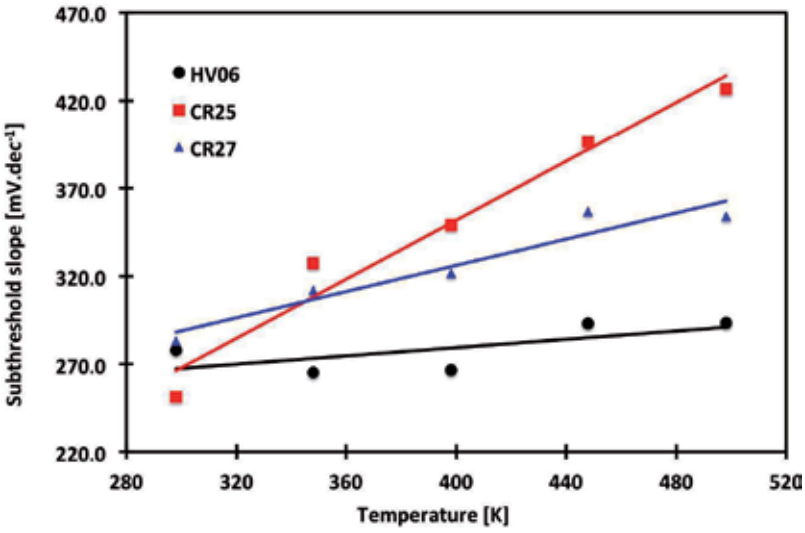

Figure 21. Subthreshold slope as a function of temperature for 1.5 μm gate length p-channel MOSFETs

The data shown in Figures 22, 23 and 24 show the variation of μ_{FE}-E and the μ_C-E characteristics for the 1.5 μm gate length p-channel MOSFETs on HV06 and CR25 and CR27, respectively, measured from 298 to 498 K. The data sets for all three dielectrics show evidence of an increase in field effect mobility with increasing temperature, and the data for CR27 in Figure 24 shows the highest field effect mobility out of the three samples across the temperature range studied.

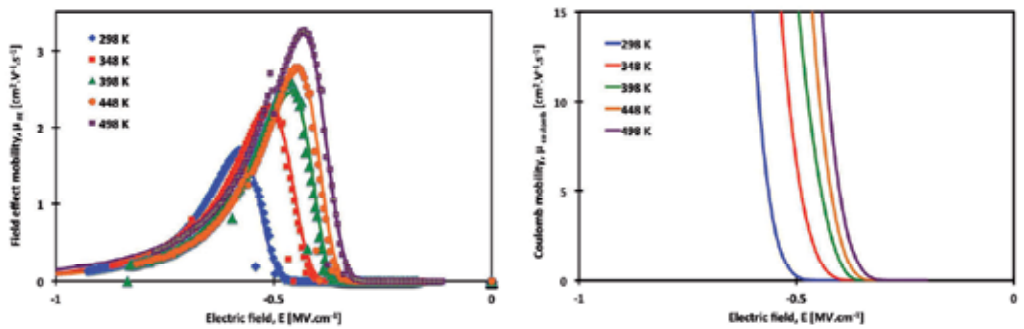

Figure 22. (a) μ_{FE}-E and (b) μ_C-E characteristics of a 1600×1.5 μm p-channel MOSFET from sample HV06

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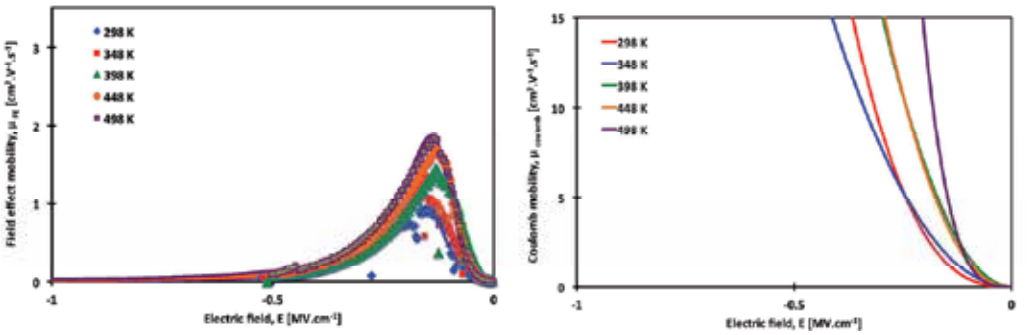

Figure 23. (a) μ_{FE} -E and (b) μ_C -E characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR25

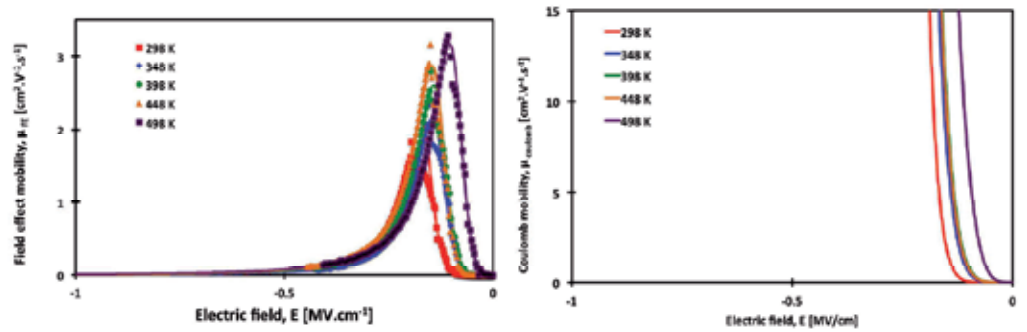

Figure 24. (a) μ_{FE} -E and (b) μ_C -E characteristics of an 8000×1.5 μm p-channel MOSFET from sample CR27

The data in Figures 22, 23 and 24 show the μ_{FE} -*E* and μ_C -E characteristics for 1.5 μm p-channel MOSFETs on HV06, CR25 and CR27 extracted from experimental V_{GS} –I_{DS} measurements taken at temperatures between 298 and 498 K that are shown in Figures 17, 18 and 19 using equation 2. All devices studied exhibit a similar trend and show an increase in field effect mobility with increasing temperature. The field effect mobility data for CR27 shown in Figure 24 demonstrates the highest field effect mobility across the temperature range out of the three samples, as supported by the data shown in Figure 25, which shows the peak field effect mobility of each device against temperature.

The data in Figures 22(b), 23(b) and 24(b) show the Coulomb mobility mechanism that was fitted to the measured characteristics using equation 11. As shown by the data in the figures, all of the devices (HV06, CR25 and CR27) show an increase in mobility with increasing temperature, which suggests that the effect of Coulomb scattering reduces with increasing temperature due to the reduction of interface trapping effects with increasing temperature. The same phenomenon was also witnessed in the equivalent n-channel MOSFETs, which suggest that the dominant mobility mechanisms are dominated by the processing of the gate dielectric for both the n- and p-channel devices.

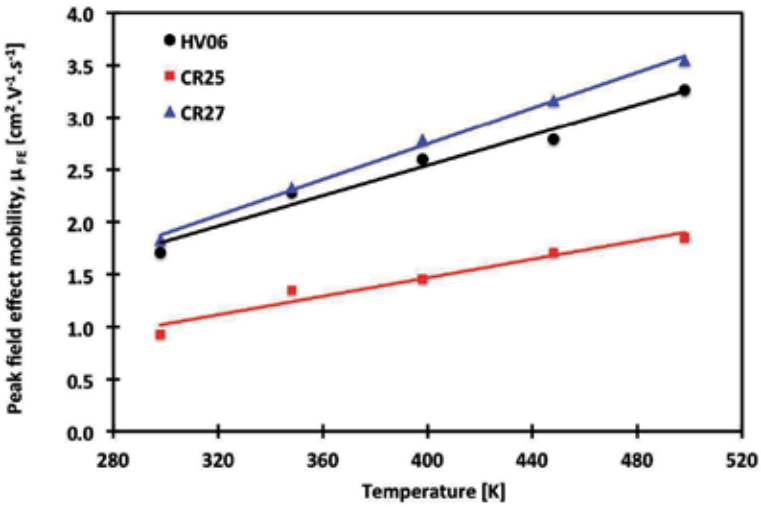

Figure 25. Peak field effect mobility (μ_{FE}) as a function of temperature for 1.5 μm gate length p-channel MOSFETs

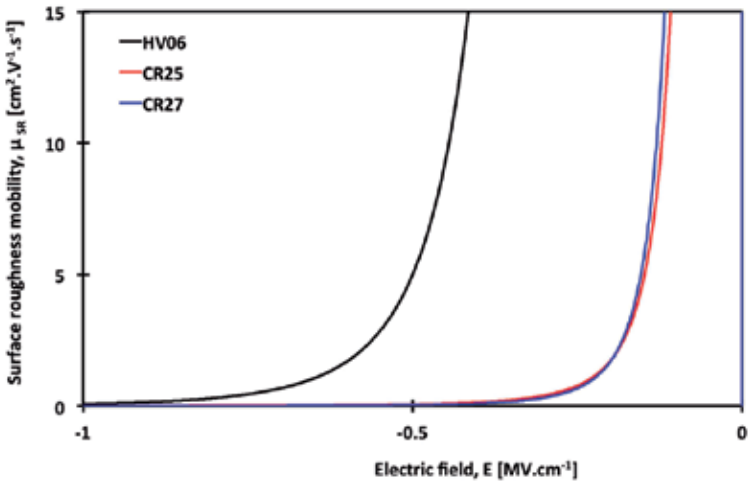

Figure 26. μ_{SR} -E characteristics of a 1600 x 1.5 μm HV06 and an 8000 x 1.5 μm CR25 and CR27 p-channel MOSFET at 298 K

At high electric fields, the extracted μ_{FE} for each of the devices is limited by surface roughness scattering as shown by the data in Figures 26 and 27, where the predicted μ_{SR} mobility fits to each of the extracted MOSFET μ_{FE} characteristics between 298 and 498 K. A negligible temperature dependence is exhibited by all three devices, which supports previous analysis performed on 4H-SiC MOSFETs and shows that the experimentally extracted μ_{SR} characteristics have the same functional form as expressed in equation 10 [5]. The data in Figure 26 shows the variation of the fitted surface roughness (μ_{SR}) as a function of electric field for each of the

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samples as 298 K. The data clearly identifies that the surface roughness mobility is different for each of the dielectrics under investigation. HV06 shows the highest surface roughness mobility, which suggests that surface roughness scattering is lower within the device and produces the highest quality dielectric–semiconductor interface out of the three samples investigated. The data for samples CR25 and CR27 show an almost identical surface roughness mobility across the measured electric field range, which suggests that the process techniques used in the fabrication of those samples produce a very similar quality of interface. However, all of the devices show very low field effect mobility at high electric fields, which is lower than recently reported values for 4H-SiC devices, such as those summarised in Table 4.

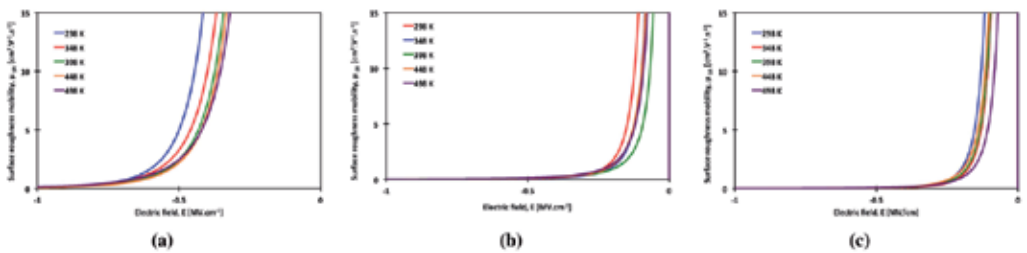

Figure 27. μ_{SR} -E characteristics of a 1600 x 1.5 μm (a) HV06 and an 8000 x 1.5 μm (b) CR25 and (c) CR27 p-channel MOSFET from 298 to 498 K

The data in Table 3 shows the fitting parameters used to generate the mobility plots for the p-channel FETs reported here.

This indicates that there is something common to all three dielectric processes that consistently act to reduce the surface roughness mobility. This could be due to the topography of the 4H-SiC epitaxial layer that was used for the fabrication of the devices or could potentially be a contribution of surface damage due to the ion implantation doping or the post-implantation anneal process that was used to form the n-type regions that are employed across all of the p-channel devices. In order to establish if this is the true cause, an investigation of the surface morphology using a technique such as atomic force microscopy is required, with measurements performed after the implantation and anneal process to measure the surface roughness, which could then be correlated to the measured electrical characteristics of the devices. A limited amount of data is available from a similar study conducted on n-channel 4H-SiC MOSFETs to establish the impact of the morphological and electrical properties of the SiO_2–4H-SiC interface on the mobility behaviour of 4H-SiC MOSFETs. The results indicated that a higher mobility can be observed in devices with a larger root-mean-square (RMS) roughness of the channel surface, possibly due to lower values of D_{it} associated to faceted surface morphologies [26]. However, this limited data contradicts observations made on other semiconductor systems, such as silicon and silicon-germanium. However, in the case of silicon carbide, evidence indicates a strong dependence between carrier mobility and the crystal surface from which the device is fabricated [27].

HV06	Acoustic phonon		Surface roughness		Coulomb
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	3.7×10^{34}	5.9	5.0
348	1×10^6	3.2×10^6	7.2×10^{28}	5.0	3.7
398	1×10^6	3.2×10^6	6.2×10^{27}	4.8	2.6
448	1×10^6	3.2×10^6	1.5×10^{27}	4.7	3.3
498	1×10^6	3.2×10^6	2.5×10^{23}	4.0	4.1
CR25	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	1.2×10^{19}	3.6	2.7
348	1×10^6	3.2×10^6	8.3×10^{15}	3.0	2.1
398	1×10^6	3.2×10^6	3.2×10^{11}	2.2	2.0
448	1×10^6	3.2×10^6	1.1×10^{15}	2.8	2.1
498	1×10^6	3.2×10^6	2.4×10^{13}	2.5	3.4
CR27	**Acoustic phonon**		**Surface roughness**		**Coulomb**
Temp	**B**	**C**	**D1**	**γ1**	**θ**
298	1×10^6	3.2×10^6	10.0×10^{21}	4.1	9.1
348	1×10^6	3.2×10^6	1.2×10^{19}	3.6	6.4
398	1×10^6	3.2×10^6	2.2×10^{18}	3.4	6.0
448	1×10^6	3.2×10^6	1.4×10^{18}	3.4	6.2
498	1×10^6	3.2×10^6	1.9×10^{14}	2.7	4.1

Table 3. Fitting parameters to the mobility models used to describe the behaviour of p-channel MOSFET structures

The data in Figure 28 shows the predicted values for the mobility limited by acoustic phonon scattering (μ_{AC}) based on equation 9. The parameters used to generate the values for μ_{AC} are identical to those used in the n-channel devices reported in a previous section and have been taken from the literature [5,8]; B is 1.0×10^6 cm s^{-1}, C is 3.23×10^6 K cm s^{-1} and α is 0.0284. As shown by the data in Figure 28, the modelled acoustic phonon mobility is consistently above 150 cm^2 V^{-1} s^{-1} for electric fields below 3.5MV cm^{-1} for the temperature range studied. Because the predicted mobility is significantly higher than both μ_{SR} and μ_C, the field effect mobility of a p-channel MOSFET is not determined by a contribution from acoustic phonon scattering. As observed with the n-channel data, the characteristics are consistently dominated at low and high electric fields by Coulomb and surface roughness scattering as shown by the data in Figures 22(b), 23(b), 24(b) and 27.

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Ref	Device	Gate dielectric	Gate dimensions (W×L μm)	Peak μ_{FE} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	V_T (V)	T_{ox} (nm)	D_{it} ($cm^{-2} \cdot eV^{-1}$)
28	n-FET	SiO_2 (pyro)	10×150	6.2	5.8	47	7.1×1011
		SiO_2 (pyro + NO)		30.4	2.7	51	1.3×1011
29	n-FET	SiO_2 (dry)	120×400	4	5		
		SiO_2 (dry +NO)		30			
30	n-FET	SiO_2 (dry + NO)	320×40	34		125	
31	n-FET	SiO_2 ($POCl_3$ POA)	30×200	89	0	56	9×10^{10}
32	n-FET	SiO_2 ($POCl_3$ PDA)		108		45	5×10^{11}
33	n-FET	SiO_2 (P_2O_5 POA)	150×290	72			3×10^{11}
34	n-FET	SiO_2 (N_2O POA)	150×290	55			3×10^{11}
35	n-FET	SiO_2 (N_2O PDA)	40×16	40		30	7.2×10^{11}
36	n-FET	SiO_2 (N_2O POA)	140×50	49		54	
37	n-FET	SiO2 (NO)	200×200	31	1.6	65	
		SiO_2 (2hr N plasma)		22	1.6	50	
		SiO_2 (4hr N plasma)		34	2.0	48	
38	n-FET	SiO_2 with Na contam	400×400	90	5		
39	p-FET	SiO_2 (pyro)	10×150	5.5	-8.5	47	8.9×1011
		SiO_2 (pyro + NO)		5.6	-6.4	51	1.3×1011
40	p-FET	SiO_2 (N_2O)	100×200	10		47	1×10^{12}
41	p-FET	SiO_2 (pyro+wet+Ar)	100×150	15.6	-4.2	45	2×10^{12}
42	p-FET	SiO_2 (N_2O)	4×150	5	-6	38	1×10^{12}

Table 4. Comparison of 4H-SiC MOSFET characteristics

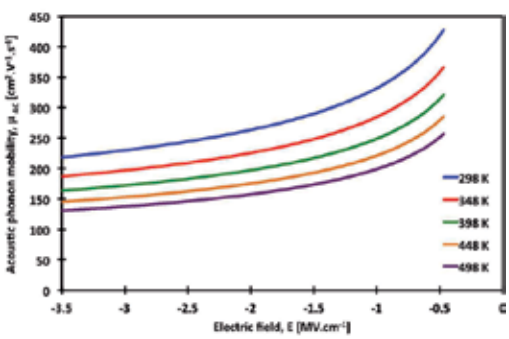

Figure 28. μ_{AC} -E characteristics for a 1.5 μm gate length p-channel MOSFET

9. Impact of gate dielectric on the 1/*f* noise characteristics of 4H-SiC MOSFETs

Low-frequency noise (1/*f* noise) measurements are used to study impurities and defects in semiconductor devices. The technique is useful to investigate device quality and reliability issues as well as the examination of the density of interface states in MOS devices. Whilst 1/*f* noise dominates the low frequency region (up to 100 kHz), it can be up converted into a high-frequency component affecting the phase noise characteristics of devices used for RF applications [43] as well as degrading the signal-to-noise ratio in analog circuitry. Very few studies of the 1/*f* noise in 4H-SiC have been explored to date [44 - 46]. Here, low-frequency noise is used to investigate how the gate dielectric influences the interface trap density and hence the characteristics of the 4H-SiC MOSFETs. The aim is to determine the impact of the interface quality and resulting noise characteristics on the device performance.

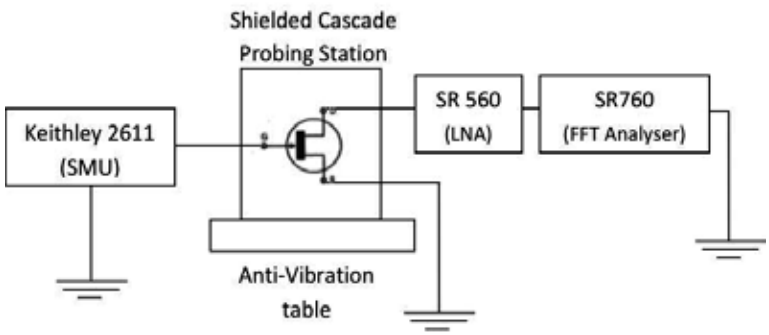

Figure 29. Schematic diagram of the low-frequency noise measurement set-up

The low-frequency noise measurements were conducted using a Stanford Research 760 FFT at 298 K, and the current-voltage characteristics that were used to normalise the characteristics were conducted on a Keithley 4200 SCS semiconductor analyser. A schematic of the measurement set-up is shown in Figure 29.

The normalised 1/*f* noise characteristics and the normalised noise power spectral density (NNPSD) for each of the dielectrics on the n-channel MOSFETs are shown in Figures 30, 31 and 32 for HV06, CR25 and CR27, respectively. The data in Figures 30(a), 31(a) and 32(a) show a plot of the NNPSD against frequency for varying V_{GS} for each of the n-channel MOSFETs studied. The data shows that each of the devices shows a similar trend, with the NNPSD decreasing with increasing gate bias, and this indicates that 1/*f* noise is higher at low gate biases (during weak inversion) and reduces at higher gate biases (at strong inversion).

Figures 30(b), 31(b) and 32(b) show the variation of normalised noise power spectrum (NNPSD) at 10 Hz as a function of V_{GS} and I_{DS} for each of the devices studied here. The trends observed in the data for each of the devices suggest that mobility fluctuations are the main contributor to the noise characteristics [47]. During weak inversion, the I_{DS} –*NNPSD* characteristics show a linear trend as shown by the data in Figure 30 (a), which suggests that carrier

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mobility fluctuations dominate the noise spectra, whereas during strong inversion and increased current levels, the dependency exhibits a different trend. This suggests that during weak inversion, the noise characteristics are dominated by carrier mobility fluctuations as a consequence or charge trapping at the interface due to Coulomb scattering as discussed in a previous section, which can be described by the McWhorter model [48]. During strong inversion, the noise characteristics reduce significantly due to the reduction in the effect of Coulomb scattering. The trends are also consistent with those reported by Rumyantsev et al. who examined the low-frequency noise characteristics of n-channel 4H-SiC with varying annealing treatments in NO [46].

CR27 exhibits the lowest noise characteristics of the three samples, which suggests that CR27 has the highest quality interface as there is a very low noise contribution from carrier mobility fluctuations at the interface, which suggests that the oxide also has the lowest trap density in the oxide out of the three dielectric samples. This is also in agreement with the findings of the D_{it} values extracted from the subthreshold slope data for CR27 that was presented in Figure 9.

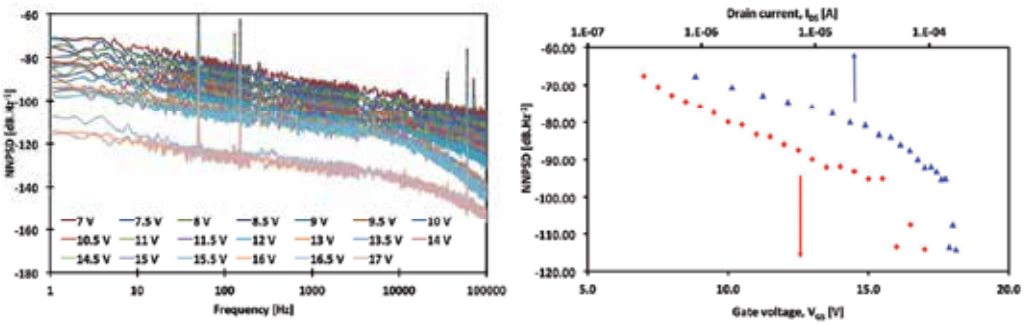

Figure 30. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with HV06 dielectric

In general, the frequency dependence of the NNPSD is described by equation 16:

$$NNPSD = \frac{\beta}{f^{\alpha}} \tag{16}$$

where α and β are fitting parameters. The frequency exponent (α) describes how much the trend deviates from a pure f^{-1} behaviour. The data in Figure 33 shows the variation of this frequency exponent, α, as a function of gate overdrive (V_{GS} -V_{TH}) for each of the n-channel MOSFETs, HV06, CR25 and CR27, respectively. As shown by the data, all three devices have consistently deviated from the common low-frequency noise exponent (α=1), and α values of between 0.5 and 1 have been extracted across the measured voltage range. According to theory, the frequency exponent deviates from 1 if the trap density is not uniform in depth, and because the extracted values of α<1, this suggests that the trap density is higher close to the silicon carbide–oxide interface and reduces further into the oxide [49].

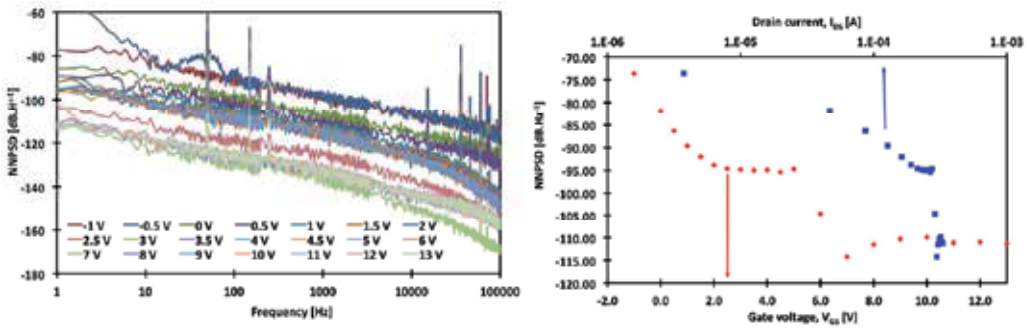

Figure 31. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with CR25 dielectric

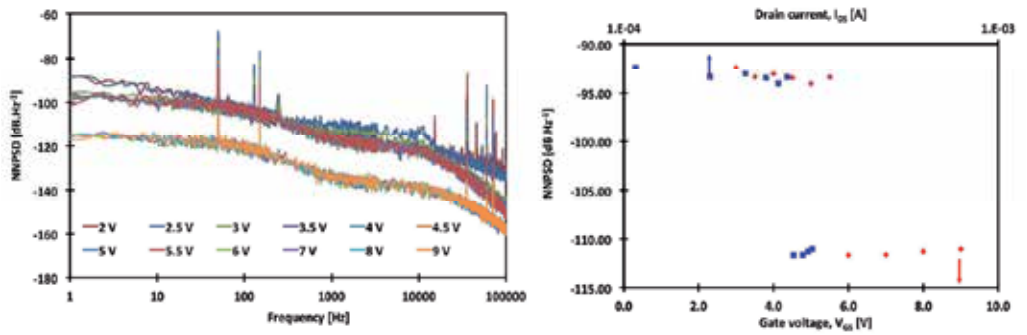

Figure 32. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 400×1.5 μm n-channel MOSFET with CR27 dielectric

The 1/*f* noise characteristics for each of the dielectrics on the p-channel MOSFETs are shown in Figures 34, 35 and 36 for HV06, CR25 and CR27, respectively. The data in Figures 34(a), 35(a) and 36(a) show a plot of the NNSPD against frequency for varying (V_{GS}) for each of the p-channel MOSFETs, HV06, CR25 and CR27, respectively. Both HV06 and CR25 exhibit a similar characteristic and suggest that 1/*f* noise is higher at low gate biases (during weak inversion) and reduces at higher gate biases (at strong inversion) as shown by the data in Figures 34(a) and 35(a). However, the data for sample CR27 shown in Figure 36(a) shows that NNSPD increases slightly with increasing gate bias for sample CR27; however, the noise level is substantially lower than the noise level in both HV06 and CR25. A plot of the normalised noise spectrum power density (NNSPD) at 10 Hz against V_{GS} and I_{DS} is shown for each of the devices in Figures 34(b), 35(b) and 36(b).

As with the n-channel devices, CR27 exhibits the lowest noise characteristics of the three p-channel samples, supporting the hypothesis that the quality of the silicon carbide–oxide interface is highest in this sample.

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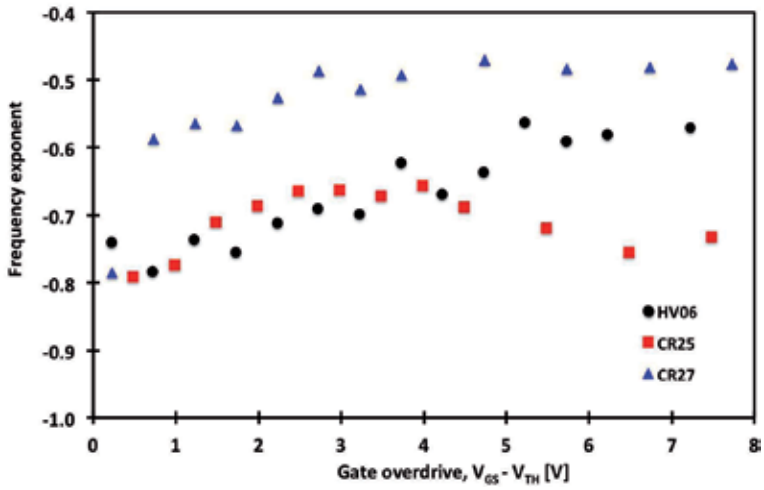

Figure 33. Variation of the frequency exponent as a function of gate overdrive for 400×1.5 μm n-channel MOSFETs

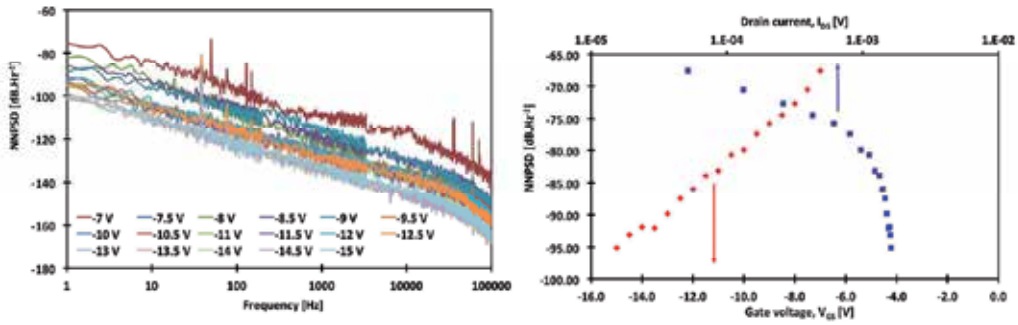

Figure 34. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with HV06 dielectric

The data in Figure 37 shows the variation of the frequency exponent as a function of gate overdrive ($V_{GS} - V_{TH}$) for each of the p-channel MOSFETs. The frequency exponent (α) was extracted from the data in Figures 34(a), 35(a) and 36(a) based on equation 16. The data for all three devices show consistent deviation from the common low-frequency noise exponent ($\alpha=1$), and values between 1 and 2 have been extracted across the measured voltage range. In contrast to data for the n-channel devices shown in Figure 33, the α values for the p-channel devices are all greater than 1. This indicates that in the case of the p-channel devices, the trap density is lower at the silicon carbide–oxide interface than in the bulk of the oxide and increases further into the oxide [49], similar to reported values for nitrided gate oxides in SOI MOSFETs [50].

The contrast between the distribution of the trapping states extracted from the 1/*f* noise data suggests that optimisation of the dielectric process steps for CMOS structures with monolith-

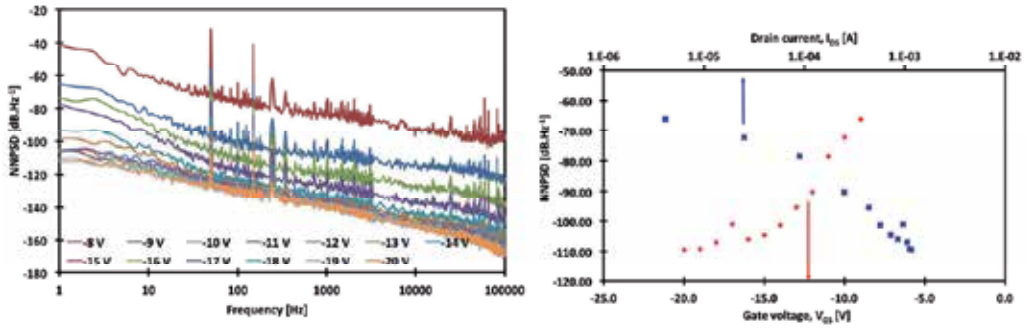

Figure 35. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with CR25 dielectric

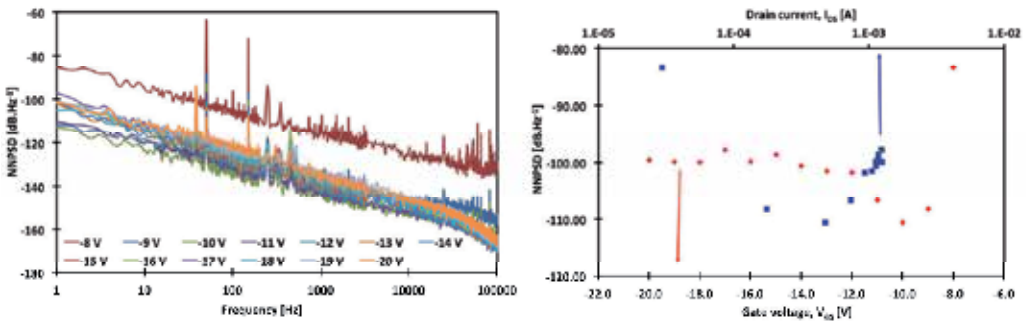

Figure 36. (a) NNPSD–f characteristics and (b) NNPSD at 10 Hz as a function of V_{GS} and I_{DS} for 8000×1.5μm p-channel MOSFET with CR27 dielectric

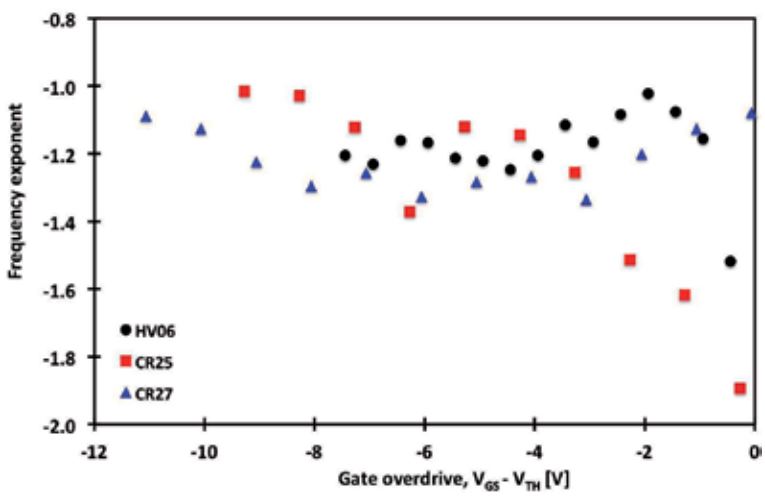

Figure 37. Variation of the frequency exponent as a function of gate overdrive for 8000×1.5μm p-channel MOSFETs

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ically fabricated n- and p-channel devices is more complex than the purely n-channel devices common in power electronic applications. The variation in depth of the highest trap density within the dielectric layer suggests that the electron interact with traps in the oxide close to the interface, whereas, holes interact with traps at deeper energy levels within the oxide.

10. Summary

The focus of this chapter was on the investigation of the electrical characteristics and device performance parameters of the 4H-SiC n- and p-channel MOSFETs that had undergone a range of dielectric process treatments to establish the suitability of conventional oxidation and deposited dielectrics for the realisation of complementary metal–oxide semiconductor circuits. The investigation into the temperature-dependent electrical characteristics of the devices demonstrated that all of the devices showed similar characteristics across the measured temperature range including an increase in I_{DS}, a reduction in V_{TH}, a reduction in D_{it} and, therefore, an increase in μ_{FE} with increasing temperature. This demonstrated that as temperature increases, there is a reduction of interface trapping effects, and therefore, Coulomb scattering reduces causing the device mobility and current to increase.

The CR27 samples for both n- and p-channel MOSFETs exhibit the highest field effect mobility characteristics, suggesting that a thin thermally grown oxide provides improved interfacial characteristics. This was further validated by the 1/*f* noise characteristics of the CR27 MOSFETs, which exhibited the lowest 1/*f* noise characteristics out of the three dielectrics at 298 K.

All three dielectrics in both the n- and p-channel devices showed severely high mobility limiting surface roughness scattering during strong inversion and high electric fields, which suggests that a process parameter – which is consistent amongst all three dielectrics and both the n- and p-channel devices – is causing high surface roughness in the channel, which is acting to degrade the channel mobility. In order to improve the device characteristics, a major focus should be given to increasing the surface roughness mobility of the samples. There is a strong trend across all of the examined samples of extremely low surface roughness mobility from applied electric fields of 1 MV cm^{-1} onwards, which is consistent across all of the processed samples and much lower than other reported devices. This is also consistent between the n- and p-channel devices, which suggests that it is inherent in the process technique used in both devices. This suggests that process contributions that are acting to degrade the surface roughness mobility of the devices is a major factor which is consistent across all of the samples. This suggests that the severely low μ_{SR} is not a contribution of the dielectric processing steps but could be a product of the ion implantation or the post-implantation anneal process.

An investigation into the 1/*f* noise characteristics of each of the MOSFET samples between 1 Hz and 100 kHz showed that in the n-channel MOSFETs, the oxide trap density was higher close to the interface, whereas, in the p-channel MOSFETs, the trap density was consistently higher further away from the silicon carbide–oxide interface consistently across all three dielectrics. The investigation also highlighted that in weak inversion, the 1/*f* noise characteristic of all of the devices is dominated by mobility fluctuations due to charge trapping at the

interface as a consequence of Coulomb scattering, which can be described by the McWhorter low-frequency noise model.

Finally, an investigation into the impact of the threshold voltage-adjust ion implantation procedure on the device characteristics was investigated for the CR27 n-channel MOSFETs. The findings showed that the increasing nitrogen dose was successful in acting to reduce the device threshold voltage; however, the nitrogen implant within the p-well also acts to improve the low electric field mobility characteristics of the n-channel 4H-SiC MOSFETs as an increased dose of nitrogen during the implant acts to reduce the effects of Coulomb scattering and therefore increase Coulomb mobility.

Author details

Lucy Martin, Hua-Khee Chan, Ming-Hung Weng and Alton Horsfall*

*Address all correspondence to: Alton.horsfall@newcastle.ac.uk

School of Electrical and Electronic Engineering, University of Newcastle, Newcastle, UK

References

[1] E. Arnold and D. Alok, IEEE Transactions on Electron Devices, Vol. 48 (2001) pp. 1870–1877.

[2] A. Perez-Tomas, P. Brosselard, P. Godignon, J. Millan, N. Mestres, M. R. Jennings, J. A. Covington, and P. A. Mawby, Journal of Applied Physics, Vol. 100 (2006) 114508.

[3] N. S. Saks, A. K. Agarwal, S. S. Mani, and V. S. Hegde, Applied Physics Letters, Vol. 76 (2006) pp. 1896

[4] A. Perez-Tomas, P. Brosselard, P. Godignon, J. Millan, N. Mestres, M. R. Jennings, J. A. Covington, and P. A. Mawby, Journal of Applied Physics, Vol. 100 (2006) 114508.

[5] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 7 (1988) pp. 1164–1171.

[6] D. K. Schroder, Semiconductor Material and Device Characterization, 3rd ed. John Wiley and Sons (Hoboken, New Jersey), 2006.

[7] H. Linewih, S. Dimitrijev, and K. Y. Cheong, Microelectronics Reliability, Vol. 43 (2003) pp. 405–411.

[8] D. Caughey and R. Thomas, Proceedings of the IEEE, Vol. 55 (1967) pp. 2192–2193.

[9] S. Potbhare, N. Goldsman, G. Pennington, A. Lelis, and J. M. McGarrity, Journal of Applied Physics, Vol. 100 (2006) 044515.

[10] C. J. Scozzie, F. B. McLean, and J. M. McGarrity, Journal of Applied Physics, Vol. 81 (1997) pp. 7687.

[11] S. K. Powell, N. Goldsman, J. M. McGarrity, J. Bernstein, C. J. Scozzie, and A. Lelis, Journal of Applied Physics, Vol. 92 (2002) 4053.

[12] J. Cooper, T. Tsuji, J. Williams, K. McDonald, and L. Feldman, IEEE Transactions on Electron Devices, Vol. 50 (2003) pp. 1582–1588.

[13] S. Potbhare, N. Goldsman, A. Lelis, J. M. McGarrity, F. B. McLean, and D. Habersat, IEEE Transactions on Electron Devices, Vol. 55 (2008) pp. 2029–2040.

[14] A. Hartstein, T. Ning, and A. Fowler, Surface Science, Vol. 58 (1976) pp. 178–181.

[15] G. Pennington, Journal of Applied Physics, Vol. 95 (2004) 4223.

[16] J. B. Varzgar, PhD Thesis, University of Newcastle, 2008.

[17] L. K. Swanson, P. Fiorenza, F. Giannazzo, A. Frazzetto, and F. Roccaforte, Applied Physics Letters, Vol. 101 (2012) 193501.

[18] P. Fiorenza, F. Giannazzo, M. Vivona, A. La Magna, and F. Roccaforte, Applied Physics Letters, Vol. 103 (2013) 153508.

[19] E. H. Nicollian and J. R. Brews, MOS (Metal Oxide Semiconductor) Physics and Technology. New Jersey: John Wiley and Sons, 2002.

[20] S. M. Sze and K. K. Ng, Physics of Semiconductor Devices, 3rd ed. New York: John Wiley and Sons, 2006.

[21] S. Dhar, S.-H. Ryu, and A. K. Agarwal, IEEE Transactions on Electron Devices, Vol. 57 (2010) pp. 1195–1200.

[22] Y. K. Sharma, A. C. Ahyi, T. Isaacs-Smith, A. Modic, M. Park, Y. Xu, E. L. Garfunkel, S. Dhar, L. C. Feldman, and J. R. Williams, IEEE Electron Device Letters, Vol. 34 (2013) pp. 175–177.

[23] S. Dhar, S.-H. Ryu, and A. K. Agarwal, IEEE Transactions on Electron Devices, Vol. 57 (2010) pp. 1195–1200.

[24] J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, T. Suzuki, and K. Fukuda, IEEE Electron Device Letters, Vol. 23 (2002) pp. 13–15.

[25] F. Roccaforte, P. Fiorenza, and F. Giannazzo, ECS Journal of Solid State Science and Technology, Vol. 2 (2013) pp. N3006–N3011.

[26] T. Masuda, S. Harada, T. Tsuno, Y. Namikawa, T. Kimoto, Material Science Forum, Vols. 600-603 (2009) pp. 695-698

[27] D. Okamoto, H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, IEEE Transactions on Electron Devices, Vol. 55 (2008) pp. 2013–2020

[28] G. Chung, C. Tin, J. Williams, K. McDonald, R. Chanana, R. Weller, S. Pantelides, L. Feldman, O. Holland, M. Das, and J. Palmour, IEEE Electron Device Letters, Vol. 22 (2001) pp. 176–178.

[29] M. Okamoto, M. Tanaka, T. Yatsuo, and K. Fukuda, Applied Physics Letters, Vol. 89, (2006) 023502.

[30] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, IEEE Electron Device Letters, Vol. 31 (2010) pp. 710–712.

[31] L. K. Swanson, P. Fiorenza, F. Giannazzo, A. Frazzetto, and F. Roccaforte, Applied Physics Letters, Vol. 101 (2012) 193501.

[32] Y. K. Sharma, C. Ahyi, T. Isaacs-Smith, A. Modic, M. Park, Y. Xu, E. L. Garfunkel, S. Dhar, L. C. Feldman, and J. R. Williams, IEEE Electron Device Letters, Vol. 34 (2013) pp. 175–177

[33] J. Rozen, A. C. Ahyi, X. Zhu, J. R. Williams, and L. C. Feldman, IEEE Transactions on Electron Devices, Vol. 58 (2011) pp. 3808–3811.

[34] A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, and F. Roccaforte, Applied Physics Letters, Vol. 99 (2011) 072117.

[35] J. Cooper, T. Tsuji, J. Williams, K. McDonald, and L. Feldman, IEEE Transactions on Electron Devices, Vol. 50 (2013) pp. 1582–1588.

[36] A. Modic, Y. Sharma, Y. Xu, G. Liu, A. Ahyi, J. Williams, L. Feldman, and S. Dhar, Journal of Electronic Materials, Vol. 43 (2014) pp. 857–862.

[37] B. R. Tuttle, S. Dhar, S.-H. Ryu, X. Zhu, J. R. Williams, L. C. Feldman, and S. T. Pantelides, Journal of Applied Physics, Vol. 109 (2011) 023702.

[38] D. Okamoto, H. Yano, T. Hatayama, Y. Uraoka, and T. Fuyuki, IEEE Transactions on Electron Devices, Vol. 55 (2008) pp. 2013–2020.

[39] M. Noborio, J. Suda, and T. Kimoto, IEEE Transactions on Electron Devices, Vol. 56 (2009) pp. 1953–1958.

[40] M. Okamoto, M. Tanaka, T. Yatsuo, and K. Fukuda, Applied Physics Letters, Vol. 89 (2006) 023502.

[41] A. Constant, M. Berthou, M. Florentin, J. Millan, and P. Godignon, Journal of the Electrochemical Society, Vol. 159 (2012) H516.

[42] S. L. Rumyantsev, M. S. Shur, M. E. Levinshtein, P. A. Ivanov, J. W. Palmour, M. K. Das, and B. A. Hull, Journal of Applied Physics, Vol. 104 (2008) 094505.

[43] C. X. Zhang, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, S. Dhar, S.-h. Ryu, X. Shen, and S. T. Pantelides, IEEE Electron Device Letters, Vol. 34 (2013) pp. 117–119.

[44] C. X. Zhang, X. Shen, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, S. A. Francis, T. Roy, S. Dhar, S.-h. Ryu, and S. T. Pantelides, IEEE Transactions on Electron Devices, Vol. 60 (2013) pp. 2361–2367.

[45] S. L. Rumyantsev, M. S. Shur, M. E. Levinshtein, P. A. Ivanov, J. W. Palmour, A. K. Agarwal, and S. Dhar, Semiconductor Science and Technology, Vol. 26 (2011) 085015.

[46] R. Voss and J. Clarke, Phys. Rev. B, Vol. 13 (1976) pp. 556–573.

[47] A. McWhorter, 1/*f* Noise and Germanium Surface Properties, R. H. Kingston, Ed. University of Pennsylvania Press (Philadelphia), 1957.

[48] R. Jayaraman and C. Sodini, IEEE Transactions on Electron Devices, Vol. 36 (1989) pp. 1773–1782.

[49] N. Lukyanchikova, M. Petrichuk, N. Garbar, E. Simoen, A. Mercha, C. Claeys, H. van Meer, and K. De Meyer, IEEE Transactions on Electron Devices, Vol. 49 (2002) pp. 2367–2370.

Chapter 4

Investigation of SiC/Oxide Interface Structures by Spectroscopic Ellipsometry

Sadafumi Yoshida, Yasuto Hijikata and Hiroyuki Yaguchi

Additional information is available at the end of the chapter

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Abstract

We have investigated SiC/oxide interface structures by the use of spectroscopic ellipsometry. The depth profile of the optical constants of thermally grown oxide layers on SiC was obtained by observing the slope-shaped oxide layers, and the results suggest the existence of the interface layers, around 1 nm in thickness, having high refractive index than those of both SiC and SiO_2. The wavelength dispersions of optical constants of the interface layers were measured in the range of visible to deep UV spectral region, and we found the interface layers have similar dispersion to that of SiC, though the refractive indices are around 1 larger than SiC, which suggests the interface layers are neither transition layers nor roughness layers, but modified SiC, e.g., strained and/or modified composition. By the use of an in-situ ellipsometer, real-time observation of SiC oxidation was performed, and the growth rate enhancement was found in the thin thickness regime as in the case of Si oxidation, which cannot be explained by the Deal-Grove model proposed for Si oxidation. From the measurements of the oxidation temperature and oxygen partial pressure dependences of oxidation rate in the initial stage of oxidation, we have discussed the interface structures and their formation mechanisms within the framework of the interfacial Si-C emission model we proposed for SiC oxidation mechanism.

Keywords: SiC-MOSFET, SiC/oxide interface, spectroscopic ellipsometry, SiC oxidation mechanism, interface state density

1. Introduction

SiC metal-oxide-semiconductor field effect transistors (MOSFETs) are still the main targets in the research and development of SiC switching devices, because of their capability of ultra-low loss, high-frequency and high-temperature operation, and high-current and high-voltage tolerance, resulting in, for example, reducing the volume of electric power conversion modules compared with those using Si devices. However, SiC-MOSFETs have some problems to be solved before wide use, such as their higher on-resistance and lower reliability than those predicted from bulk properties. These poor device characteristics have been attributed to, for example, low carrier mobility due to high interface state density at the SiC/oxide interface and crystal defects. To elucidate the origin of poor characteristics of interfaces, it is important to make clear the interface structures as well as the study on the relation between interface structures and electrical properties.

1.1. Observation methods of interface structures

As metal-semiconductor and insulator-semiconductor junctions, and semiconductor hetero-junctions are key components of semiconductor devices, many measurement and observation techniques, e.g., X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), scanning TEM (STEM), secondary electron microscopy (SEM), photoluminescence (PL) and cathodoluminescence (CL) spectroscopy, Rutherford backscattering spectroscopy (RBS), secondary ion mass spectroscopy (SIMS), have been adopted for the investigation of their interface structures. These techniques can be divided into three categories, i.e., (Figure 1)

1. observations of the interfaces on the cross section of specimens,

2. measurements of the thickness profile by etching or sputtering of the over or upper layers,

3. analysis of the signal coming from the interface through the upper layers.

In the cases of categories (1) and (2), there is a danger of the change and/or damage on the interface structures in the preparation process of specimens and by exposing the interface to the air, and a fear of non-uniformity of etching and/or sputtering of upper layers in an atomic layer thickness scale. In the case of cross-sectional TEM images, the specimen is required to reduce the thickness less than 100 nm. However, as the specimen is composed of still dozens of atomic layers, the image is formed by summing over the beams coming from a number of atomic layers in the specimen, and thus, it is hard to distinguish the effect due to the existence of interface layer from that of interface roughness and/or non-uniformity.

While, in the case of category (3), the observation is carried out without sample preparation, like thinning by etching and sputtering, and thus, there is no fear of the problems for the case of categories (1) and (2). In other words, the observation technologies belonging to category (3) are ideal ones which can observe the buried interface without any treatment, i.e., kept intact. However, this technique is only applicable to the case where the probing and signal beams from the interface can transmit through the upper or over layers, and thus, generally, the techniques are applicable only to the cases of very thin over layers or transparent ones for the

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probe beam. Optical methods like ellipsometry and infrared reflectance spectroscopy, X-ray reflectivity (XRR), and RBS are the examples of the technologies of category (3). In the case of technologies of this category, however, as the signals from the interface are mixed with those from the upper and lower layers, it is necessary to analyze the signal under the assumption of a certain structural model. The information on interface structures is derived by the fitting of the calculated values by use of the model assumed and the observed data. Therefore, the results strongly depend on the model assumed, and thus, to build up an appropriate structural model is very important for obtaining significant information of interfaces from the observation. The model assumed is, in a word, a hypothesis, and thus, it is necessary to verify the validity of the model used. The influence of the selection of model used in the analysis of the obtained data will be discussed in the case of ellipsometric measurements of SiC/oxide interfaces in Section 2.

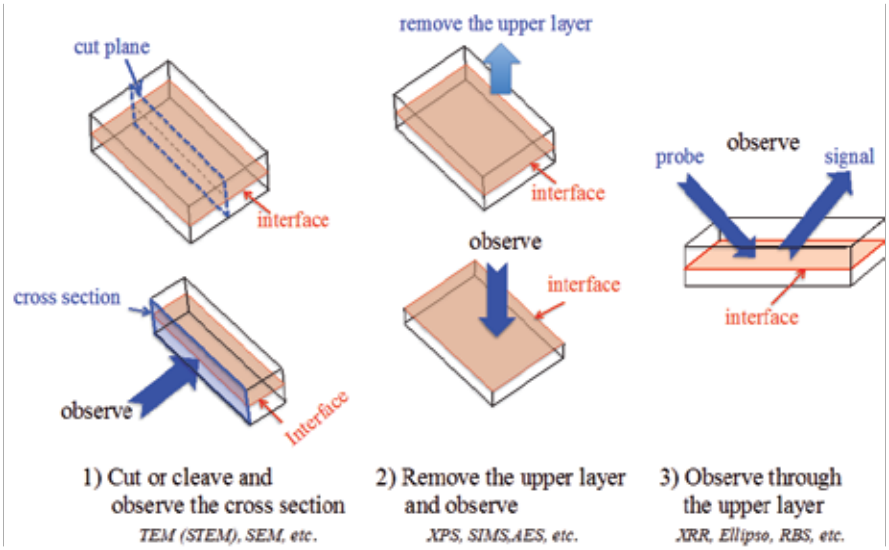

Figure 1. Three categories for the observation methods or techniques of interface structures.

1.2. Measurements by use of ellipsometry

As the oxide layers formed by thermal oxidation of SiC are transparent in the visible and ultraviolet spectral ranges, optical methods are suitable to detect the signal from the interface through the upper oxide layer. Especially, ellipsometry, i.e., the measurement of the changes in polarization upon the reflection of light from a surface, has very high sensitivity for very thin films because of the measurement of phase difference between p and s polarized light components and using oblique incident light beams, which brings about longer path in the films than those for perpendicularly incident light.

Many studies on the structures of Si/oxide interface by spectroscopic ellipsometry have been reported. Deal and Grove [1] measured the thickness of the thermal oxide on Si by using a

multiple beam interferometer in the range between 0.1 and 10 μm and derived the linear-parabolic model, so-called, D-G model, for Si oxidation. Taft and Cordes [2] reported the existence of the interface layers, 0.6 nm in thickness and 2.8 in refractive index by use of an ellipsometer at the wavelength λ = 546.1 nm. Aspnes and Theeten [3] have analyzed the interface structures in detail by spectroscopic ellipsometry. They proposed the equation to calculate the dielectric constants for two kinds of interface layers, i.e., physical mixture of amorphous Si and SiO_2, which corresponds to the cases of micro-roughness and inclusion or void in Si, and chemically mixed Si and O atoms. In the former, they used Bruggeman's effective medium approximation (EMA), and in the latter, they used Si-centered tetrahedral O atoms, $Si_{4-\nu}O$ (ν = 0-4) model by Philipp and composite medium theory by the Clausius-Mossotti relation. They reported that their results of spectroscopic ellipsometry for thermal oxides on Si are incompatible with either micro-roughness or an abrupt transition from Si to SiO_2, but rather support a graded transition layer, 0.7 ± 0.2 nm region in thickness of atomically mixed Si and O of average stoichiometry $SiO_{0.4\pm0.2}$. Massoud et al. [4] have performed in situ measurements of the thickness of Si oxides during the thermal oxidation in reduced oxygen partial pressure by the use of an automatic ellipsometer, and found the enhancement of the oxidation rate in thin thickness regime, which cannot be explained by the D-G mode, and showed good fit can be obtained by adding exponential term to D-G equation, though the physical meaning of adding new term, i.e., the origin of the exponential term, has not been ascertained. Nguyen et al. [5] found that the dielectric function of interface layers is similar to that of Si except the 0.02 eV red shift of inter-band critical point E_1 peak energy with rather small absolute values, from which they concluded there exist 2.2 nm thick interface layers composed of strained Si layer of 1.5 nm in thickness, and micro-roughness with 0.7 nm in optically equivalent thickness. They also said the transition layers reported by Aspnes and Theeten cannot be found, though the existence of the transition layers have been reported by using angle-resolved XPS, i.e., two monolayer compositional transition layers and one monolayer Si strained layer formed on a Si (001) face [6]. The refractive indices of very thin Si oxide layers were determined as a function of oxide thickness by ellipsometry using the thickness determined from tunnel current oscillation measurements [7]. Herzinger et al. measured the refractive indices of oxides on Si at the photon energy between 0.75 and 6.5eV by the use of variable-angle spectroscopic ellipsometry [8].

1.3. Observations of SiC/oxide interfaces

So far, many studies on SiC/oxide interface structures have been performed using various techniques, e.g., cross-sectional TEM and STEM belonging to category (1), and e.g., XPS and SIMS belonging to category (2). However, the results are sometimes contradicted with each other, and/or the results cannot be verified because of the fears mentioned above. For example, it has been reported that the SIMS measurement shows C atoms piled up near the interface more than 20%, and several percent even in Si oxide layers. On the contrary, it has been reported that XPS and medium energy ion scattering (MEIS) measurements suggest no such excess C around the interface and in the oxide films [9-11]. This contradiction is considered to be partly due to the difficulty in distinguishing between C atoms bonded to Si in adjacent SiC layers, the content of which is $10^{22}/cm^3$ order and excess C atoms near the interface in the case

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of SIMS observation. In the case of XPS, C atoms bonded with Si and O can be distinguished between each other by the difference in their chemical shifts. As another example, Zheleva et al. [12] reported that high-resolution STEM combined with EELS measurements show the existence of interface layers, around 10 nm in thickness, with C-rich composition, and the thickness of the interface layers well correlates with the interface state density [13]. On the contrary, Hatakeyama et al. [14] reported that nosuch thick interface layer was observed by use of the same techniques, HAADF-STEM and EELS measurements, and, if there exists, it is less than 1 nm, which agrees with other measurements including our results by the use of spectroscopic ellipsometry.

Ellipsometry has been used mainly in the measurements of the thickness of oxide layers, where the interface structures were not taken into account. Suzuki et al. [15] and Zheng et al. [16] for 6H-SiC and Fung and Kopanski [17] for 3C-SiC measured oxide thickness by use of ellipsometry, and explained the oxidation time dependence of the oxide thickness by diverting the D-G model proposed for Si oxidation. Song et al. [18] measured oxide thickness of thermally grown oxide on 4H-SiC by use of RBS and spectroscopic ellipsometry, and found good agreement with each other, and they modified the D-G model in order to apply to SiC oxidation, i.e., adding the process of CO diffusing out from interface to surface as well as oxygen diffusion from surface to interface in the diffusion-limited regime, and used to explain their experimental results for oxidation time dependence of oxide thickness. It is noted that all of these measurements were performed by ex situ ellipsometry measurements, i.e., ellipsometric measurements were performed in air at room temperature after taking out from the oxidation furnace.

Sometimes, the thicknesses derived from the ellipsometry measurements are used as "physical thickness", or index of the progress of oxidation in the studies on, for examples, thickness dependences of some physical and chemical properties of oxide layers on SiC. If oxide layers are optically not uniform in the depth direction from SiC/oxide interface to oxide surface, and/or if the refractive indices of oxide layers are not same as those of stoichiometric SiO_2, e.g., there exist interface layers having different composition or properties from that of oxide layers, the thicknesses obtained are never physical thickness, because the thicknesses were derived under the assumption of an optically uniform single layer of stoichiometric SiO_2 on SiC with abrupt interface.

RBS, XRR, and Fourier-transformed infrared (FTIR) spectroscopy, the technologies belonging to category (3), have also been used to characterize SiC/oxide interfaces. RBS technique has been used mostly combined with ellipsometry. Ray et al. [19] measured oxide thickness by spectroscopic ellipsometry in the range thinner than 15 nm, and by RBS and ion channeling technologies as well as spectroscopic ellipsometry in the large thickness range, and studied on the oxygen partial pressure dependence of oxidation mechanisms and interface density by use of the analysis using the D-G model. Szilagyi et al. [20] measured oxide thickness and density by using spectroscopic ellipsometry and RBS, and roughness by atomic force microscopy (AFM), and the differences in oxidation process for Si- and C-faces of 4H-SiC were discussed comparing with that of Si. They also used modified D-G model to analyze oxidation mechanisms. A limited number of the results on the SiC/oxide interface structures obtained by use

of XRR and FTIR spectroscopy have been reported so far. The effects of NO annealing after oxidation of SiC to the interface structures and electrical properties were studied by use of XRR measurements for 6H-SiC [21] and 4H-SiC [22]. FT-IR spectroscopy by using attenuated total reflection (ATR) method has been performed to know the structures of the ultra-thin oxides on SiC [23,24]. The differences in stress and chemical state of oxides and oxide/SiC interface have been studied from the observation of TO and LO mode absorption due to Si-O-Si bond asymmetric stretching vibration for the oxides on Si- and C-faces of 6H-SiC and 4H-SiC.

We have employed spectroscopic ellipsometry for observing the SiC/oxide interface to investigate SiC/oxide interface structures. We have developed the characterization method of the oxide layers and SiC/oxide interfaces, i.e., the method using sloped oxide layers, and made clear the depth profile of the refractive indices and interface structures, i.e., there exist interface layers, around 1 nm in thickness, having high refractive indices [25,26], the values of which closely relate to the electrical properties of MOS diodes [27]. By the extension of measurement of wavelength to deep ultraviolet range, the structures of interface layers were discussed [28]. We have also developed the observation system in order to perform real time *in-situ* observation of SiC oxidation [29] for the first time. By using this system, we have found the enhancement of oxidation rate of SiC in thin-thickness regime less than several nm [30,31] as in the case of Si oxidation, and discussed on the oxidation and interface layer formation mechanisms [32]. These results have led to the proposal of a novel oxidation mechanism of SiC, i.e., "interfacial Si-C emission model" [33].

In this paper, the measurements of the depth profile of the refractive indices of thermal oxidation layers on SiC by using spectroscopic ellipsometry are described in Section 2, followed by the characterization of the interface layers, and their relation to the electrical properties of MOS diodes in Section 3, the real-time observation of SiC oxidation in Section 4, and the discussions on the SiC oxidation process and interface layer formation process based on SiC oxidation mechanisms in Section 5, and finally we summarize the investigations of SiC/oxide interface structures by using spectroscopic ellipsometry. All the spectroscopic ellipsometry measurements in this chapter were performed using a commercial spectroscopic ellipsometer typed GESP-5 (Sopra), typically at an angle of incidence of 75°.

2. Measurements of the depth profile of the refractive indices of thermal oxidation layers on SiC

2.1. Thickness dependence of apparent refractive indices of oxide films

The (0001) Si-faces of commercial 6H polytype SiC epilayers, 5 μm in thickness and n-type with the carrier concentration of 5×10^{15}cm^{-3}, were oxidized by two methods, pyrogenic oxidation and oxidation in dry oxygen flow, so-called dry oxidation [25]. Pyrogenic oxidation was conducted at 1100°C in a flow of oxygen and hydrogen gases for 1-8 h. Dry oxidation was conducted at 1000°C in a flow of oxygen for 4-16 h. Ellipsometry measurements were performed in the wavelength range from 250 to 850 nm. We have derived the optical constants

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and the thickness of the oxide films under the assumption that the films have an optically single-layer structure and have uniform and isotropic optical properties. Here, we call the refractive indices obtained under the model of a single layer as "apparent refractive indices", in order to distinguish from those by use of a two-layers model mentioned in the next section. The wavelength dependence of the refractive indices of oxide films were assumed to follow Sellmeier's dispersion law,

$$n = \sqrt{1 + \frac{\left(n_{inf}^2 - 1\right)\lambda^2}{\lambda^2 - \lambda_0^2}}, \tag{1}$$

where parameter n_{inf} is the refractive index of the wavelength at infinity, while parameter λ_0 is the wavelength corresponding to characteristic oscillation. Here, we assumed the extinction coefficient $k = 0$ over the wavelength range measured. The values of the thickness of the film and the parameters n_{inf} and λ_0 were derived by fitting the wavelength-dependence curves of calculated ellipsometric parameters (Ψ, Δ) to the measured ones. The surface roughness of the oxide films on SiC was examined by means of atomic force microscopy (AFM) measurement, and the root mean square of the surface roughness is around 0.2 nm.

Figure 2(a) shows the wavelength dependences of the refractive indices of the oxide films, thickness of which are both 20 nm, oxidized with two different methods, i.e., pyrogenic and dry oxidation. For comparison, the values for oxide films on Si are also shown in the figure. It is found from the figure that the refractive indices of the oxide films on SiC are both smaller than those of the oxide films on Si at all the wavelengths measured. The figure also reveals that the refractive indices for dry oxidation are smaller than those for pyrogenic oxidation. The refractive indices increase with oxidation time or oxide thickness and reaching to the values for oxide films on Si, though the values of all the films are smaller than those of oxide on Si. The thickness dependences of the refractive indices at the wavelength of 630 nm for dry oxidation are shown in Figure 2(b). For pyrogenic oxidation, the refractive indices decrease with the decrease of film thickness as in the case of dry oxidation. It has been reported that, for Si, the refractive indices of the oxide films increase with the decrease of film thickness, as shown by the dotted line in the figures [7], which is quite different from those for the oxide films on SiC reported here. In Si oxidation, the increase of refractive indices along with the decrease of oxide thickness has been explained by the existence of the transition layers, i.e., suboxide layers SiO_x with $x < 2$ at Si/SiO_2 interfaces, whose refractive indices are larger than those of SiO_2, while the decrease of refractive indices for SiC oxidation cannot be explained by the existence of a $SiC\text{-}SiO_2$ transition layers. As the refractive indices of SiC are larger than those of SiO_2, the refractive indices of transition layer, i.e., the $SiC\text{-}SiO_2$ mixed layer SiC_xO_y should be larger than those of SiO_2.

As another candidate to explain these phenomena, the roughness of SiC/oxide interfaces can be considered. The roughness observed by AFM shows that there exists rugged structure with the various peak to valley height and interval over the surface much less than 1 nm, which are both much smaller than the wavelength of light used in ellipsometry measurements. In such a case, i.e., the case that the wavelength of a prove beam is much larger than the scale of surface

microstructures, the rough surface can be treated as the existence of an optically equivalent layer having the composition of the mixture of the adjacent layers of interface. Therefore, the refractive indices of optically equivalent layers corresponding to rough interface are also the values between the refractive indices of SiC and those of SiO_2, i.e., larger than those of SiO_2, and thus small refractive indices of oxide films cannot be explained by the effect of interface roughness.

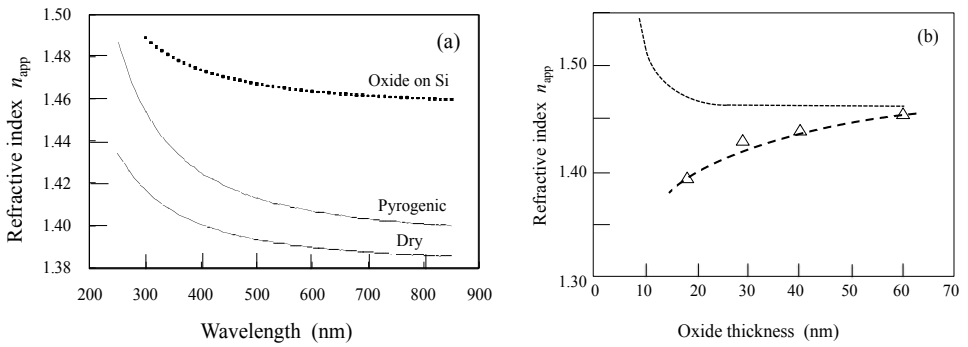

Figure 2. (a) Wavelength dependences of the refractive indices of oxide films formed by dry and pyrogenic oxidation. (b) Oxide thickness dependence of refractive indices of oxide films by dry oxidation. The dotted lines show the values for oxide film on Si [25].

2.2. Measurements of the depth profile of the refractive indices using sloped oxide films

In the previous section, the apparent refractive indices n_{app} obtained under the assumption of an optically single layer structure are shown to be smaller than those of the oxide films on Si, and increase with oxide film thickness, reaching the values of Si oxides of around 60 nm in thickness. To make clear why these apparent refractive indices change with oxidation time or oxide thickness, the depth profile of the refractive indices of oxide films on SiC was measured by spectroscopic ellipsometry [26].

For measurements of the depth profile or thickness dependence of the refractive indices of oxide films, we have proposed the method of using a slope-shaped oxide films. The pieces of SiC substrates with oxide layers were immersed gradually in buffered hydrogen fluoride at a constant speed to form slope-shaped oxide layers. The schematic illustration of the method is shown in Figure 3 [34]. Using the sloped oxide films, it is possible to measure the optical properties of the oxide films having various thicknesses using one sample. This means only the film thickness changes along the slope, though the interface structures are the same for all positions, i.e., for all oxide thicknesses. Of course, oxide films with various thicknesses can also be obtained by changing the oxidation time. By this method, however, there is a fear of change in the film structures, particularly the interface structures with the oxidation time.

(0001) Si-faces of n-type 6H-SiC epilayers having 5 μm in thickness and the carrier concentration of 5×10^{15} cm^{-3} were used for the study. The epilayer surfaces were oxidized in dry oxygen flow at 1100°C for 16 h to form the oxide films with around 60 nm in thickness. The sloped

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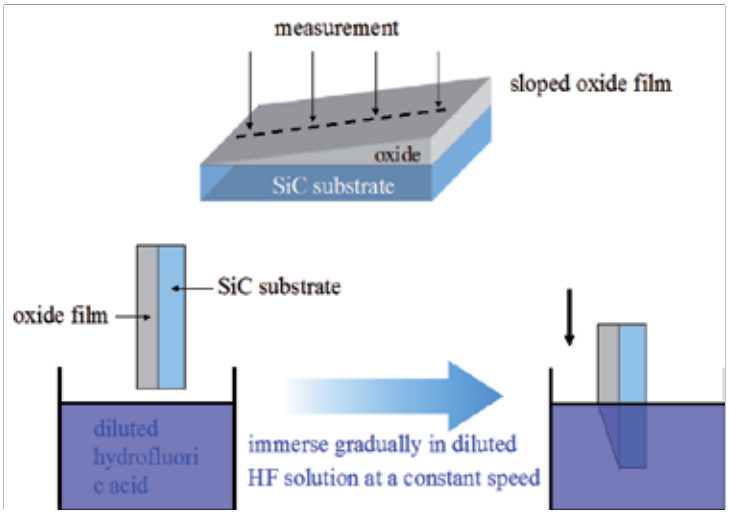

Figure 3. Schematic illustration of the method to fabricate a slope-shaped oxide film on SiC.

oxide films were fabricated by the method mentioned above, and ellipsometry measurements have been carried out at the positions along the slope.

Firstly, we have obtained the apparent refractive indices and film thickness assuming an optically single-layer structure with uniform optical properties, same as in Section 2.1. The variations of oxide thickness in the measured position along the slope are shown in Figure 4(a). From the figure, it is found that the oxide thickness changes almost linearly with the position, except in very small oxide thickness region, which means that the oxide films were etched at an angle as expected. Figure 4(b) shows the changes in n_{app} along the slope at the wavelength λ = 630 nm, for example. Figure 5 shows those as a function of oxide thickness. The refractive indices decrease with film thickness at all the wavelengths measured as in the case at 630 nm. It is found from the figure that n_{app} at 60 nm in thickness is around 1.45, which is almost the same as that reported for stoichiometric SiO_2, i.e., fused quartz. With the decrease of oxide film thickness, the value of n_{app} decreases gradually. At the positions with oxide thickness smaller than 5 nm, the values of n_{app} decrease markedly with the decrease of oxide thickness and approaches 1 at the position of the oxide film thickness = 0. As this feature is nearly the same as those observed for the oxide films formed by other oxidation methods mentioned in Section 2.1, it can be said that n_{app} decreases with decreasing oxide film thickness regardless of the oxidation method.

These results contradict the assumption used for the evaluation of the refractive indices and the thickness from the measured ellipsometeric parameters, i.e., the films are composed of optically single layers and have uniform and isotropic optical properties. This contradiction, therefore, suggests that this assumption is inadequate for the analysis. Then, we have considered the film structure models that can explain the thickness dependence of the refractive indices obtained from the ellipsometry measurements. For the oxide films on Si, it has been said there exists a compositional transition layer at the interface between Si and oxide [7]. Similarly, for the oxide films on SiC, it can be considered the presence of a transition layer at

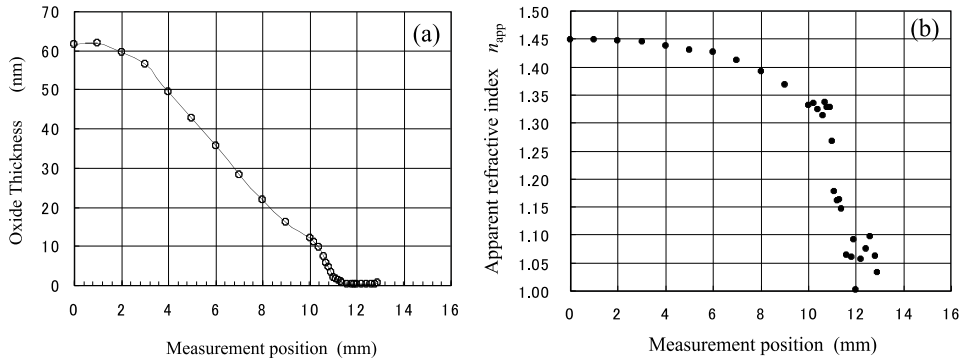

Figure 4. (a) Oxide thickness and (b) apparent refractive indices (λ = 630 nm) of a sloped oxide film on SiC along the slope [26].

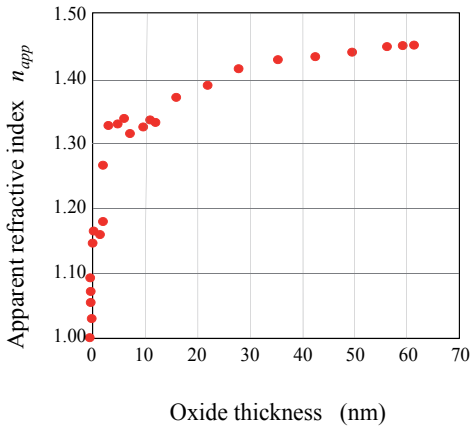

Figure 5. Thickness dependence of n_{app} of an oxide film on SiC at λ = 630 nm [26].

the interface between SiC and oxide layer. However, we have failed to explain the thickness dependences of n_{app} observed by the model taking into account the presence of the transition layer, the optical constants of which changes gradually from those of SiC to those of SiO_2.

Then, we attempted to obtain the optical properties of interface layers under the assumption of two-layers structure model, i.e., the structure of stoichiometric SiO_2 layer/interface layer/SiC substrates. Here, we assumed the presence of interface layers, not a transition layer but the layer having the wavelength dependence of the refractive indices of the interface layers that follows Sellmeier's dispersion law given by Eq. (1). We have used the optical constant of fused quartz for stoichiometric SiO_2. We have obtained the fitting parameters n_{inf} and λ_0 appeared in Eq. (1) and the thicknesses of interface layer and SiO_2 layer from the ellipsometry parameters measured as a function of wavelength. Figures 6(a) and (b) shows the values of the thicknesses of the SiO_2 layers and the interface layers, and the values of n_{inf} and λ_0, obtained at each measurement position, respectively. It is found from the figures that the thickness of

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the SiO_2 layer changes almost linearly along the slope, and the thickness and the parameters n_{inf} and λ_0 of the interface layers do not change but are almost constant over the positions measured. These results indicate that the thickness dependence of n_{app} in oxide films on SiC can be explained by changing the thickness of the SiO_2 layer only, which suggest that the SiO_2 layer lies on the interface layer having the refractive indices given by the Sellmeier's equation with the parameter values n_{inf} ~4 and λ_0 ~ 0.15 and the thickness ~1 nm. As the parameter n_{inf} in Sellmeier's equation indicates the refractive index at long wavelengths, this means that there exist interface layers, around 1 nm in thickness with the refractive indices higher than those of SiC and SiO_2 (n = 2.6 and 1.45 at λ = 630 nm, respectively). These results strongly suggest that the interface layers are not mixed layers between SiC and SiO_2, i.e., neither transition layers nor optically equivalent layer due to interface roughness.

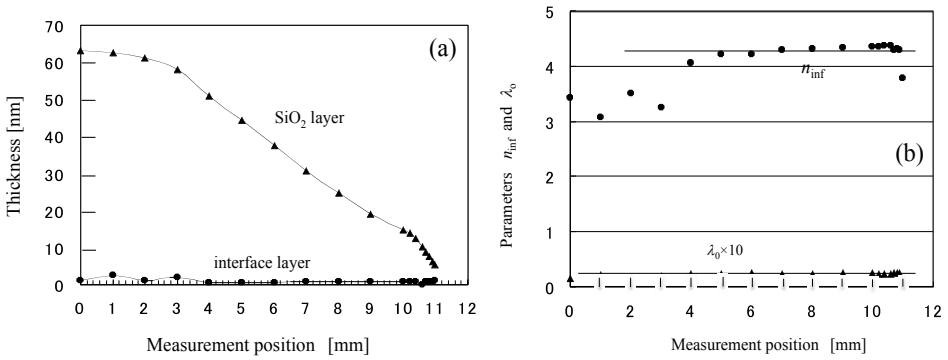

Figure 6. (a) Thicknesses of the SiO_2 and the interface layers, and (b) the Sellmeier's parameters n_{inf} and λ_0 of the interface layers as a function of the measurement position [26].

We have derived the refractive indices of the interface layers n_{it} as a function of wavelength on the assumption of the Sellmeier's dispersion law for refractive indices and the extinction coefficient k_{it} = 0. This is not self-explanatory in general. Then, we attempted to derive the optical constants of the interface layers at each wavelength from the measured (Ψ, Δ) values without using any assumption for optical constants [35]. The results reveal that the values of extinction coefficient are in the order of 0.1 though the values vary widely. The values of the refractive indices obtained at each wavelength almost agree with the values calculated from the values of n_{inf} and λ_0 obtained under the assumption of k_{it} = 0 and the Sellmeier's dispersion law for n_{it}. These results suggest that the assumption of the Sellmeier's dispersion law for n_{it} is also reasonable.

We have analyzed the interface layers for various formation methods of oxide, i.e., dry oxidation and low-temperature deposition of oxide (LTO), as well as pyrogenic oxidation. Dry oxidation was done in the pure oxygen flow at 1100°C for 16 h. Pyrogenic oxidation was done in a hydrogen-oxygen flame at 1100°C for 8 h. LTO films were deposited by low-pressure chemical vapor deposition (LPCVD) using SiH_4 and O_2 gases at 400°C and post-oxidation annealing (POA) in Ar atmosphere was performed at 1200°C for 1 h [36]. For all of the samples, the values of parameter n_{inf} and λ_0 are almost constant against oxide film thickness. Therefore,

the results of the ellipsometric measurements along the slope of the oxide films can be explained by two-layers mode mentioned above regardless of oxide formation methods. All the values of the refractive indices calculated using the values of n_{inf} and λ_0 obtained for three oxide films are higher than those of stoichiometric SiO_2 and bulk SiC. The values of n_{inf} depend on the oxidation process, and the values for LTO films are smaller than those for pyrogenic and dry oxidation, though the values of λ_0 are not different largely among these three layers.

From these results, we can conclude that there exist interface layers, having high refractive indices compared with those of SiC and SiO_2, the values of which depend on the oxide layer formation method, around 1 nm in thickness, at oxide/SiC interface and only the thickness of the SiO_2 layers changes with oxidation time or oxide thickness. It can be said that the optical properties estimated form the analysis using the single layer model mentioned in the previous section, i.e., the oxide films are assumed to be optically uniform single layer on SiC, are "apparent" features and it is not true that the optical constants of the oxide layers change with oxidation time or oxide thickness.

3. Characterization of the interfaces between SiC and oxides, and their relation to the electrical properties of MOS diodes

3.1. Characterization of the optical properties of interface layers between SiC and oxide

In the previous sections, it is said that the refractive indices of interface layers depend on the oxide layer formation process. For example, the values of n_{inf} for LTO films are smaller than those of pyrogenic and dry oxidation, while the LTO films are known to have lower interface state densities and effective oxide charge density than those of thermally oxidized films. Therefore, these results suggest the values of n_{inf} of the interface layers may be related to the electrical properties of SiC MOS structures in some extent. The large refractive indices evaluated suggest the existence of bonds with large polarization, like Si-Si bonds at the interface, which may influence on the electrical properties of the interfaces.

We have evaluated the oxide/SiC interfaces by spectroscopic ellipsometry measurements in the spectral range between 1.4 and 4.3 eV in Section 2. It has been reported in the studies on Si/oxide interfaces that the wavelength of optical constants in the absorption region, i.e., direct interband transition region, gives the information on a structural defect near the interfaces, such as oxide-induced stacking fault [37] and interface strain [5] because these defects bring about the shift of peaks corresponding to critical point. For Si, the absorption peak corresponding to E_1 (3.35eV) point locates in the visible to ultraviolet (UV) spectral range as shown in Figure 7 [38,39]. Therefore, the measurements in visible and ultraviolet spectral ranges can be reflected from the direct optical transition of Si. The band gap energy of 4H-SiC, for example, is 3.2 eV, which can be covered in the measurements mentioned above i.e., 250-850 nm or 4.96-1.46 eV. However, its absorption is very small up to around 4eV because SiC is an indirect energy bandgap semiconductor, and the absorption rises up near the direct transitions, for example, E_0 (5.65eV for 4H-SiC) [40]. Thus, the measurements including the deep UV (DUV)

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spectral range may be capable to give more information on the SiC/oxide interface structures. Therefore, to obtain the information on the properties in direct interband transition region, we have expanded the wavelength range of the spectroscopic ellipsometry to deep UV region, i.e., to 200 nm, or 6.0 eV, which covers the E_0 peak of 4H-SiC [28].

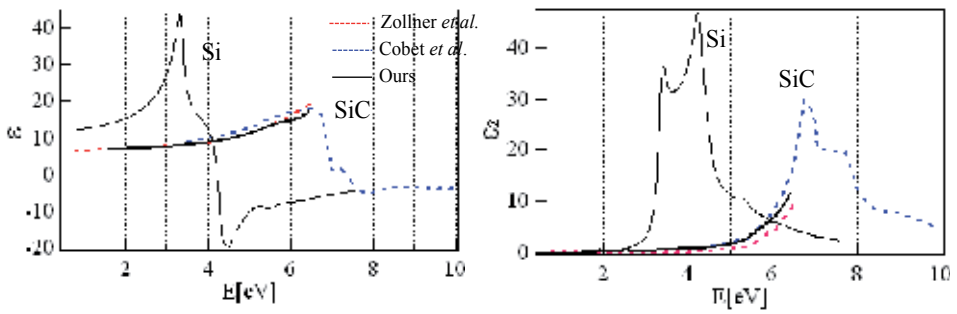

Figure 7. Photon energy dependences of the real and imaginary parts of dielectric constants for bulk Si and 4H-SiC [38,39].

Epitaxial wafers of 4H-SiC with 8° off-oriented (0001) Si-faces, n-types, were used in this study. A sample was oxidized at 1100°C in a dry oxygen atmosphere. By the oxidation for various time from 2.4 to 14.5 h, we obtained the oxide layers from 15.5 to 42.2 nm in thickness. The ellipsometric measurements were performed in the photon energy range between 2.0 and 6.0 eV. For the analysis of oxide layers on SiC, we used a two-layers structure model, i.e., the oxide layers are composed of a SiO_2 layer having the refractive indices for stoichiometric SiO_2 composition and an interface layer lain on SiC. Firstly, in the energy range between 2.0 and 4.0 eV, we evaluated the thicknesses of oxide layer and interface layer by fitting the calculated (Ψ, Δ) spectra to the measured values in this energy range. Here, we used the modified Sellmeier's dispersion relation, which takes into consideration of weak absorption, because the optical absorption of the interface is considered to be quite small in this photon energy range.

$$\varepsilon_1 = 1 + \frac{\left(n_{inf}^2 - 1\right)\lambda^2}{\lambda^2 - \lambda_0^2},\ \varepsilon_2 = \frac{C_1}{\lambda} + \frac{C_2}{\lambda^2} + \frac{C_3}{\lambda^3}, \tag{2}$$

where ε_1 and ε_2 are the real and imaginary parts of dielectric constant, respectively, n_{inf} and λ_0 are the refractive index of the wavelength at infinity, and the characteristic oscillation wavelength, respectively, and C_1, C_2, and C_3 are the fitting parameters for the optical absorption, so that we could obtain the thickness and optical constants of the interface layer as well as the SiO_2 layer thickness. After the determination of the SiO_2 and interface layer thicknesses in 2.0-4.0 eV range, by using these thickness values, the optical constants (n_{it}, k_{it}) of the interface layer were evaluated at each photon energy in the entire range from 2.0 to 6.0 eV from the ellipsometric parameters (Ψ, Δ) measured at the corresponding energies.

The thicknesses of the interface layers obtained are almost constant around 1 nm for all the oxide thicknesses measured. Figure 8 shows the photon energy dependence of n_{it}, and $k_{it,}$ of the interface layer at various oxide thicknesses from 15.7 to 42.2 nm. In the figure, the values of n and k for 4H-SiC are also shown by the red-colored lines. The values of optical constants in the range between 2 and 4 eV derived at each photon energy agree well with those obtained by use of the Sellmeier's relation determined by curve fitting in the same energy range. This agreement indicates that the structural model used in the analysis of ellipsometric data is appropriate. The figure suggests that the photon energy dispersion of n_{it} is quite similar to that of SiC, though the absolute values are around 1 larger than those of SiC, and slightly decreases with oxide thickness, and the differences between the interface layer and SiC tend to increase with photon energy. The photon energy dispersion of k_{it} is seen to be quite similar to that of SiC in entire energy range, i.e., nearly zero below 4 eV and a rise at around 5 eV.

The experimental results can be summarized as follow. There exists an interface layer of about 1 nm in thickness, though the absolute values of refractive index are 0.5-1 larger than that of SiC. The optical constants of the interface layer have similar energy dispersion to those of SiC in the photon energy range from 2.0 and 6.0 eV. These results indicate the existence of an interface layer, the material of which has a similar band structure as that of SiC. This leads the conclusion that the interface layer is not the transition layer between SiC and SiO_2, but a material having the modified structure and/or composition from SiC.

In the case of the thickest oxide sample, the energy where k_{it} rises up is smaller than that of bulk 4H-SiC. Nguyen et al. [5] evaluated the photon energy dependence of the dielectric constants of the interface layers for Si and found a red shift of 0.042 eV of the interband critical point E_1 (3.35eV) compared with the bulk silicon values, and concluded there exists a strain layer of Si by the compressive stress due to the lattice expansion by oxidation, as well as the layer due to rough interface or transition of composition less than 0.7 nm in thickness. Our result of the increase of k_{it} in the deep UV region for the thickest oxide of SiC can be explained by the red shift of E_0 peak of SiC due to the increase of interfacial strain accompanied with oxidation, because the expansion of Si bond due to oxidation is expected also for SiC.

We will discuss on the formation mechanisms and the structures of interface layers in Sections 4 and 5, relating with the oxidation mechanisms of SiC.

3.2. Relation between the optical and electrical properties of interface layers

i. Performance of spectroscopic ellipsometry measurements and *C*-*V* measurements on the same samples

It is found that there exist interface layers around 1 nm in thickness and the refractive indices n_{it} depend on the oxidation conditions, i.e., oxidation method and oxidation temperature, which suggests that the values of n_{it} may reflect the change of the interface structures to some extent. Under these considerations, we have tried to investigate SiO_2/4H-SiC interfaces by using capacitance-voltage (*C*-*V*) measurements and FTIR spectroscopy, in parallel with spectroscopic ellipsometry measurements [41]. In the cases of the oxide layers formed by dry oxygen, we found high densities of interface trap, larger shift of *C*-*V* curve along the gate

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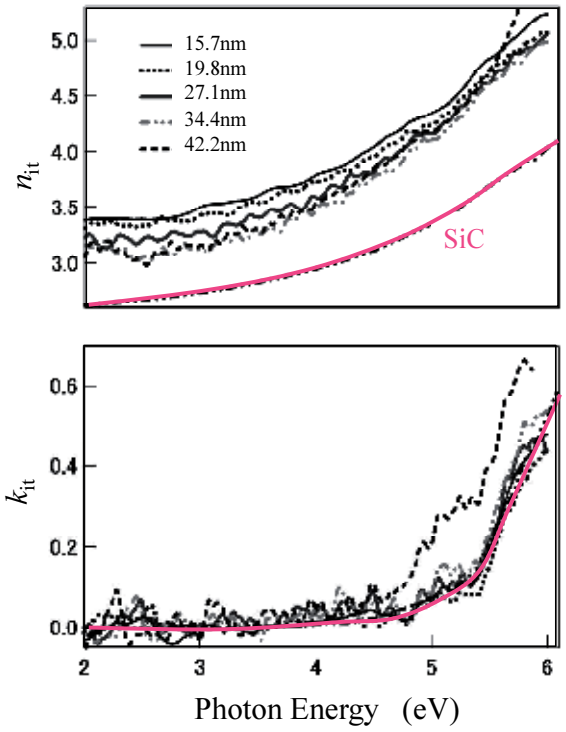

Figure 8. The photon energy dependences of optical constants, n_{it} and k_{it}, of the interface layers at various oxide thicknesses for oxide films on Si-face of 4H-SiC by dry oxidation [28].

voltage axis and large leakage current from *C-V* measurements. FT-IR measurements suggest lower vibration frequency of the Si-O-Si stretching mode compared to that of fused quartz.

Based on these preliminary results, we have performed systematic studies on the SiC-oxide interfaces fabricated by various oxidation methods grown on SiC (0001) Si- and (000-1) C-face surfaces to make clear the relation between the refractive indices of interface layers derived from spectroscopic ellipsometry measurements and the interface sate densities derived from *C-V* measurements [27]. *C-V* measurements were performed on the same samples used in the ellipsometric measurements for the purpose of direct comparison between optical and electrical characteristics. Based on the results obtained, we have discussed on the structures of SiC/oxide interfaces related to the interface states which degrade the electrical properties of SiC-MOS structure, like channel mobility of the carriers.

For optical measurements, we have evaluated the refractive indices of the interfaces n_{it} from the ellipsometric measurements by the analytical methods mentioned in the previous section as well as the results from XPS measurements [42]. To keep high sensitivity in the measurements over the wide photon energy range, i.e., wide spectral range from deep UV to visible range, the measurements were carried out at the different angles of incidence of 70° and 75° for 1.5-2.0eV and 2.0-6.4 eV, respectively. For electrical measurements, we have performed

high-frequency *C-V* measurements at 1 MHz for the same samples used in the optical measurements to evaluate interface state density D_{it} by way of the Terman method.

These optical and electrical measurements using same samples have been carried out for the oxides grown on SiC with various growth conditions, i.e., dry and wet oxidation at 1000°C and 1100°C for Si-face, and dry oxidation at 900, 1000, and 1100°C, and wet oxidation at 900, 950, and 1000°C for C-face, as well as the samples with post-oxidation annealing. By using the results obtained from the measurements, we have compared the growth condition dependences of optical and electrical properties, i.e., refractive indices of interface n_{it} and interface trap density D_{it} to make clear the correlation between n_{it} and D_{it}.

ii. Dependences of n_{it} and D_{it} on oxidation temperature, oxide method, and surface polarity

Figures 9 and 10 show the values of optical constants n_{it} and k_{it} as a function of photon energy, and D_{it} as a function of energy from the Fermi levels, for Si-face and C-face, respectively, oxidized by wet and dry oxidation at various oxidation temperatures. It is found from Figure 9 that the values of n_{it} and D_{it} for wet oxidation are both larger than those for dry oxidation, and both change little with oxidation temperature for Si face. While for C-face, as seen in Figure. 10, the values of n_{it} and D_{it} for dry oxidation are both larger than those for wet oxidation, and both change remarkably with oxidation temperature and increase with increasing oxidation temperatures for dry oxidation. Contrary, for wet oxidation, D_{it} increases with increasing temperature as in the case of dry oxidation, but n_{it} increases, i.e., the oxidation temperature dependences of n_{it} has opposite tendency for dry oxidation. These results are summarized in Tables 1(a) and (b) for temperature, surface polarity and oxidation method dependences. We have found that the growth condition dependences of n_{it} are well corresponding to those of D_{it}, though the case of C-face oxidized by wet oxidation is an exception. The reasons of this exception have been discussed elsewhere [27], comparing with the researches on the oxidation temperature and oxidation method dependences of D_{it} reported [36, 43-45].

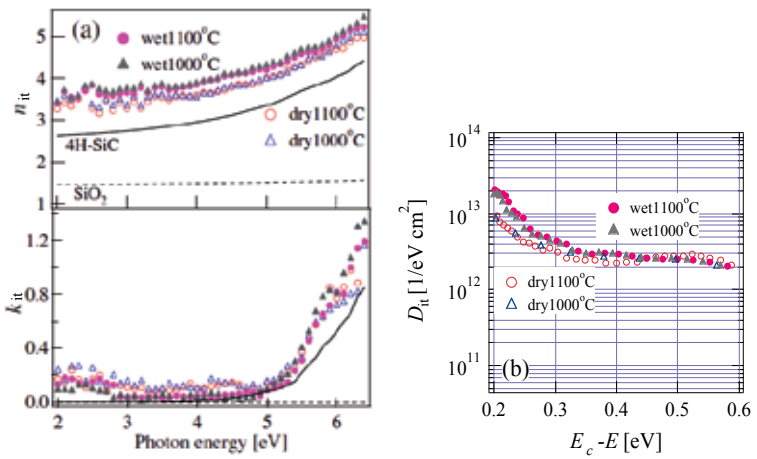

Figure 9. Refractive index, n_{it}, and extinction coefficient. k_{it}, of the interface layer (a), and interface states density D_{it} (b), for Si-face. The solid and broken lines in (a) show the optical constants of SiC and SiO_2, respectively [27].

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The differences in D_{it} for oxidation method, surface polarity and oxidation temperature have been reported by many researchers and the origins have been studied by use of, for example, XPS [46] and EPR [47].

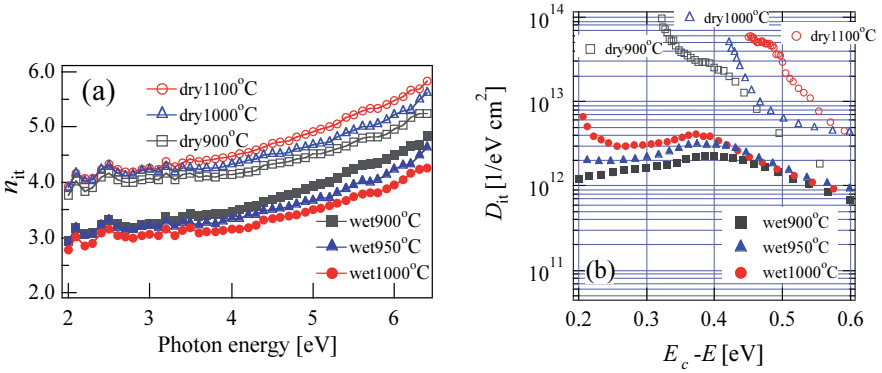

Figure 10. Refractive indices of the interface layer n_{it} (a), and interface states density D_{it} (b), for C-face [27].

(a) Temperature dependences

polarity	Si-face	C-face
dry oxidation	small change	small change
wet oxidation	increase	decrease

(b) Oxidation method and polarity dependences

Si-face·dry	<	C-face·dry
∧		∨
Si-face·wet	>	C-face·wet

Table 1. Oxidation temperature (a) and oxidation method and polarity dependences (b) of both the refractive indices of interface n_{it} and interface state density D_{it}

iii. Effect of post-oxidation annealing on n_{it} and D_{it} for wet oxidation

To understand the differences in n_{it} and D_{it} by oxidation method, we have performed post-oxidation annealing (POA) in Ar and O_2 atmosphere at 600°C for 3 h for wet oxidation samples based on the results reported [25]. Figures 11 and 12 show n_{it} and D_{it} values for Si- and C-face, respectively, with and without POA. The figures reveal that, for both polarities, the values of n_{it} and D_{it} come close to those for dry oxidation by POA. From these, it is considered that as grown samples by wet oxidation, hydrogen-related species terminate the dangling bonds of Si or C at the interface, and then they are removed by POA, which brings about the interface characteristic close to those for dry oxidation. The changes by annealing in oxygen and argon atmosphere are almost the same with each other for Si-face. Contrary, for C-face, the changes by annealing in oxygen are much larger than that in argon atmosphere, which is considered to be due to the oxidation even at around 600°C for C-face.

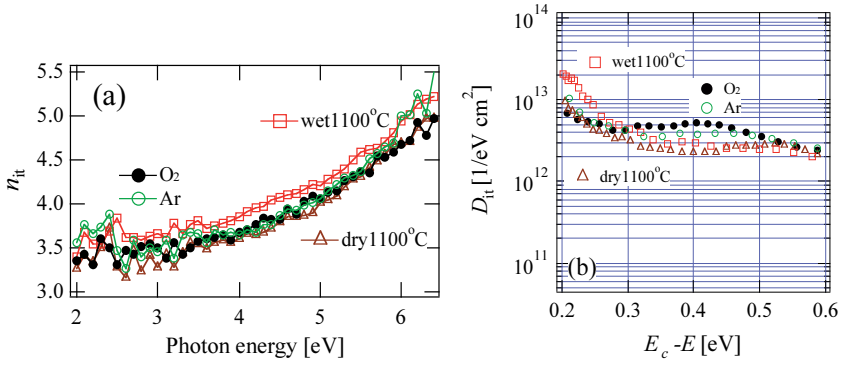

Figure 11. Changes in n_{it} (a) and D_{it} (b) on Si-face by POA for wet oxidation [27].

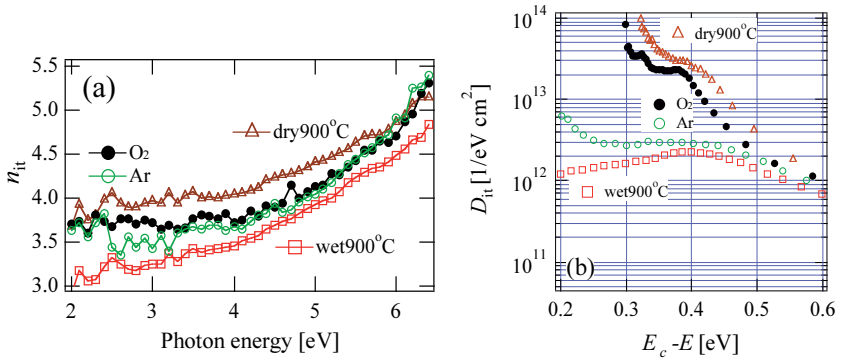

Figure 12. Changes in n_{it} (a) and D_{it} (b) on C-face by POA for wet oxidation [27].

iv. Effect of the change in oxidation rate on n_{it} and D_{it} for C-face

In Figures 9 and 10, the measurements were performed on the samples oxidized at the same temperatures for Si- and C-faces to know the surface polarity dependences of n_{it} and D_{it}. It is well known that the oxidation for C-face is around 10 times faster than that for Si-face. Therefore, these results were obtained from the oxides with different oxidation rates for C- and Si-faces. Then, we have prepared oxide films grown with same growth rate to avoid the influence from the growth rate to polarity dependence. The oxidation rate for C-face at 850°C is reported to be almost same as that for Si-face at 1100°C. The values of n_{it} and D_{it} for dry oxidation of C-face at various oxidation temperatures between 800°C and 1100°C as well as those of Si-face at 1100°C are shown in Figure 13. It is found from the figure that the differences i*n* n_{it} and D_{it} between the oxides for C-face at low temperatures and those for Si-face grown at 1100°C considerably reduce with decreasing oxidation temperature, which suggests that the lowering in the oxidation rate is quite effective for reducing n_{it} and D_{it} values. However, the method of changing oxidation temperature is possible to result in the change of the oxidation reaction process. Therefore, we have prepared the samples for C-face oxidized at the same temperature, 900°C, but with low oxygen partial pressure between 0.4 and 0.6 atm. However,

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similar tendency in the case of decreasing oxidation temperature for the values of n_{it} and D_{it} were obtained [27].

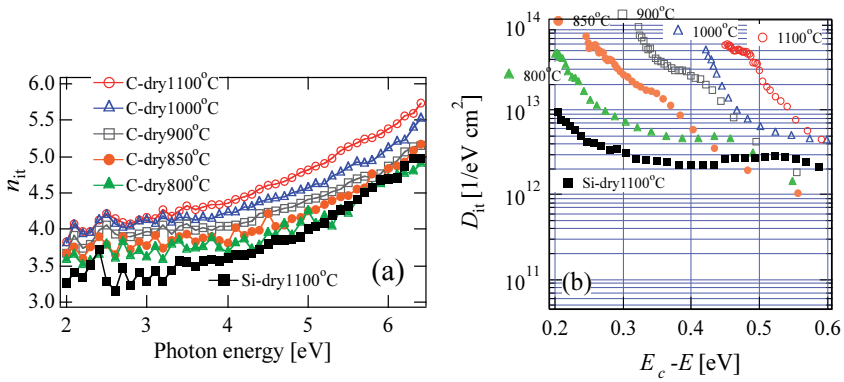

Figure 13. The values of n_{it} (a) and D_{it} (b) on C-face at oxidation temperatures between 800°C and 1100ºC [27].

v. Verification of the correlation between n_{it} and D_{it} of interface layers by γ-ray irradiation

We have found the refractive indices of interface layers measured by spectroscopic ellipsometry correlate well with the interface state density estimated by *C-V* measurements. To verify this correlation quantitatively, it is necessary to perform quantitative comparison between the changes of the interface state density and the refractive indices of the interfaces. It is well known that γ-lay irradiation brings about the increase of interface state density. Therefore, the quantitative correlation between the change in the refractive indices and interface state densities can be studied by performing *C-V* and ellipsometric measurements using the samples increased in interface state density artificially by γ-ray irradiation.

We have prepared the samples, interface state density of which were increased by γ-ray irradiation, and, for these samples, we have performed *C-V* and ellipsometric measurements before and after γ-ray irradiation [48]. Si-face of 6H-SiC with epilayers, 5 μm in thickness and n-type, 5×10^{15}cm^{-3} were used. The epilayers were oxidized at 1100°C for 2 h by pyrogenic oxidation method to form oxide layers, around 30 nm in thickness. The ellipsometric measurements were carried out for the slope-shaped oxide films formed by gradually immersing the samples into BHF solution at a constant speed. After the optical measurement, the oxide layers were removed. Then, the samples were oxidized again, and Au and Al electrodes for gate and ohmic contacts, respectively, were formed on oxide layer and back surface of SiC substrate to form MOS diodes.

After *C-V* measurements, the samples were subjected to ^{60}Co γ-ray for various duration times from 1 to 38 h (0.4-14.7 kC/kg with the rate of 2.58-3.87×10^{2}C/kg h) at room temperature, and again *C-V* measurements were carried out. Finally, after the electrodes were removed, slope-shaped oxide films were formed and ellipsometric measurements were carried out. Optical analysis is the same as in the cases of that mentioned in the previous sections, i.e., using two-layers model composed of a SiO_2 layer and an interface layer on SiC. The values of n_{inf} and λ_0

parameters appeared in the Sellmeier's dispersion equation Eq. (1) for the interfaces of samples before and after γ-ray irradiation were measured.

The results reveal the values of n_{int} increases, while that of λ_0 show little change by γ-ray irradiation, i.e., the refractive indices of interface layer increase by γ-ray irradiation. The changes in the value of n_{inf}, Δn_{inf} and interface state density, ΔN_{it}, are plotted as a function of absorption dose, where N_{it} (cm^{-2}) is the integration of D_{it} ($eV^{-1}cm^{-2}$) by energy, and are shown in Figure 14 (a). Figure 14 (b) shows the relation between Δn_{inf} and ΔN_{it}. The figure shows there exists a strong correlation between them, almost linear relation, though the data points are not so much. This result suggests the values of refractive indices of interface obtained from ellipsometery measurements are well reflected from the electrical properties of interface, like interface state density. Finally, it should be noted about the influence of γ-ray irradiation to the SiO_2 layers. We have confirmed that the influence on the derivation of the refractive indices of the interface layers by the change in refractive index of SiO_2 layer by γ-ray irradiation, around 0.02, is small enough to neglect.

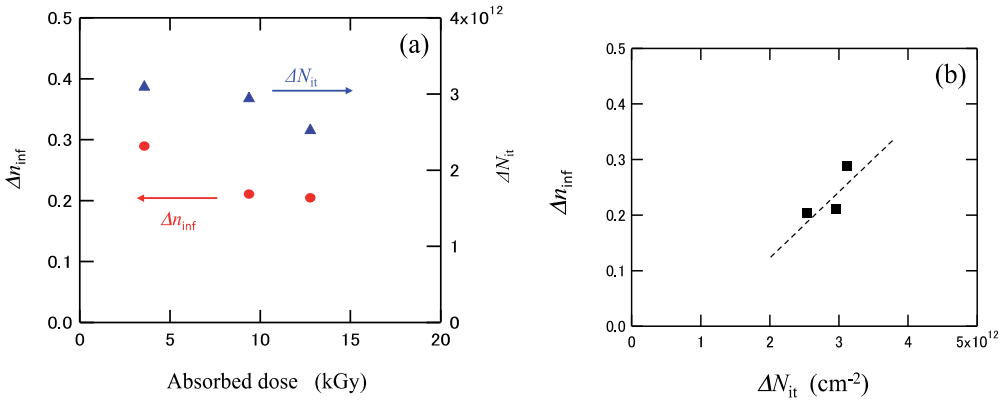

Figure 14. (a) Changes in n_{inf}, Δn_{inf} and interface state density, ΔN_{it}, as a function of γ-ray absorption dose, and (b) the relation between Δn_{inf} and ΔN_{it}.

4. Real-time observation of SiC oxidation

4.1. Real-time observation of SiC oxidation using an in situ spectroscopic ellipsometer

We have found that, in the thermal oxides on SiC, there exist interface layers, around 1 nm in thickness, with the optical constants having similar energy dispersion with SiC, though absolute values of refractive indices are around 1 higher than that of SiC. And, we also found that the values of refractive indices correlate well to the interface state density. As the interface structures may form during the oxidation, the interface structures should be closely related to oxidation mechanisms of SiC, and therefore, it is necessary to study the oxidation mechanisms to know the formation mechanism of the interface layer i.e., to make clear the origin of interface layers observed, which may lead how to reduce the interface state density at the SiC-oxide interface. Therefore, in order to elucidate the origin of the interface states, it is also important

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to know the mechanism of SiC oxidation, especially at the initial stage of oxidation. For these requirements, the precise measurements of oxidation rate, especially in very thin-thickness regime, are indispensable. Many studies have been performed on the oxidation time dependences of oxide films of SiC by use of various methods, including spectroscopic ellipsometry for various SiC polytypes [15-18,20]. In these studies, however, the measurements were performed after the oxidation, i.e., *ex-situ* measurements, where accurate oxide thickness as a function of oxidation time cannot be obtained because the oxidation proceeds even during rising and dropping in substrate temperature. Especially in small thickness range, i.e., the initial oxidation stage, this inaccuracy may bring about the difficulty in the precise study on the oxidation process. Therefore, to study on the mechanism of SiC oxidation in more detail, especially in initial stage of oxidation, a real-time observation technique is indispensable.

We have developed an in situ ellipsometric measurement system, composed of a lamp-heated furnace and a spectroscopic ellipsometer (SOPRA,GESP5), to observe the SiC oxidation in real time. The details of the system are described elsewhere [29]. Figure 15 (a) illustrates schematically the in situ spectroscopic ellipsometer we designed. The furnace has two optical windows for incident beam and reflected light beam from the sample surface for ellipsometric measurements. The fused quartz glass windows are angled so that the surfaces of the window glass are normal to the incident and reflected beams, i.e., inclined ±15° from the normal direction of the sample surface, to perform the ellipsometric measurements at an angle of incidence of 75°. The samples were heated up to a prescribed temperature between 600°C and 1200°C by the IR beam from a halogen lamp focused on the sample surface through the guiding quartz rod. The temperature of the samples was measured by using an IR radiation thermometer. The furnace was evacuated by a turbo molecular pump down to 2×10^{-6} Pa and Ar gas was introduced into the chamber during the measurement of optical constants of SiC substrate before oxidation at the oxidation temperature. Oxidations were performed by introducing dry oxygen and wet oxygen for dry and wet oxidations, respectively.

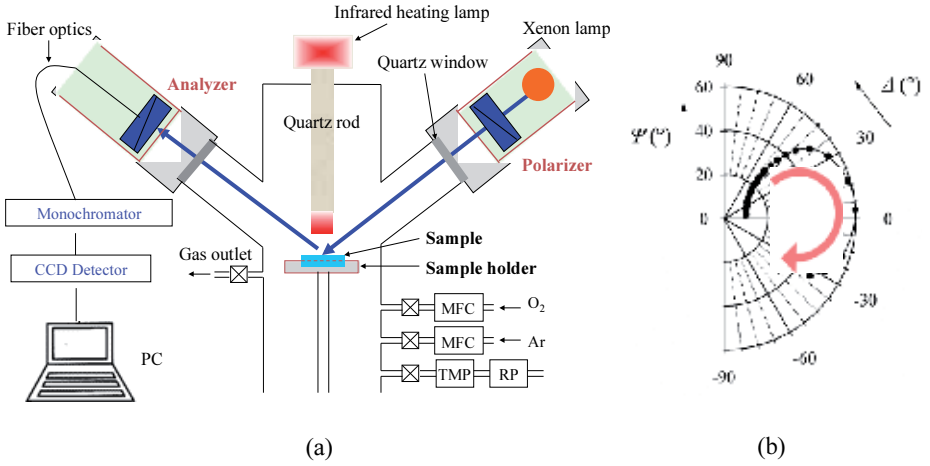

Figure 15. (a) Schematic diagram of the in situ spectroscopic ellipsometer we designed, and (b) an example of the observed values of (Ψ, Δ) over the oxidation time range from 5 min to 6 h in the case of the oxidation temperature 972°C. The values of Ψ and Δ are plotted in the radius and angle in this pole figure, respectively.

Figure 15 (b) shows an example of the observed values of (Ψ, Δ), plotted on a pole figure coordinate, over the oxidation time range from 5 min to 6 h at 972°C. The experimental points (Ψ, Δ) move clockwise with oxidation time. It should be noted the merit of pole figure, i.e., Ψ and Δ are shown by the radius and angle, respectively. Comparing with a right angle coordinate, there is no jump but connected at 0° and 360° or 2π in Δ, and the figure reveals that the precision of Δ depends on the absolute values of Ψ.

We have carried out real-time *in-situ* measurements at various growth temperatures between 893°C and 1147°C. The oxide thicknesses are plotted as a function of oxidation time in Figure 16. Compared with the previously reported results obtained from *ex situ* measurements [15,18], it is found from the figure that the data during the initial oxidation stage were obtained with much improved detail and much smaller spread.

For Si thermal oxidation, Deal and Grove [1] have considered two rate-determining processes, i.e., the reaction process at the interface and the process of oxygen diffusion through the oxide layer, and proposed, so-called, D-G-model, given as,

$$X^2 + AX = B\left(1 + \tau\right) \tag{3}$$

where, X, t and τ are the oxide thickness, oxidation time, and initial oxidation time, respectively. B/A and B are denoted as the linear and parabolic rate constants of oxidation, respectively. Many researchers have applied D-G model to explain SiC oxidation [15, 18]. We also applied the D-G model to the results obtained from in situ ellipsometric measurements. The fitted curves derived using Eq. (3) are shown by the broken lines in Figure 16, which reveals that the fits are good at all the oxidation temperatures in our experiments. However, there is a discrepancy between the values of B/A and B obtained in this study and those reported by, for example, Song et al. [18], who modified D-G model for Si oxidation to that for SiC by taking into account the presence of carbon, i.e., adding the out diffusion process of CO from the interface to the surface. One of the reasons of this discrepancy is considered to be the difference of measurement method, i.e., the *ex-situ* measurements performed after the oxidation have been used in the previously reported studies, while we used *in-situ* real-time measurements and thus, the relations between oxide thickness and oxidation time can be precisely obtained. The reasons of these discrepancies in the values of rate constants appeared in D-G model between ours and those by Song et al. have been discussed in details by Goto et al. [49] with the relation of the oxide growth rate enhancement in thin thickness regime for SiC oxidation.

4.2. Oxide growth rate enhancement of SiC in thin oxide regime

In the previous section, we mentioned that real-time observation of SiC thermal oxidation using an *in-situ* ellipsometer has been performed for the first time and shown that the results are well explained by the D-G model. However, it has been reported that the oxidation behavior of Si in thin oxide thickness range cannot be explained using the D-G model, where the oxide growth rate enhancement has been found. Therefore, we have studied the initial oxidation stage of SiC in more details to make clear such an oxide growth rate enhancement occurs also for SiC or not.

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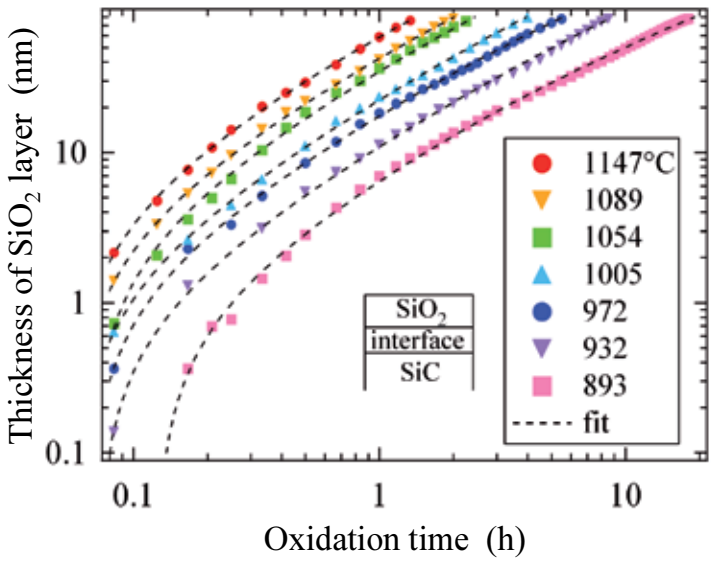

Figure 16. Oxide thickness as a function of oxidation time at various oxidation temperatures. The broken lines show the fitting curves by use of D-G model [29].

In the study mentioned in Section 4.1, the real-time measurements of (Ψ, Δ) were performed at the single wavelength λ = 400 nm. In order to observe the oxidation in initial oxidation stage, i.e., to elucidate the oxidation process and interface layer formation in more detail, we have undertaken the spectroscopic observation of SiC oxidation by using a CCD detector. We have performed the measurements of oxidation rate in thin-thickness regime both for C- and Si-faces of 4H-SiC by in situ real-time observation using a spectroscopic ellipsometer with CCD detector [30,31,50].

Ellipsometric measurements were carried out at wavelengths between 310 and 410 nm, where we can perform the ellipsometric measurements without the disturbance by the strong light emission from the heated sample. We have derived the thickness of oxide layers as a function of oxidation time by using the same analytical method mentioned in the previous sections.

Firstly, we have applied the D-G model to the results obtained at various oxidation temperatures. Though the fits are seen in general well over the wide thickness range in the thickness range of thinner than around 20 nm, it was found there exists a tendency for the observed values to be slightly larger than the calculated ones by using the D-G model. To see these discrepancies in more detail, we have derived the oxidation rates dX/dt from the observed curves of oxide thickness X(t).

Figure 17 shows the oxide thickness dependences of oxidation rate for C-face and Si-face. The figures reveal that the values of the oxidation rate including the thin thickness range of less than 10 nm can be obtained by real-time in situ spectroscopic observation. However, the figures also suggest that the oxidation rates calculated using the D-G model cannot be fitted to the

observed ones over the entire oxide thickness range at all the oxidation temperatures measured, though the fitting is well in the range thicker than around 20 nm for C-face and several nm for Si-face, as shown by the solid lines in Figure 17(a). While, in the thin thickness region, the oxidation rates are larger than the values calculated by use of the D-G model regardless of oxidation temperature. These results reveal that the oxidation having a larger growth rate than that predicted by the D-G model occurs in thin-thickness range, though the critical thickness is different between C-face and Si-face.

By the D-G model, the relation between the growth rate dX/dt and the oxide thickness X is given [1] as,

$$\frac{dX}{dt} = \frac{B}{A + 2X}. \tag{4}$$

In small thickness range, i.e., X<<A, the oxidation is limited by the reaction rate at the interface, and the growth rates are constant, equal to B/A from Eq.(4). However, the experimental results shown in Figure 17(b) reveal that, the growth rates are not constant but increase with decreasing oxide thickness in small thickness range. These experimental results for C- and Si-face suggest that the oxidation enhancement occurs regardless of surface polarity.

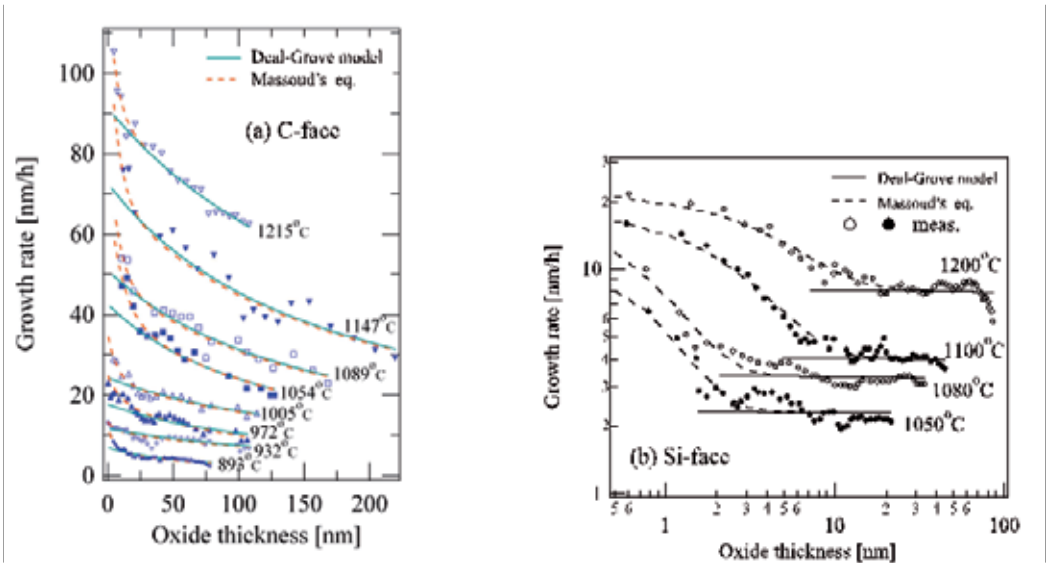

Figure 17. Oxide thickness dependences of oxide growth rates at various oxidation temperatures for (a) C-face, and (b) Si face [30,31].

4.3. Application of Massoud's empirical equation to SiC oxidation

Many researchers have tried to explain the oxide growth rate enhancement in thin-thickness regime for Si oxidation [4,51-54]. Massoud et al. [4] have proposed an empirical equation giving

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the oxidation rate as a function of oxidation thickness by adding an exponential term to the D-G equation, as,

$$\frac{dX}{dt} = \frac{B}{A + 2X} + C\exp\left(-\frac{X}{L}\right), \tag{5}$$

where C and L are the pre-exponential constant and the characteristic length, respectively.

We have tried to fit the calculated values to the observed ones by use of Eq. (5) for both Si- and C-faces. In all the oxidation temperatures, much better fittings than those using Eq. (4) were obtained, as shown by the broken and solid lines, respectively, in Figures 18 (a) and (b). From the curve fitting, the values of L as well as C, B/A and B were derived. Both for Si- and C-faces, the values of L scarcely depend on the oxidation temperature, around 7 nm, the behavior of which is almost the same as that for the oxidation of Si [4]. These results suggest that oxidation enhancement is predominant when oxide thickness is smaller than around 7 nm for both faces of SiC and Si oxidations.

i. Temperature dependences of oxidation rates

We discuss the temperature dependences of the four parameters B/A, B, C, and L below. Figure 18(a) shows the Arrhenius plots of the linear rate constant B/A for C-face and Si-face. The B/A values for C-face are one order of magnitude larger than those for Si-face at all the temperatures measured, which corresponds well to the experimental results that the growth rate of C-face is about 10 times larger than that of Si-face. The figure suggests that the values of B/A for Si-face lie on a single straight line having the activation energy of 1.31 eV, while for C-face the values lie on two straight lines the breaking point of which is around 1000°C. The activation energies for the higher and the lower temperature ranges are 0.75 and 1.76 eV, respectively. In this experiment, the growth rates of SiC for oxide thickness smaller than around 100 nm were measured. Therefore, we do not discuss the temperature dependences of the values of B here because of insufficient precision in determining the parabolic rate constant B without data for more thick oxide.

The values of $C/(B/A)$ are around 2-6 for Si-face, but for C-face smaller than 1. As the values of $C/(A/B)$ give the magnitude of oxide growth enhancement, the growth rate enhancement phenomenon is suggested to be more marked for Si-face than for C-face. The Arrhenius plots of the parameters C and L are shown in Figure 18(b). The figure reveals that the values of C for Si-face are almost independent of temperature, but those for C-face increase with the increase of temperature. While for the values of L, that for C face reveals little dependence on temperature, but that for Si-face steeply increase with temperature. The absolute values of L for Si face and C-face are around 3 and 6 nm, respectively, at 1100°C. It is found from the figure that the temperature dependences of C and L are different between Si-face and C-face of SiC. For Si oxidation, in comparison, it has been reported that L are around 7 nm and almost independent of temperature, and the values of C increase with temperature [4], which are the same for SiC C-face, but different for SiC Si-face. From these results, it can be said that the

oxidation mechanism of SiC C-face is similar to that of Si in some sense, while that of SiC Si-face is quite different from that of Si.

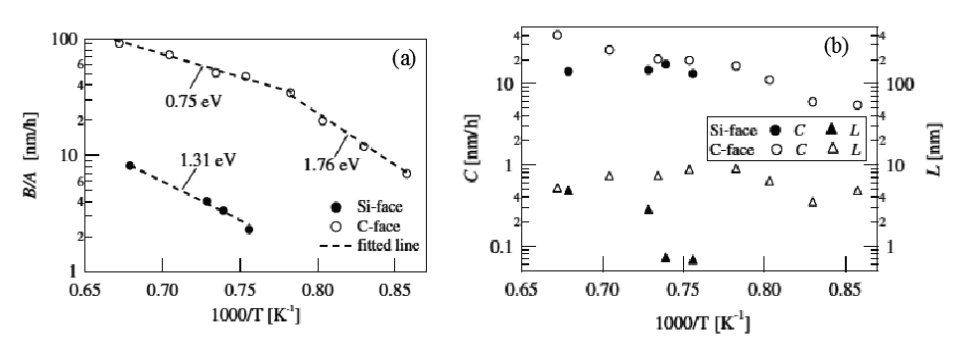

Figure 18. Arrhenius plots of the linear rate constant *B*/*A* (a), and *C* and *L* (b), for C- and Si-faces [31].

ii. Oxygen-partial-pressure dependence of oxidation rates

In the previous section, we have studied the temperature dependences of oxidation rate. Another parameter to control the oxidation rates is the quantity of oxygen supplied to the interface. Therefore, we have studied the pressure dependence of oxidation rate. Especially at reduced pressure, the oxidation rates become small, which is good to observe the initial oxidation stage in details.

Figures 19(a) and (b) show the oxide thickness dependence of oxide growth rate at various oxygen partial pressures for C- and Si-face, respectively. These figures reveal that the oxide growth rate enhancement occurs at any partial pressure, as in the cases at 1 atm. Figures 20(a) and (b) show the oxygen-partial-pressure, *p*, dependence of the values of the linear rate constant *B*/*A* and the enhancement parameters *C* and *L* for C-face and Si-face. It is found from Figure 20(a) that the values of *B*/*A* behave similar pressure dependences for both surface polarities, as ~ $p^{0.6}$. The D-G model [1] leads the results that *B*/*A* and *B* are proportional to *p*, which contradicts to our results, as well as for Si oxidation, i.e., ~ $p^{0.7\text{-}0.8}$ [4]. We have already reported that the value of *B* for both Si- and C-faces is proportional to *p* [50], which also contradicts to the prediction from D-G model. Figure 20(b) shows the variations of the values of *C* and *L* with oxygen pressure for Si- and C-faces. It is found from the figure that those values for both surface polarities are almost constant with respect to pressure, which is different from the pressure dependence of the values of *B*/*A* and B. The fact that the enhancement parameters *C* and *L* are independent of pressure, which is quite different from those for *B*/*A* and *B* values, suggests the existence of an additional oxidation-rate-limiting mechanism, which is independent of the quantity of oxygen supplied, other than the interface reaction of oxygen with SiC (*A*/*B*) and the diffusion of oxygen and CO through SiO_2 layers (*B*).

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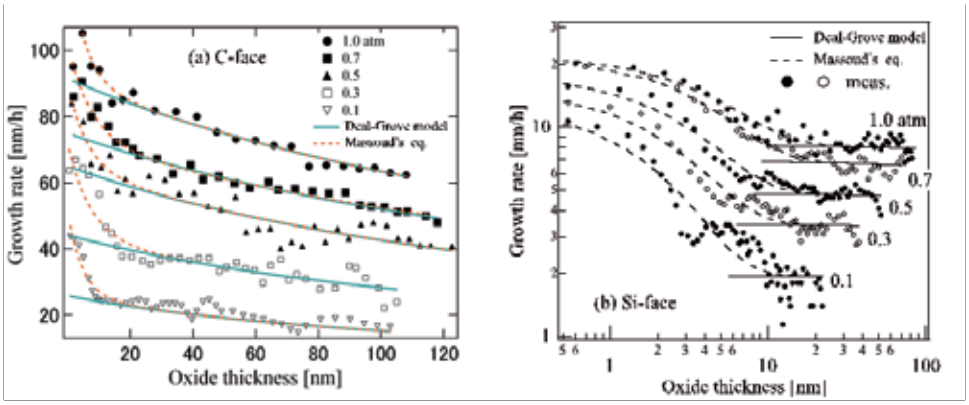

Figure 19. Oxide thickness dependences of oxide growth rates at various oxygen pressures for (a) C-face, and (b) Si-face [31,50].

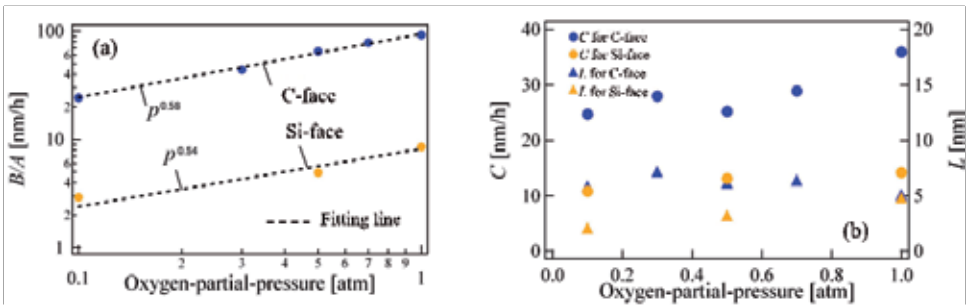

Figure 20. Oxygen pressure dependences of the values of the parameters, *B*/*A*, *C*, and *L* for C- and Si-faces [31].

5. Studies on the SiC oxidation process and interface formation based on SiC oxidation mechanisms

In the previous sections, we have studied SiC oxidation process by use of in situ real-time observation using automatic spectroscopic ellipsometry and found the oxidation rate enhancement in very thin-thickness regime, for the first time, which cannot be explained by using the D-G model. Then, we have applied Massord's equation proposed for the growth rate enhancement for Si, and discussed the oxidation temperature and oxygen partial pressure dependences of the parameters appeared in the equation. However, the Massord's equation was derived without considering any physical and/or chemical mechanisms of Si oxidation, i.e., the equation was derived for fitting to the experimental results on the oxide thickness dependence of growth rate. Therefore, the Massourd's equation (Eq.(5)) is one of the empirical equations, and thus, it may not be appropriate to discuss the physical or/and chemical meaning from the results of the nature of parameters in the equation.

Growth rate enhancement has been observed also for Si oxidation in thin-thickness regime. Kageshima et al. [52] and Uematsu et al. [55] have proposed the model for Si oxidation, called "interfacial Si emission model", where Si atoms are emitted into the oxide layers as well as into Si substrate, owing to the strain that arises from the expansion of Si lattices to form SiO_2 lattice. By the interfacial Si emission model, the oxidation rate at the interface is primarily large and becomes suppressed by the accumulation of emitted Si atoms near the interface with the progress of oxidation. This means that the oxidation rate never enhances in small thickness range but rapidly decreases with the increase of oxide thickness.

The interfacial Si emission model suggests that the stress near/at the oxide-Si interface originated from the formation of SiO_2 lattice brings about the growth enhancement in the initial oxidation stage. The density of Si atoms in SiC (4.80×10^{22} cm^{-3}) [56] is almost equal to that in Si (5×10^{22} cm^{-3})[57], which may bring about almost identical situation for SiC oxidation as in the case of Si oxidation. Therefore, it can be considered that the interfacial emission of atoms caused by the interfacial stress also brings about the growth enhancement in SiC oxidation. Based on these considerations, we have proposed the model, called "interfacial Si-C emission model", taking into account the presence of carbon in SiC to explain the experimental results for SiC oxidation reported [33],

As the formation of interface structures is considered to be closely related with the initial oxidation process, we have studied initial oxidation of SiC in more detail at reduced oxygen partial pressers, and discussed on the formation process of the interface layers in terms of SiC oxidation mechanism in ultra-thin-thickness regime. Though the oxide growth rate of SiC is much smaller than that of Si, it is still too fast to observe the initial growth process in detail. Therefore, a reduction in the growth rate, for examples, by lowering oxidation temperature, and/or lowering the oxygen partial pressure, is believed to be useful for observation of the initial oxide growth process of SiC more minutely. To make clear the oxygen partial pressure dependence of the SiC oxidation process, ex situ measurements have been carried out at the pressures from 10^{-3} to 4 atm [16,19]. However, the initial oxidation process has not been examined in detail, partly due to the limit of the precision of the data obtained by ex situ measurements in small thickness regime.

5.1. Observation of SiC oxidation in ultra-thin oxide regime at low temperatures

We have studied SiC oxidation at low temperatures or under reduced oxygen pressure in detail by performing in situ and real-time spectroscopic ellipsometry in ultra-thin oxide thickness regime [58]. Figures 21(a) and (b) show the oxidation time dependences of the thicknesses of SiO_2 and interface layer for the oxidation at 850° and 700°C, respectively, in the oxygen pressure of 1 atm. At 850°C, both the interface layer and the SiO_2 layer thicknesses increase with time, but the thickness of interface layer is saturated at about 1 nm by the oxidation time more than 2 h though the continuous increase in SiO_2 layer thickness is seen even after 2 h. While the oxidation at 700°C brings about the rapid increase of SiO_2 thickness up to around 1 nm and then the very small oxidation rate, resulting in the 1.2 nm in thickness even after 8 h oxidation. The figure also shows that the thicknesses of the interface layer are almost zero up to 8 h, indicating that no interface layer is formed between SiO_2 and SiC at 700°C. These results

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suggest that an interfacial layer is not formed by low temperature oxidation, but is formed at 850°C. From the experimental results mentioned above, it is also possible to derive the conclusion that the interface layer is not formed or is extremely thin when the SiO_2 layer is thinner than around 1nm but is formed when SiO_2 thickness is over 1-2 nm. That is to say, there are two possibilities in the condition of realizing oxide layers on SiC with no interface layer, i.e., low oxidation temperatures or/and oxide layers thinner than around 2 nm. However, it is hard to study interface structure in this oxide thickness range at 850°C, because the oxide layer, around 1 nm in thickness, is formed in too short time to measure in details even at 850°C.

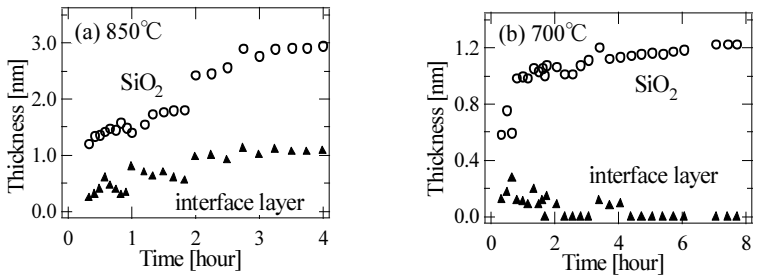

Figure 21. Oxidation time dependences of thicknesses of the SiO_2 layer and the interface layer for the oxidation at (a) 850°C and (b) 700°C [58].

By way of reducing the partial pressure during the oxidation, we have examined the oxidation at 850°C more precisely in order to clarify the formation process of interface layers. The reduction of oxygen pressure down to 0.01 atm brings about the oxidation rate almost the same as that of 700°C, 1 atm. At the reduced oxide growth rates, we can obtain the information about the interface layer in the thin oxide thickness range less than 1 nm even for the oxidation at 850°C. The results reveal that the interface layer thickness is extremely thin, when the SiO_2 layer thickness is smaller than ~1 nm. Therefore, the formation of an interface layer is considered to be independent of oxidation temperature but depends on the SiO_2 layer thickness. These results, as well as those in the study mentioned in Section 3.1, suggest that the interface layers are never transition layers between SiC and SiO_2, like as SiO_x, and/or SiO_xC_y, but the layers modified a little from SiC.

According to the interfacial Si-C emission model [33], Si atoms are considered to be emitted not only to oxide layer side but also to SiC substrate side. The Si atoms emitted into SiC may form SiC layers including Si interstitials near the SiC/oxide interface. The SiC layers with Si interstitial may have large refractive indices than SiC due to the large atomic density, but may have similar band structures due to, not the displacement of lattice sites, but the occupation of interstitial sites. Together with the experimental results that the interface layers have large refractive indices but have extinction coefficient just like SiC, the interface layers formed by SiC oxidation are supposed to SiC layers with interstitial Si atoms emitted from the interface accompanied by the oxidation of SiC. For Si oxidation, Nguyen et al. have found the existence of strained Si layers just near the Si/oxide interface and have attributed to the strain due to the expansion of Si lattices by oxidation [5]. As the red shift of the E_0 gap energy is arose by the

tensile stress in Si, the layers having different optical constants from Si are formed near the interfaces. Similarly, for SiC, the stress due to the oxidation is considered to generate the layers having different optical constants from that of SiC near the interface. The stress is reported to cause the polytype conversion from 4H-SiC to 3C-type, which is also possible to change the properties of SiC near the interface. Based on the interfacial Si-C emission model, the fact that the interface layer is not formed or the thickness of the interface layer is very small for thin oxide layers can be understood as follows. As a strain at the interface is considered to increase with the increase of oxide layer thickness, the strain in thin oxide layers is very small, and thus a little amount of Si atoms are emitted, which results in no or very thin interface layer formed. The critical thickness of the oxides at which an interface layer forms, or the noticeable changes of optical constants occur in the SiC layer near the interface, may be around 1nm.

5.2. Observation of SiC oxidation in thin oxide regime and the discussion on SiC oxidation and interface formation mechanisms

In the previous section, we have studied the initial oxidation stage, up to several nm in oxide thickness, by use of oxidation at low temperatures or under reduced oxygen pressure up to several nm in thickness of oxide, and discussed the structure and formation mechanisms of interface layer. However, it is feared that the oxidation mechanism changes with oxidation temperatures, like lower than 1000°C. Therefore, we have studied the initial oxidation stage, up to several 10 nm in thickness, at reduced oxygen pressure down to 0.02 atm at 1100°C to discuss on the formation process of the interface layers in the frame of SiC oxidation mechanism, i.e., the interfacial Si-C emission model [33], in thin-thickness regime.

Epitaxial wafers of 4H -SiC with a 0.5° off-oriented (000-1) C-face and a 8° off-oriented (0001) Si-face, both are n-types, having a net donor concentration N_d - N_a = 3 × 10^{15} cm^{-3} and 1 × $10^{16}cm^{-3}$, respectively, were used in this study. All the oxidations were conducted at the oxidation temperature of 1100°C under various oxygen partial pressures between 0.02 and 1 atm. The obtained (Ψ, Δ) spectra were analyzed using a two-layers structure model and optical constants of the interface layers were assumed to follow the modified Sellmeier's dispersion relation taking a weak optical absorption into account, Eq. (2).

Figures 22(a) and (b) show the oxide thickness dependence of the interface layer thickness and those of n_{inf} of the interface layers on the SiC (000-1) C-face and (0001) Si-face, respectively. The values of n_{inf} for 4H-SiC and SiO_2 are also shown by the broken lines in the figures. As seen in Figure 22, the interface layer thickness increases with increasing oxide thickness and saturates around 1.5 nm at the oxide thickness of around 7 nm, and this saturation thickness depends slightly on the partial pressure. The figures also show that the values of n_{inf} are also saturated around 7 nm in oxide thickness and the saturated values depend slightly on the partial pressure.

The oxide thickness dependence of the oxide growth rates on the 4H-SiC C-face and Si-face are shown in Figures 23 (a) and (b), respectively. The figures indicate, for both Si- and C-faces, basically similar oxide thickness dependences of the growth rate are seen at the partial pressures lower than 0.1 atm to those at above 0.1 atm shown in Section 4, even at the partial pressures lowered to 0.02 atm. Namely, just after the oxidation starts, the oxide growth rates

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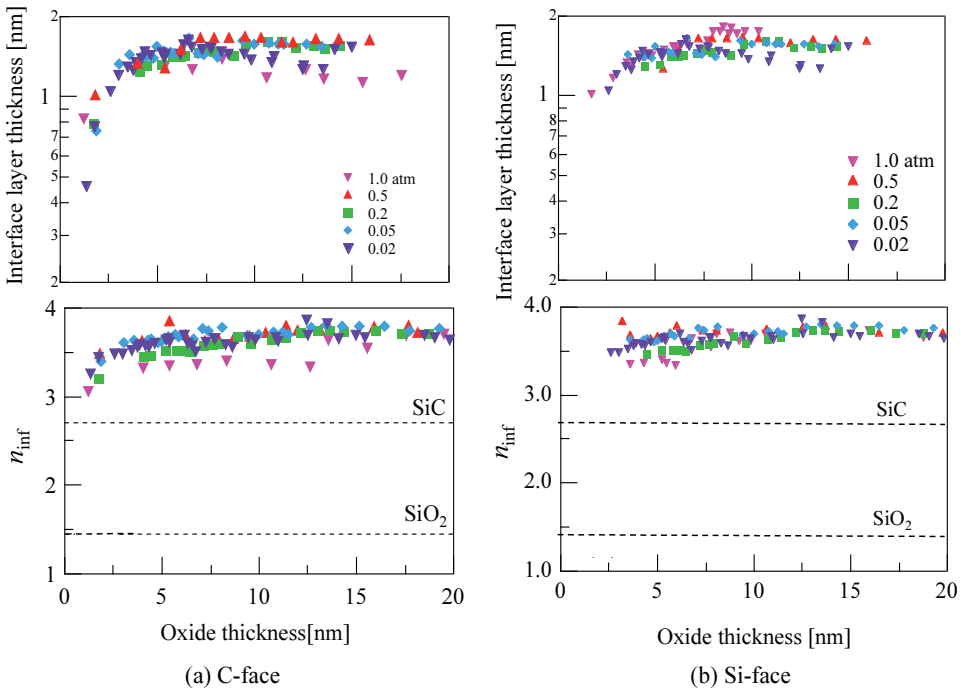

Figure 22. Oxide thickness dependence of interface layer thickness and n_{inf}. at various oxygen partial pressures on (a) the (000-1) C-face and (b) the (0001) Si-face [32].

rapidly decrease and the deceleration rate changes to a gentle one at around 7 nm in oxide thickness (hereafter the two oxidation stages are denoted as the rapid and gentle deceleration stage, respectively).

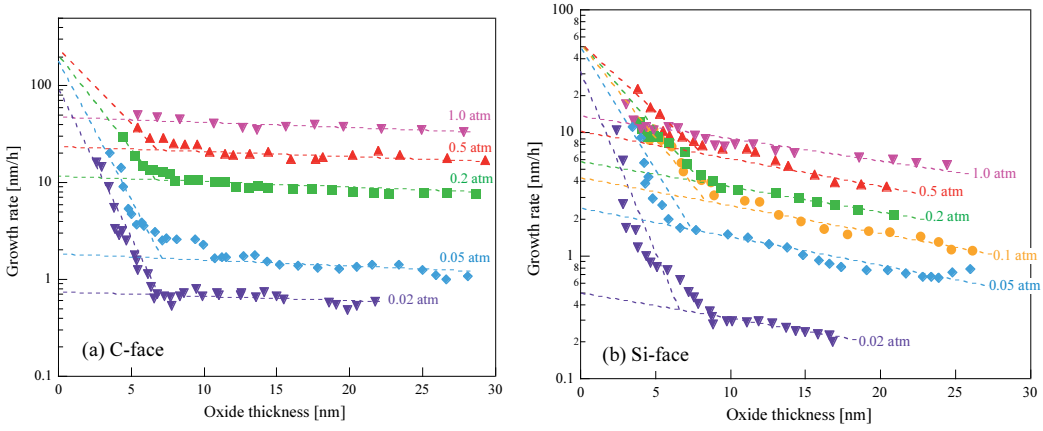

Figure 23. Oxide growth rates as a function of oxide thickness at various oxygen partial pressures on (a) the (000-1) C-face and (b) the (0001) Si-face. Broken lines are fitted to the experimental data using exponential functions [32].

We fitted the experimental data at each partial pressure with two straight lines, as shown by the dotted lines in Figures 23 (a) and (b), and derived the initial growth rate of the two deceleration stages, R_0 and R_1, by extrapolating the straight line to oxide thickness $X = 0$ in the rapid and gentle deceleration stages, respectively. The figures show that the thickness at which the deceleration rate changes from a rapid to a gentle one (termed "deceleration-rate-change thickness X_c "), i.e., the cross point of the two decay lines, is almost constant around 7 nm regardless of the oxygen partial pressure or surface polarity.

Figure 24 shows the oxygen partial pressure dependence of R_0 and R_1 on the C- and Si-faces. Since oxide growth in the thin region was too fast to follow spectroscopic ellipsometry measurements in the case of 1 atm pressure on the C-face, it was hard to estimate the oxide growth rates in the rapid deceleration stage accurately. Thus, the value of R_0 for the C-face at 1 atm is not shown in this figure. The dashed line in Figure 24 shows the data proportional to the oxygen partial pressure and fitted to the R_1 data for the C-face. For both polar faces, the data points of R_1 are almost on the line, suggesting that R_1 is proportional to the partial pressure, though, for the Si-face, R_1 becomes slightly smaller as seen from the linear relation approaching 1 atm. It should be noted that the rates are almost equal for the C- and Si-faces at low pressures, which is different from the fact that the oxide growth rates for the C-face are about 10 times larger than those for the Si-face in the several 10 nm thickness region at atmospheric oxygen pressure [15,18,19,31].

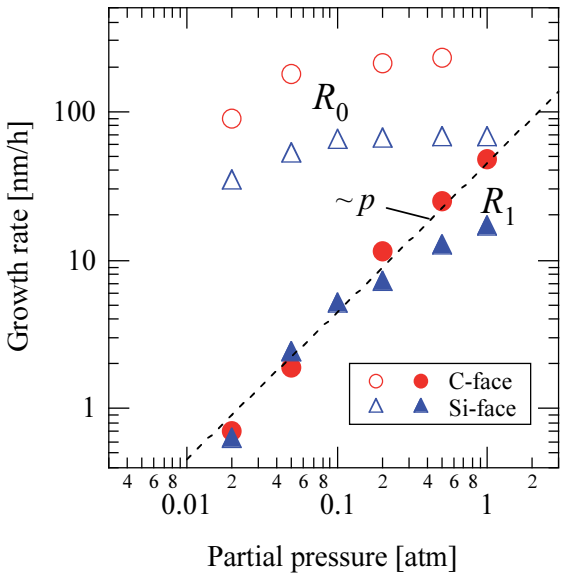

Figure 24. Oxygen partial pressure dependence of the initial growth rate, R_0 (unfilled symbols), and the gentle deceleration growth rate, R_1 (filled symbols), on the C-face (circles) and Si-face (triangles) [32].

We will discuss these results based on the oxidation mechanisms, especially, by use of interfacial Si-C atoms emission model, as follows. Here, we briefly state the essence of the Si

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and C emission model that we proposed for a description of the SiC oxidation process [33]. During oxidation, Si and C interstitials are emitted from the SiC/oxide interface, and a decrease in the interfacial reaction rate, k, as expressed by the following function, occurs as the interstitials accumulate inside the oxide near the interface accompanying progress in oxidation,

$$k = k_0\left(1-\frac{C_{Si}^{int}}{C_{Si}^{lim}}\right)\left(1-\frac{C_C^{int}}{C_C^{lim}}\right), \tag{6}$$

where C^{int} and C^{lim} are the concentrations at the interface and the solubility limit in the oxide, respectively, of the corresponding interstitial atoms, i.e., Si and C, and k_0 is the initial interfacial oxidation rate. If the oxide grows only at the interface, the oxide growth rate dX/dt is represented by the equation,

$$N_0\frac{dX}{dt} = kC_O^{int} \tag{7}$$

where N_0 is the molecular density of SiO_2, and C^{int}_O is the concentration of oxygen at the interface. As seen from this equation, a decrease in k corresponds to a decrease in dX/dt. It should be noted that the D-G model corresponds to the case that k is constant regardless of the oxide thickness in this oxidation model.

i. Formation and structures of the interface layers

We have reported [27,28] that the photon energy dependence of the optical constants n_{it} and k_{it} derived from the complex dielectric constants between 2 and 6 eV, covering the direct interband transition energy E_0 of 4H -SiC of 5.65 eV, is similar to that of bulk 4H -SiC, though the absolute values of n_{it} are about 1 larger than those of SiC, which were again confirmed in this study. The similarity in the energy dispersion of the optical constants of the interface layers suggests that the interface layer is not a transition layer between SiC and SiO_2. Rather, it is a layer having a modified structure and/or composition compared to SiC, such as a stressed or interstitials-incorporated SiC layer, locating not on the SiO_2 side but on the SiC side of the SiC/oxide interface.

The experimental results also indicated that the thickness at which the interface layer thickness and the value of n_{inf} becomes constant (i.e., 7 nm) is determined not from the surface polarity or oxygen partial pressure but from the oxide thickness. The Si-C emission model describes this behavior by considering that Si and C atoms are emitted into both directions of the SiC/oxide interface accompanying oxidation at the interface, i.e., into not only the oxide layer but also the SiC layer, and accumulation of interstitial Si and/or C atoms emitted into the SiC substrate may form a layer having similar optical properties as SiC but larger refractive indices compared to SiC. Since accumulation of interstitials is linked to the growth of the oxide, it is considered that growth of the interface layer is saturated at some intrinsic oxide thickness even

if the oxygen pressure is changed. We will discuss the behavior of the interface layer as well as that of X_c, later.

ii. Oxide thickness dependence of oxide growth rate

As mentioned above, there are two oxidation stages in the oxide growth rate curves, i.e., first rapid deceleration and second gentle deceleration. Since the growth rates at each deceleration stage are seen as a straight line in a semi-logarithm plot (shown by broken lines in Figures 23 (a) and (b)) in the respective stage, the oxide thickness dependence of the oxide growth rate can be approximated by the sum of two exponential functions [59] as

$$\frac{dX}{dt} = R_0 \exp\left(-\frac{X}{L_1}\right) - R_1 \exp\left(-\frac{X}{L_2}\right) \tag{8}$$

where R_0 and R_1 (R_0>>R_1) have the same meaning as in Figure 23, i.e., pre-exponential constants, and L_0 and L_1 (L_0<L_1) are the characteristic lengths for the deceleration of oxide growth rate in each oxidation stage, respectively. Equation (8) means that in the thin oxide regime, oxide growth occurs by two ways and they proceed not in series but in parallel because the growth rate is given by the sum of two terms and is chiefly determined by the faster one in each stage. Obviously, the L_0 and L_1 values correspond to the gradients of the fitted line in the rapid and gentle deceleration stage, respectively. As shown in Figure 23, the L_0 value decreases with decreasing partial pressure, which corresponds to the more remarkable rapid deceleration. In contrast, the L_1 value is almost constant regardless of the partial pressure. This suggests that the oxidation process is different between the rapid and gentle deceleration stages. We will discuss these two deceleration stages relevant to the oxide growth mechanism.

iii. Discussion of the two decelerating stages in terms of SiC and Si oxidation mechanisms

The existence of a rapid deceleration stage in the oxide growth rate just after oxidation starts (X < 10 nm) has also been observed for Si oxidation [4,60]. However, in investigations on Si oxidation mechanisms, the cause of the rapid deceleration has not yet been clarified. That is, the Deal-Grove model cannot fully account for the initial rapid deceleration [1]. An empirical equation, i.e., the D-G term plus an exponential term, proposed by Massoud et al.[4], can only reproduce the observed growth rates numerically, but does not provide a physical meaning. The interfacial Si emission model [52] is now believed to be the model that can reproduce the observed oxide growth rate quantitatively very well for Si oxidation. However, the model also cannot reproduce the remarkable rapid deceleration at subatmospheric oxygen pressures, as pointed out by Farjas and Roura [60]. For SiC oxidation, we have tried to reproduce the observed data using Massoud's empirical equation [30,31,50]. Here, we discuss the reasons why two deceleration stages exist in the thickness dependence of oxide growth rate, based on the interfacial Si-C emission model.

The interfacial reaction rate (k in Eq. (6)) is unlikely to depend on the oxygen partial pressure, p, because it corresponds to the rate at which one SiC molecule is changed to one SiO_2 molecule, which should not depend on p. In the thin oxide regime discussed here, the interface oxygen

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concentration C^{int}_O can be expressed as $C^{int}_O \sim pC^{lim}O$ by Henry's law, where C^{lim}_O is the solubility limit of oxygen in SiO_2. Therefore, the growth rate in the thin oxide regime, R, should be proportional to p, which is in good agreement with the experimental results in the gentle deceleration stage, i.e., R_1.

According to the Si-C emission model [33], as the number of accumulated atoms increases with oxidation, and is thus proportional to the quantity of oxidized molecules, i.e., the thickness of the oxide X, the variation in k may be approximately given as an exponential function of X in the form of $C\exp(-X/L)$, where C and L are the pre-exponential term and characteristic length, respectively, related to the accumulation of Si and C interstitials at the interface. From these considerations, as well as the fact that R_1 is proportional to p, the gentle deceleration of the oxide growth rate can be attributed to the accumulation of Si and C interstitials near the interface, and given approximately as $dX/dt \sim R_1\exp(-X/L_1)$, which is coincident with the second term in Eq. (8).

If the initial growth rate R_0 in the rapid deceleration stage is also followed by Eq. (7), it can be expressed as $R_0 \sim k_0C^{int}_O/N_0$, where k_0 is the interfacial reaction rate when the oxidation starts. As the value of k_0 is also unlikely to depend on the oxygen partial pressure, R_0 should be proportional to the oxygen pressure. As seen in Figure 24, while R_0 is not proportional to p, it decreases with decreasing p in the low p region. This suggests that R_0, i.e., the rapid deceleration, is not related to the interfacial oxide growth. In the case of Si oxidation, the experimental data show almost no dependence of R_0 with respect to p [4].

We next consider the reason why R_0 is not proportional to but rather is almost independent of the oxygen partial pressure, both for Si and SiC oxidations. It has been considered that oxide growth occurs only or mainly at the Si/oxide (SiC/oxide) interface. However, according to the Si emission model [52] for Si oxidation and the Si and C emission model [33] for SiC oxidation, Si atoms (Si and C atoms) are emitted into the oxide layer, some of which encounter the oxidant inside the oxide to form SiO_2. If the oxide is so thin that, some of the Si atoms emitted can go through the oxide layer and reach the oxide surface, those Si atoms are instantly oxidized to form a SiO_2 layer at the surface. This indicates there exist another oxide growth process other than the oxide formation at the SiC/oxide interface and that due to the oxidation of Si interstitials inside the oxide layers, i.e., the oxide formation by way of the oxidation of Si interstitials at the oxide surface. It is noted that this oxide formation process on the surface has not been considered in the Si emission model for Si oxidation [52]. The oxide growth rate of SiC is, therefore, totally given by the sum of these three oxide formation processes. In the case of oxidation inside the oxide, the probability of the emitted Si interstitials meeting the oxidant inside the oxide should be proportional to the oxygen concentration in the oxide. Therefore, this oxidation process should be proportional to p like R_1, and thus can be excluded as a candidate of the origin of R_0.

In contrast, in the case of oxidation on the oxide surface, the amount of oxygen is thought to be sufficient to oxidize all the Si atoms emitted and appearing on the surface, because the number of oxygen molecules impinging onto the surface from the gaseous atmosphere is several orders larger than the number of emitted Si atoms transmitted through the oxide even if the oxygen pressure is as low as 0.02 atm. Therefore, the oxide growth rate for oxidation on

the oxide surface should be independent of the oxygen partial pressure, which is in good agreement with the behavior of R_0. Besides, the possibility that Si interstitials go through the oxide and reach the oxide surface is considered to decrease rapidly with increasing oxide thickness, and can be given the form $\exp(-X/L_0)$, where L_0 ($<L_1$) is the escape depth of Si atoms from the oxide layer. From these considerations, the rapid deceleration stage of oxide growth rate observed just after oxidation starts is thought to be due to oxidation of Si interstitials on the oxide surface. Therefore, the value of X_c obtained from the experiments of 7 nm indicates that the escape depth of Si atoms from the oxide is estimated to be several nanometers at 1100°C. Since the behavior of Si interstitials other than at the interface should be the same for the C- and Si-faces, it is reasonable that the value of X_c does not depend on the polarity of the SiC faces. Moreover, the fact that the growth rates in the thin regime at low pressures are not very different for the C- and Si-faces can be explained by considering that surface oxide growth is dominant over oxide growth in this stage and oxidation on the oxide surface may proceed independent of the surface polarity.

Theoretical calculations of the growth rates reported so far have not taken into account the surface oxide growth for both Si and SiC oxidations. However, in the extremely thin oxide thickness range and especially at low oxygen partial pressures, the contribution from surface oxide growth as well as those from the interface and internal oxide growth should be taken into account. However, to confirm the argument derived from the experimental results in this study, it is necessary to perform numerical calculations of the oxide growth rates within the framework of the Si-C emission model, taking into account the contribution from oxidation on the surface. In the case of Si oxidation, the interfacial Si emission model [52] cannot reproduce the growth rate in the thin oxide region at sub-atmospheric pressures, as pointed out by Farjas and Roura [60], where the introduction of the contribution from the surface oxide growth may dissolve the disagreement between the calculated and the observed oxide growth rates.

As mentioned above, the X_c value is almost constant around 7 nm regardless of the oxygen partial pressure, though the rapid deceleration stage can be observed more remarkably at lower partial pressures. In the case of Si oxidation, a rapid deceleration stage has also been observed just after oxidation starts, and the thickness corresponding to X_c is also almost independent of the oxygen partial pressure, though the growth rates at X_c depend on the oxygen partial pressure [4,60]. Therefore, it can be stated that X_c is determined only by the thickness of the oxide layer for both the Si and the SiC oxidation cases. It is to be noted that the value of X_c is very close to the thickness at which the interface structures become constant as revealed above. In addition, the pressure dependence of the oxide thickness when the interface layer becomes unchanged also exhibits the same behavior, i.e., they are almost independent of pressure. These results suggest that an interface layer gradually grows during the surface oxide growth and, after transforming to the interfacial and internal oxide growth, the interface layer stops growing. It is considered that the interface layer located on the SiC side of the interface may be oxidized to form SiO_2 and a new interface layer may form on the SiC side, which results in movement of the position of the interface layer in the direction of the SiC substrate with progress in oxidation. Therefore, the brake for the interface layer growth

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is considered to be responsible for the abrupt change in growth rate at X_c. Otherwise, during the surface oxide growth, fewer interstitials emit into the SiC-side because the concentration of interstitials in the oxide is quite low; in turn, the emission into the SiC-side increases with accumulation of interstitials in the oxide and then the accumulation of interstitials is saturated when it balances with the progress in oxidation front.

6. Summary

We have employed spectroscopic ellipsometry, one of the methods of observing buried interfaces keeping intact for observing SiC/oxide interfaces to investigate their structures. We have developed the characterization method of the oxide layers and SiC/oxide interfaces, i.e., by using sloped oxide layers, and made clear the depth profile of the refractive indices and interface structures, i.e., there exist interface layers, having high refractive indices compared with those of SiC and SiO_2, the values of which depend on the oxide layer formation method, around 1 nm in thickness, at oxide/SiC interface and only the thickness of the SiO_2 layers changes with oxidation time or oxide thickness. It can be said that the optical properties estimated from the analysis using the single layer model, i.e., the oxide films are assumed to be optically uniform single layer on SiC, are "apparent" features, and it is not true that the optical constants of the oxide layers change with oxidation time or oxide thickness. The results that the refractive indices of the interface are larger than those of both SiC and SiO_2 reveal that the interfaces are neither the transition layers having the composition between SiO_2 and SiC nor those due to interface roughness.

Optical and electrical evaluations of SiC/oxide interface based on the spectroscopic ellipsometry in the visible to deep UV region and the *C-V* measurements by using the same samples for both measurements have been carried out for the samples with both surface polarities, and formed by various oxidation methods and temperatures, including the samples after various POA. Quite good correlations between the changes in refractive indices of the interface layers n_{it} by the oxidation condition and those in interface state density D_{it} are found for all the cases of oxidation conditions. These correlations suggest that the formation of the interface layers with large refractive indices is related to the generation of interface states. It is also found that the wavelength dependences of extinction coefficient of the interface layers k_{it} are quite similar to those of SiC in the entire wavelength range measured, suggesting the presence of layers with a little different band structures from that of bulk SiC, e.g., strained SiC layers. By using the method of inducing interface state density by γ-ray irradiation, we have confirmed that the values of refractive indices of interfaces obtained from spectroscopic ellipsometery are well correlated with the electrical properties of interface, like interface state density, which strongly supports that the values of refractive indices of interface layers are reflected from the electrical properties of interfaces.

We have also developed the observation system in order to perform real-time *in-situ* observation of SiC oxidation for the first time. By using this system, we have observed the occurrence of the oxide growth rate enhancement in the thin oxide regime for the oxidation of SiC both

for Si- and C-faces. We have also observed that the growth rate of SiC for both polar faces can be well represented by the Massoud's empirical equation using the four adjusting parameters. From the differences in temperature and oxygen partial pressure dependences of these parameters, we have discussed on the difference of the oxidation mechanisms between Si-face and C-face of SiC.

Finally, we have studied the oxygen partial pressure dependence of the SiC oxidation process in the initial oxidation stage in details at oxygen partial pressures ranging from 0.02 to 1.0 atm. It was found that regardless of the surface polarity as well as the oxygen partial pressure, an interface layer having modified SiC structures is formed accompanied by oxidation just below the SiC/oxide interface in the same manner, i.e., the thickness and refractive indices of the interface layer increase with an increase in the oxide thickness, the interface layer thickness reaches about 1.5 nm at an oxide thickness of around 7 nm, and then the thickness and structure of the interface layer do not change anymore with further increase in oxide thickness. The oxide thickness dependence of the growth rate at sub-atmospheric oxygen partial pressures down to 0.02 atm is similar to those at 1 atm. Namely, just after the oxidation starts, the oxide growth rate rapidly decreases and the deceleration-rate changes to a gentle mode at around 7 nm in oxide thickness, which is almost the same thickness at which the thickness and the structure of the interface layers become constant. We have shown that the interfacial Si-C emission model can explain the cause for the change in deceleration rate of the oxide growth rate from the oxygen partial pressure dependence and found that the oxide growth due to oxidation of Si interstitials on the oxide surface plays a dominant role in the extremely thin thickness region, less than several nanometers.

Through the studies on SiC/oxide interfaces based on the spectroscopic ellipsometry measurements, we have found the existence of strong correlation between the optical properties of interface, like n_{it}, and the electrical properties, like D_{it}. However, in general, the mechanisms of the relation between the MOS characteristics of SiC, i.e., low carrier mobility and threshold voltage instability, and the interface structures have not been made clear. It is eager to understand the mechanisms of SiC-MOS characteristics in relation to the interface structures. The results obtained suggest the interface structures, i.e., the formation of interface layers with high refractive indices depend on oxide thickness as well as the oxidation conditions. Therefore, it can be said that the process of forming no interface layers or the interface layers with very thin or having lower refractive indices is desirable, by the methods of, for example, using very thin oxide layers. The formation of insulated layers for MOS structures not by oxidation of SiC, but by the deposition of insulator materials, for examples, Si oxide and Al oxide, may be other candidates, though caution should be taken to avoid the proceed of oxidation during the device process performed after the formation of MOS interface. Anyway, the important point is to develop the process based on the information of "true" interface structures obtained by use of non-distractive measurement methods, like ellipsometry, with selecting an appropriate model for the analyses of measured data.

Author details

Sadafumi Yoshida[1*], Yasuto Hijikata[2] and Hiroyuki Yaguchi[2]

*Address all correspondence to: s.yoshida@aist.go.jp

1 Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan

2 Graduate School of Science and Engineering, Saitama University, Saitama, Japan

References

[1] Deal BE, Grove AG. General relationship for the thermal oxidation of silicon. J Appl Phys 1965;36(12):3770-8.

[2] Taft E, Cordes L. Optical evidence for silicon-carbide oxide interface. J Electrochem Soc 1979;126:131-4.

[3] Aspnes DE, Theeten JB. Optical properties of the interface between Si and its thermally grown oxide. Phys Rev Lett 1971;43(14):1046-9. Dielectric function of Si-SiO_2 and Si-Si_3N_4 mixture. J Appl Phys 1979;50(7):4928. Spectroscopic analysis of the interface between Si and its thermally grown oxide. J Electrochem Soc 1980;127(6): 1359-65.

[4] Massoud HZ, Plummer JD, Irene EA. Thermal oxidation of silicon in dry oxygen growth-rate enhancement in the thin regime. I. Experimental results. J Electrochem Soc 1985;132(11):2685-93. II. Physical mechanisms. *ibid*. 2693-700. Analytical relationship for the oxidation of silicon in dry oxygen in the thin-film regime. J Appl Phys 1987;62(8):3416-23.

[5] Nguyen N, Chandier-Horowitz D, Amirtharaj PM, Pollengrino JP. Spectroscopic ellipsometry determination of the properties of the thin underlying strained Si layer and the roughness at SiO_2/Si interface. Appl Phys Lett 1994;64(20):2688-90.

[6] Suwa T, Teramoto A,.Kumagai K, Abe K, Lie X, Nakao Y, Yamamoto M, Nohira H, Muro T, Kinoshita T, Sugawa S, Ohmi Hattori M. Chemical structure of interfacial transition layer formed on Si (100) and its dependence on oxidation temperature, annealing in forming gas, and difference in oxidizing species. Jpn J Appl Phys 2013;52:031302.

[7] Hebert KJ, Zafar S, Irene EA, Kuehn R, McCarthy TE, Demirliogle EK. Measurement of the refractive index of thin SiO_2 films using tunneling current oscillation and ellipsometry. Appl Phys Lett 1996;68(2):266-8.

[8] Herzinger CM, Johs B, McGahan WA, Woollan A. Ellipsometric determination of optical constants for silicon and thermally grown silicon dioxide via a multi-sample, multi-wavelength, multi-angle investigation. J Appl Phys 1998;83(6):3323-36.

[9] Jernigan GG., Stahlbush RE, Das MK, Cooper Jr JA, Lipkin LA. Interfacial differences between SiO_2 grown on 6H-SiC and on Si(100). Appl Phys Lett 1999;74(10):1448-50. Effect of oxidation and reoxidation on the oxide-substrate interface of 4H- and 6H-SiC. *ibid*. 2000;77(10):1437-9.

[10] Zhu X, Lee HD, Feng T, Ahyi AC, Mastrongiovann D, Wan A, Garfunkel E, Williams JRG, Feldman LC. Structure and stoichiometry of (0001) 4H-SiC/oxide interface. Appl Phys Lett 2010;97:071908.

[11] Watanabe H, Hosoi T, Kirino T, Kagei Y, Uenishi Y, Chanthaphan A, Yoshigoe A, Teraoka Y, Shimura T. Synchrotron X-ray photoelectron spectroscopy study on thermally grown SiO_2/4H-SiC (0001) interface and its correlation with electrical properties. Appl Phys Lett 2011;99:021907.

[12] Zheleva T, Lelis A, Duscher G, Liu F, Levin I, Das M. Transition layers at the SiO_2/SiC interface. Appl Phys Lett 2008;93:022108.

[13] Biggerstaff TL, Reynolds Jr CL, Zheleva T, Lelis A, Habersat D, Henry S, Ryu S-H, Agawal A, Dusher G. Relationship between 4H-SiC/SiO_2 transition layer thickness and mobility. Appl Phys Lett 2009;95:032108.

[14] Hatakeyama T, Matsuhata H, Suzuki T, Shinohe T, Okumura H. Microscopic examination of SiO_2/4H-SiC interfaces. Mater Sci Forum 2011;679-680:330-3.

[15] Suzuki A, Ashida H, Furui N, Maneno K, Matsunami H. Thermal oxidation of SiC and electrical properties of Al-SiO_2-SiC MOS structure. Jpn J Appl Phys 1982;21(4): 579-85.

[16] Zheng Z, Tresslerand RE, Spear KE. Oxidation of single-crystal silicon carbide, Part 1 Experimental studies. J Electrochem Soc 1990;137(3):854-8. Part II. Kinetic model. *ibid.* 1990;137(9):2812-6.

[17] Fung CD, Kopanski JJK. Thermal oxidation of 3C-silicon carbide single-crystal layers on silicon. Appl Phys Lett 1984;45(7):757 -9.

[18] Song Y, Dhar S, Feldman LC, Chung G, Williams JR. Modified Deal Grove model for the thermal oxidation of silicon carbide. J Appl Phys 2004;95:4953-7.

[19] Ray EA, Rozen J, Dhar S, Feldman LC, Williams JR. Pressure dependence of SiO_2 growth kinetics and electrical properties on SiC. J Appl Phys 2008;103:023522.

[20] Szilagyi E, Petrik P, Lohner T, Koos AA, Fried M, Battistlig G. Oxidation of SiC investigated by ellipsometry and Rutherford backscattering spectrometry. J Appl Phys 2008;104:014903.

[21] Hazura S, Chakraborty S, Lai PT. Density profiles and electrical properties of thermally grown oxide nanofilms on p-type 6H-SiC (00001). Appl Phys Lett 2004;85(23): 5580-2.

[22] Correa SA, Radtke C, Soares G.V, Miotti L, Baumiol IJR, Dimitriyev S, Ham J, Hold L, Kong F, Stedile FC. Effects of nitrogen incorporation on the interface layer between thermally grown dielectric films and SiC. Appl Phys Lett 2009;94:251909.

[23] Tsuchida H, Kamata I, Izumi K. Infrared analysis of SiO_2 films on the 6H-SiC surfaces. Appl Surf Sci 1997;117/118:225-9.

[24] Yoshikawa M, Seki H, Inoue K, Nanen Y, Kimoto T. Characterization of inhomogeneity in silicon dioxide films on 4H-silicon carbide epitaxial substrate using a combination of Fourier transform infrared and cathodoluminescence spectroscopy. Appl Spectroscopy 2014;68(10):1176-80.

[25] Iida T, Tomioka Y, Hijikata Y, Yaguchi H, Yoshikawa M, Ishida Y, Okumura H, Yoshida S. Characterization of oxide films on SiC by spectroscopic ellipsometry. Jpn J Appl Phys 2000;39(10B):L1054-6.

[26] Iida T, Tomioka Y, Yoshimoto K, Midorikawa M, Tsukada H, Orihara M, Hijikata H, Yaguchi H, Yoshikawa M, Itoh H, Ishida Y, Yoshida S. Measurements of the depth profile of the refractive indices in oxide films on SiC by spectroscopic ellipsometry. Jpn J Appl Phys 2002;41(2A):800-4.

[27] Hashimoto H, Hijikata Y, Yaguchi H, Yoshida S. Optical and electrical characterizations of 4H-SiC-oxide interfaces by spectroscopic ellipsometry and capacitance-voltage measurements. Appl Surf Sci 2009;255:8648-53.

[28] Seki H, Wakabayashi T, Hijikata Y, Yaguchi Y, Yoshida S. Characterization of 4H-SiC-SiO_2 interfaces by deep ultraviolet spectroscopic ellipsometer. Mater Sci Forum 2009;615-617:505-8.

[29] Kakubari K, Kuboki R, Hijikata Y, Yaguchi H, Yoshida S. Real time observation of SiC oxidation using an *in-situ* ellipsometer. Mater Sci Forum 2006;527-529:1031-4.

[30] Yamamoto T, Hijikata Y, Yaguchi H, Yoshida S. Growth rate enhancement of (000-1)C-face silicon-carbide oxidation in thin oxide regime. Jpn J Appl Phys 2007;46(32):L770-2.

[31] Yamamoto T, Hijikata Y, Yaguchi H, Yoshida S. Oxide growth rate enhancement of silicon carbide (0001) Si-faces in thin oxide regime. Jpn J Appl Phys 2008;47(19): 7803-6.

[32] Kouda K, Hijikata Y, Yagi S, Yaguchi H, Yoshida S. Oxygen partial pressure dependence of the SiC oxidation process studied by in-situ spectroscopic ellipsomerty. J Appl Phys 2012;112:024502.

[33] Hijikata Y, Yaguchi H, Yoshida S. A kinetic model of silicon carbide oxidation based on the interfacial silicon and carbon emission phenomena. Appl Phys Express 2009;2:021203.

[34] Yoshikawa M, Satoh K, Ohshima T, Itoh H, Nashiyama I, Yoshida S, Okumura H, Takahashi, Ohnishi K. Depth profile of trapped charges in oxide layer of 6H-SiC metal-oxide-semiconductor structures. J Appl Phys 1996;80(1):282-7.

[35] Tomioka Y, Iida T, Midorikawa M, Tukada H, Yoshimoto K, Hijikata Y, Yaguchi H, Yoshikawa M, Ishida Y, Kosugi R, Yoshida S. Characterization of the interfaces between SiC and oxide films by spectroscopic ellipsometry. Mat Sci Forum 2002;389-393:1029-32.

[36] Cho W, Kosugi R, Senzaki J, Fukuda K, Arai K, Suzuki S. Study on electron trapping and interface states of various gate dielectric materials in 4H-SiC metal-oxide-semiconductor capacitors. Appl Phys Lett 2000;77(13):2054-6.

[37] Dunham ST. Interaction of silicon point defects with SiO_2 films. J Appl Phys 1992;71(2):685-96.

[38] Cobet C, Wilmers K, Wethkamp T, Edwards NV, Esser N, Richter W. Optical properties of SiC investigated by spectroscopic ellipsometry. Thin Solid Films 2000;364:111-3.

[39] Zollner S, Chen JG, Duda E, Wetteroth T, Wilson SR, Hilfiker JN. Dielectric functions of bulk 4H and 6H SiC and spectroscopic ellipsometry studies of thin SiC films on Si. Appl Phys Lett 1999;85(12):8353-61.

[40] Lindquist OPA, Jarrendhl K, Peters S, Zettler JT, Cobet C, Esser N, Aspnes DE, Henry A, Edwards NV. Ordinary and extraordinary dielectric function of 4H- and 6H-SiC from 3.5 to 9.0 eV. Appl Phys Lett 2001;78(18):2715-7.

[41] Ishida Y, Takahashi T, Okumura H, Jikimoto T, Tsuchida H, Yoshikawa M, Tomioka Y, Hijikata Y, Yoshida S. The investigation on 4H-SiC/SiO_2 interfaces by optical and electrical measurements. Mater Sci Forum 2002;389-393:1013-6.

[42] Hijikata Y, Yaguchi H, Yoshikawa M, Yoshida S. Composition analysis of SiO_2/SiC interfaces by electron spectroscopic measurements using slope-shaped oxide films. Appl Sur Sci 2001;184:161-6.

[43] Fukuda K, Kato K, Senzaki J, Kojima K, Suzuki T. 4H-SiC MOSFETs on C(000-1) face with inversion channel mobility of 127 cm^2/Vs. Mater Sci Forum 2004;457-460:1417-20.

[44] Allerstam F, Olafsson HO, Gugjonsson G, Dochev D, Sveinjornsson EO, Rodle T, Jos R. A strong reduction in the density of near-interface traps at the SiO_2/4H-SiC interface by sodium enhanced oxidation. J Appl Phys 2007;101:124502.

[45] Chung GY, Williams JR, Tin CC, McDonald K, Farmer D, Chanana RK, Pantelides ST, Holland OW, Feldman LC. Interface state density and channel mobility for 4H-SiC MOSFETs with nitrogen passivation. Appl Surf Sci 2001;184:399-403.

[46] Hijikata Y, Yaguchi H, Yoshida S. Effect of Ar post-oxidation annealing on oxide-4H-SiC interfaces studied by capacitance to voltage measurements and photoemission spectroscopy. J Vac Sci Technol 2005;A23(2):298-303.

[47] Cantin JL, von Bardeleben HH, Shinkin Y, Ke Y, Devaty RP, Choyke WJ. Identification of the carbon dangling bond center at the 4H-SiC/SiO_2 interface by an EPR study in oxidized porous SiC. Phys Rev Lett 2004;92(1):015502.

[48] Midorikawa M, Hijikata Y, Yaguchi H, Yoshikawa M, Kamiya T, Yoshida S. Characterization of SiC/oxide films interfaces by spectroscopic ellipsometer (II), Extended Abstracts, The 49th Spring Meeting, 2009, The Japan Society of Applied Physics and Related Societies. p.433.

[49] Goto D, Hijikata Y, Yagi S, Yaguchi H. Differences in SiC thermal oxidation process between crystalline surface orientations observed by in-situ spectroscopic ellipsometry. J Appl Phys 2015;117:095306.

[50] Yamamoto T, Hijikata Y, Yaguchi H, Yoshida S. Oxygen-partial-pressure dependence of SiC oxidation rate studied by *in-situ* spectroscopic ellipsometry. Mater Sci Forum 2009;600-603:667-70.

[51] Grove AS. Physics and Technology of Semiconductor Devices, John Wiley & Sons, New York, 1967, p.31.

[52] Kageshima H Shiraishi K, Uematsu M. Universal theory of Si oxidation rate and importance of interfacial Si emission. Jpn J Appl Phys 1999;38(9A/B):L971-4.

[53] Ogawa S, Takakuwa Y. Rate-limiting reactions of growth and decomposition kinetics of very thin oxides on Si (001) surfaces studied by reflection high-energy electron diffraction combined with Auger electron spectroscopy. Jpn J Appl Phys 2006;45(9A): 7063-79.

[54] Watanabe T, Tatsumura K, Ohdomari I. New linear-parabolic rate equation for thermal oxidation of silicon. Phys Rev Lett 2006;96:196102.

[55] Ueshima M, Kageshima H, Shiraishi K. Simulation of high-pressure oxidation of silicon based on the interfacial silicon emission model. Jpn J Appl Phys 2000;39(10A):L952-4. Simulation of wet oxidation of silicon based on the interfacial silicon emission model and comparison with dry oxidation. J Appl Phys 2001;89(3): 1948-53.

[56] Hijikata Y, Yaguchi H, Yoshida S, Tanaka Y, Kobayashi K, Nohira H, Hattori T. Characterization of oxide films on 4H-SiC epitaxial (000-1) faces by high-energy-resolution photoemission spectroscopy: comparison between wet and dry oxidation. J Appl Phys 2006;100:053710.

[57] Takahashi K, Nohira H, Hirose K, Hattori T. Accurate determination of SiO_2 film thickness by X-ray photoelectron spectroscopy. Appl Phys Lett 2003;83(16):3422-4.

[58] Takaku T, Hijikata Y, Yaguchi H, Yoshida S. Observation of SiC oxidation in ultra-thin oxide regime by in-situ spectroscopic ellipsometry. Mater Sci Forum 2009;615-617:509-12.

[59] Kouda K, Hijikata Y, Yaguchi H, Yoshida S. *In-situ* spectroscopic ellipsometry study of SiC oxidation at low oxygen-partial-pressures. Mater Sci Forum 2010;645-648:813-6.

[60] Farjas J, Roura P. Oxidation of silicon: further tests for the interfacial silicon emission model. J Appl Phys 2007;102:054902.

Section 2

SiC Electronic Devices

Chapter 5

Comparative Study of Optimally Designed DC-DC Converters with SiC and Si Power Devices

O. Deblecker, Z. De Grève and C. Versèle

Additional information is available at the end of the chapter

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Abstract

In this chapter, power losses and mass of optimally designed Si- vs. SiC-based isolated DC-DC converters are compared in quantitative terms. To that end, an adapted version of a computer-aided design tool, previously published by the authors, is used. The database of the existing tool was completed with new wide band gap semiconductor devices currently available from manufacturers. The results are presented for two switch-mode power supplies, each constituted of an isolated DC-DC converter, operating at very different power levels: a 100 kW auxiliary railway power supply and a multiple output 33.5 W power supply intended for a space application. The gains in terms of power losses and mass from one technology to the other can advantageously be evaluated thanks to the developed tool.

Keywords: Multiobjective optimization, genetic algorithms, DC-DC converters, SiC devices

1. Introduction

The electric energy is one of the most flexible forms of energy available today, which is mainly due to the development of power electronics over the past decades. Nevertheless, a correct design of power electronic converters is not a trivial task: it usually involves the minimization of multiple conflicting objectives such as, *e.g.* (but not restricted to), the power losses and mass, while ensuring the satisfaction of several technological and thermal constraints. In this context, the authors proposed in a previous work [1,2] a computer-aided design (CAD) tool dedicated

to isolated DC-DC converters, based on multiobjective (MO) optimization using genetic algorithms (GAs). A key advantage of that predesign tool is that it does not restrict to one solution. Instead, it proposes to the designer a set of optimal solutions so that he can choose *a posteriori* which solution best fits the application under consideration or which objective function to favor.

Modern DC-DC power converters often belong to the category of switched mode power supplies (SMPS), for their high-energy efficiency (more than 90%) and their ability to ensure galvanic isolation [3]. Moreover, SMPS are employed in a lot of applications, covering a wide power range (from several tens of watts to hundreds of kilowatts) and fed by different voltage levels. For instance, they are more and more used in vehicular applications (traction and auxiliary converters in trains and electric automobile vehicles) as well as in aeronautics and space.

In addition to passive components, such as filter capacitors/inductors and transformers for providing the electrical isolation, SMPS include power transistors continually switching between low dissipative full-on and full-off states. The switching frequency of those semiconductor devices strongly impacts the design of the magnetic components. Indeed, it is well known that a high-switching frequency yields small values of the core cross section and hence smaller inductors or transformers. Knowing that magnetic components can account for more than 50% of the volume and mass of a power converter, one then understands how crucial it is to use semiconductor devices with fast switching speeds. Yet it should be kept in mind that increasing the switching frequency also increases the switching losses, which can lead to abnormally high-junction temperatures and/or heat sink module dimensions [3]. Currently, the power switches (IGBTs and MOSFETs) as well as diodes are based on silicon (Si) technology, and hence, the continuously increasing demand for lightweight power converters forces the engineers to operate the components at switching frequencies close to their intrinsic limits. This maximum value is however seldom reached, as a trade-off between the switching losses and the speed is needed.

It is now well established in the power electronics community that silicon-carbide (SiC) and gallium-nitride (GaN) semiconductor materials show superior properties, enabling potential power device operation at higher voltages, temperatures, and switching speeds than conventional Si technology (see Figure 1). As a result, this gives rise to new perspectives for the design of power converters with enhanced performances [4–7]. Until now, GaN-based power transistors are still restricted to low voltage applications, whereas SiC components are available with higher voltage ratings and therefore higher power capability. Some manufacturing limitations of GaN devices can be found in [8,9]. Note that, recently, the experimental prototype of a hard switched 20 W/50 V RF GaN-based DC-DC converter intended for use in an envelope-tracking power amplification system has been presented, achieving an efficiency up to 91.6% at 50 MHz [10]. Regarding the performances, power devices based on diamond would be, of course, the most interesting, but this option is not economically acceptable today.

Within this framework, the present contribution aims at comparing in quantitative terms power losses and mass of optimally designed Si- *vs*. SiC-based isolated DC-DC power converters [11]. To that end, an adapted version of the previously mentioned MO optimization

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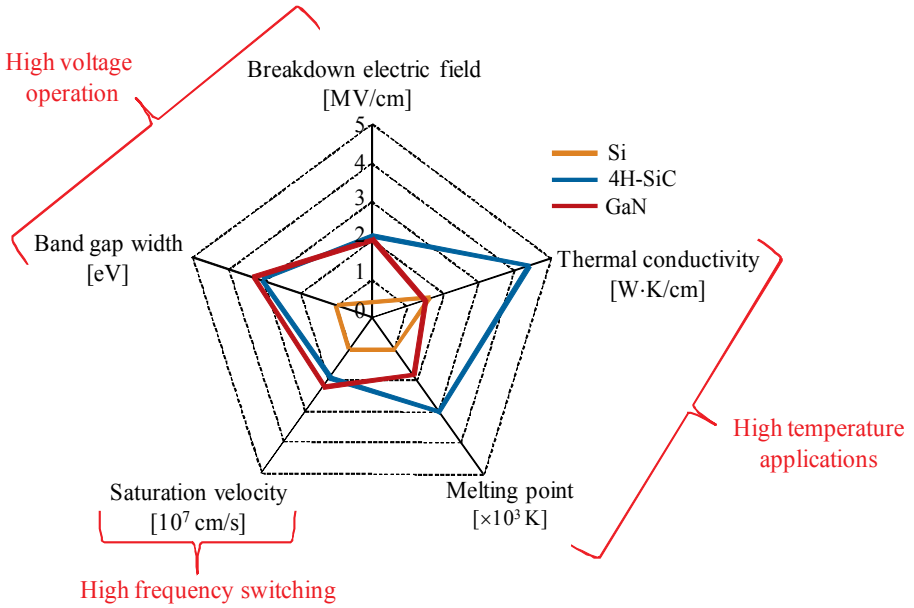

Figure 1. Summary of Si, SiC, and GaN relevant material properties.

CAD tool, completed with a new database of wide band gap semiconductor devices, will be used. Two power supplies operating at very different power levels will be selected as application examples: a high-power (100 kW) auxiliary railway SMPS and a low-power (33.5 W) SMPS intended for a space application.

The remainder of this chapter is organized as follows. In Section 2, a comparison between Si and wide band gap (WBG) materials is first presented. Then the WBG devices (mainly SiC) that will be taken into account in this work are listed in the same section. In Section 3, basic information about the models employed to represent the power converters are given. The existing CAD tool, based on GA, is briefly reviewed in the fourth section. The MO optimal design of the two above-mentioned power supplies, each constituted of an isolated DC-DC converter, is conducted in Sections 5 and 6, with and without including SiC devices in the optimization procedure in order to evaluate the gains in terms of power losses and mass. Finally, conclusions and perspectives are exposed in Section 7.

2. Wide band gap materials and power electronic devices

Since the 1950s, WBG materials are expected to replace silicon in semiconductor power devices when it reaches its limits [12]. However, their use in power electronics has been widely considered only recently due to their advantages over Si power devices regarding temperature and power operation [4]. The purpose of this section is to briefly review the intrinsic properties and figures of merit of the principal WBG materials, in comparison with classical Si material.

Then the WBG semiconductor devices (mainly SiC) that will be considered in this chapter are listed.

2.1. Properties of wide band gap semiconductors

Several interesting properties of Si and WBG semiconductor materials are reported in Table 1, at a temperature of 300 K [5,13,14]. Note that different polytypes of SiC material exist, each one being characterized by its own crystal lattice structure. They differ in their electronic properties but feature similar mechanical and thermal behavior, which is due to the particular nature of the Si-C chemical link. Among those, the most commonly used is the polytype 4H-SiC.

Properties (at 300 K)	Si	4H-SiC	6H-SiC	3C-SiC	GaN	Diamond
Band gap width E_g [eV]	1.12	3.26	3.03	2.3	3.45	5.45
Breakdown electric field E_c [MV·cm^{-1}]	0.3	2.2	2.5	2	2	10
Intrinsic carrier concentration n_i [cm^{-3}]	9.6×10^{9}	5×10^{-9}	1.6×10^{-6}	1.5×10^{-1}	1.9×10^{-10}	1.6×10^{-27}
Electrons mobility μ_N [cm^2·V^{-1}·s^{-1}]	1500	1000	500	800	1250	2200
Holes mobility μ_P [cm^2·V^{-1}·s^{-1}]	600	115	101	40	850	850
Thermal conductivity λ [W·K cm^{-1}]	1.5	4.9	4.9	3.2	1.3	22
Relative permittivity ε_r	11.8	10	9.7	9.7	9	5.5
Saturation velocity v_{sat} [×10^7 cm·s^{-1}]	1	2	2	2.5	2.2	2.7
Maximum working temperature T_{max} [°C]	150	760	760	500	800	1100

Table 1. Comparison between intrinsic properties of Si and WBG semiconductor materials.

The band gap width E_g refers to the energy needed for one electron to jump from the valence to the conduction band. A material with a high E_g implies that the probability for an electron to cross the band gap under thermal excitation is low, thus allowing high working temperature operation. Note that the term "wide band" usually refers to values of E_g greater than 2 eV [6]. Materials with a high band gap are also less subject to electron jumps caused by radiations, which is an asset in the case of space or nuclear applications.

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The maximum working temperature T_{max} is defined as the temperature for which the number of intrinsic carriers becomes greater than doping. In that case, the material loses its semiconducting properties. For instance, in Table 1, it can be noticed that WBG materials have higher T_{max} than Si. Diamond and SiC are also better heat conductors than Si, according to the values of their thermal conductivity λ.

A WBG also corresponds to a high breakdown electric field E_c, which permits to build components with high voltage capabilities (currently up to 20 kV for SiC power devices). Indeed, the breakdown electric field for WBG materials is more or less one order of magnitude higher than for Si, according to the value reported in Table 1. Thus, WBG components might be, for example, interesting candidates for use in power supplies of space traveling wave tubes, which have to produce voltages up to several kilovolts [15].

As explained in [6,14], the reverse leakage current of bipolar junctions is proportional to n_i or n_i^2, with n_i the intrinsic carriers concentration. Thus, considering the values of n_i in Table 1, the reverse leakage current is several order of magnitudes smaller with WBG components compared to Si.

Generally, high values for the charge carrier mobilities μ_N (electrons) and μ_P (holes), and for the saturation velocity v_{sat} (which is the maximum velocity the charge carriers can reach under the application of an electric field), are needed. In that way, it is possible to operate at higher current densities and switching frequencies [16]. It can be seen in Table 1 that SiC and GaN materials have slightly smaller mobilities than Si. Yet that drawback is balanced by a higher saturation velocity. Moreover, a large value of v_{sat}, combined with small values of the electrical permittivity ε_r, is important for high-frequency applications [14].

The conduction losses essentially depend on ε_r and the breakdown electrical field E_c. Indeed, the on-state resistance r_{on} of a unipolar component, as, e.g., a metal oxide semiconductor field effect transistor (MOSFET), is inversely proportional to these two variables [14]:

$$r_{on} \propto \frac{1}{\varepsilon_r E_c} \tag{1}$$

This permits to highlight another advantage of WBG components over classical Si ones. Indeed, Figure 2 represents the on-state resistance r_{on} as a function of the maximum supported voltage for Si and WBG unipolar components, once again at 300 K. Commonly, a value of a few hundreds of $m\Omega\ cm^2$ yields reasonable conduction losses. In that case, Figure 2 shows that the maximum supported voltage for Si components is approximately limited to 1 kV, whereas WBG components can support a few tens of kilovolts.

For a comparison of the possible power electronics performances of these materials, some commonly known figures of merit, i.e., special quality criteria, are listed in Table 2 [17,18]. The values reported in this table have been calculated from the data given in Table 1 and normalized with respect to Si. A larger value represents a better material performance in the corresponding category.

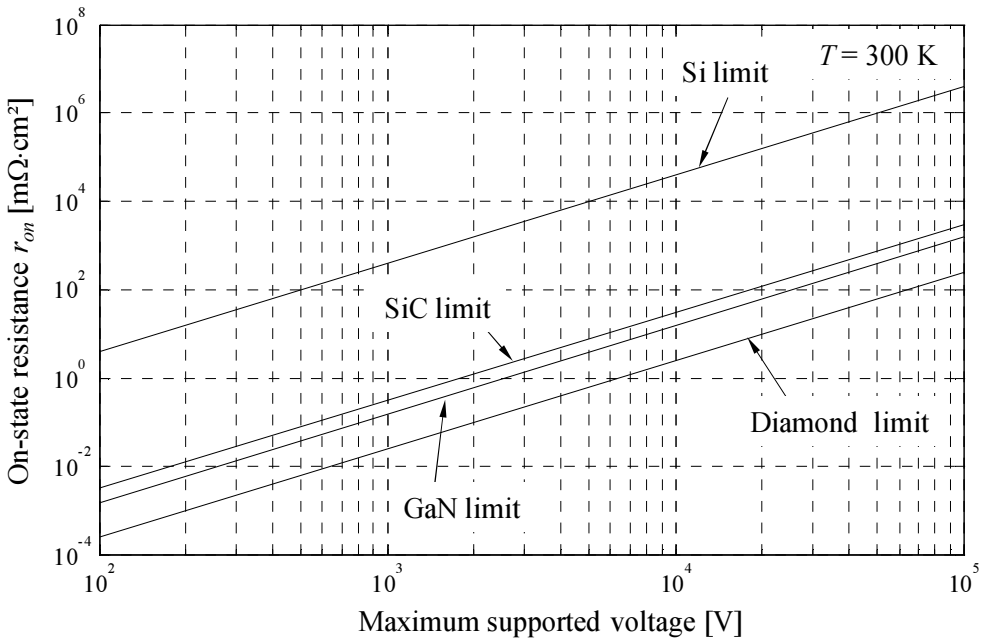

Figure 2. Theoretical limits of Si and WBG unipolar components on-state resistance as a function of the maximum supported voltage, at 300 K.

Johnson has proposed to use the product of the breakdown electric field and the saturation velocity as a figure of merit (JFM), which determines the ultimate power-frequency capability of the material: JFM = $(E_c\, v_{sat}/\pi)^2$. Later, the following criterion was defined by Keyes: KFM = $\lambda\,(v_{sat}/\varepsilon_r)^{1/2}$, which provides a thermal limitation to the switching behavior of transistors. Baliga has proposed yet another figure of merit (BFM) for evaluating a semiconductor material. It is related to the operating losses of a high-power field-effect transistor: BFM = $\varepsilon_r\,\mu\,E_c^3$ (with μ the mobility of current carriers). However, this criterion was associated primarily with ohmic losses due to the specific on-resistance of the drift region and was used to assess the capabilities of a semiconductor from the standpoint of low-frequency devices. For the assessment of high-frequency devices, the losses associated with the commutations must also be considered. The criterion BHFM = $\mu\,E_c^2$, based on the assumption that switching losses are caused by the recharging input capacitance of a device, was proposed in [18]. Finally, Schneider proposed a figure of merit to assess the performances of high-voltage bipolar components, taking into account the thermal dissipation and maximum operating temperature of the semiconductor material [19]: SFM = $E_c\,(\mu_N+\mu_P)\,\lambda T_{max}$.

From Table 2, it can be noticed that the figures of merit for diamond are at least 40–50 times more than those of any other semiconductor material (except for Keyes' criterion). On the other hand, SiC polytypes and GaN have more or less similar figures of merit, which implies similar performances.

	Si	SiC (4H)	SiC (6H)	SiC (3C)	GaN	Diamond
JFM	1	215.1	277.8	277.8	215.5	81000
KFM	1	5	5.1	3.7	1.5	35.3
BFM	1	222.8	158.6	129.9	188.3	25319
BHFM	1	35.9	23.1	23.7	37	1629.6
SFM	1	64.4	39.5	19	30.8	5207.1

Table 2. Main figures of merit for WBG semiconductors compared with Si.

2.2. Wide band gap power devices

Collecting enough information about WBG devices in order to enrich the database of the existing CAD tool was a difficulty of this work. Indeed, these technologies are relatively recent and their market penetration is still at the beginning. Components switching times and losses, on-state resistances, etc., were for instance difficult to obtain. Consequently, an important bibliographical task has been performed in order to create a database sufficiently rich to be exploited, by consulting the scientific literature and manufacturer data sheets, and by participating to international conferences and exhibitions.

Currently, the only SiC semiconductor devices which are widely available are unipolar components (MOSFETs and Junction Field Effect Transistors, or JFETs). On the contrary, bipolar components as, e.g., insulated gate bipolar transistors (IGBTs), are still in research and development phase (some prototypes have nevertheless been presented in literature, see, e.g., [14] for a summary). GaN-on-Si switches have been introduced and commercialized for applications in power electronics converters. These switches benefit from fast switching times of GaN technology while maintaining a comparable cost with Si technology.

Currently, several manufacturers are commercializing WBG power devices. Those that will be considered further in this chapter include the following:

- JFETs available from *SiCED* and *SemiSouth*, with ratings from 500 V/5 A up to 1.2/1.7 kV with current capabilities as high as 52 A. These are normally off components, which means that no source-drain current is needed to keep the polarization between the gate and the source equal to zero.
- SiC MOSFETs currently available from *ROHM Semiconductor* and *Cree*, with ratings from 600 V/10 A up to 1.2 kV/100 A.
- Hybrid modules (Si MOSFET or CoolMOS, with a SiC antiparallel Schottky diode) produced by *Microsemi* (500 V/67 A or 600 V/143 A), which permit to reduce the switching losses compared to classical Si modules [20].
- GaN enhancement mode power transistors (EMPTs) produced by *EPC* with voltage ratings in the range from 40 V to 200 V and current capabilities from 3 A to 33 A.

- SiC Schottky diodes available from *Infineon*, *Fairchild*, *Cree*, *Semisouth*, etc., with ratings from 600 V/1 A up to 1.2 kV/30 A or 1.7 kV/25 A. Bipolar diodes and Junction Barrier Schottky (JBS) diodes will not be considered in this study.

Note that the database of WBG and classical Si devices will be completed over time in order to extent the design possibilities of the CAD tool. A version of the database is available from [21] but not reported here for the sake of conciseness.

It should also be noted that, even if the maximum working temperature of SiC material is theoretically superior to 700°C (see Table 1), for reasons of packaging, reliability, etc., the components currently available cannot be used at junction temperatures above 200°C (or even 175°C according to some manufacturers) [4]. Likewise, GaN power transistors from *EPC* should not be operated at a junction temperature higher than typically 125°C.

3. DC-DC converters modeling

Three types of models are commonly used in the design stages of electrical systems and components, namely, analytical models, simulation models (using dedicated software as, e.g., Saber or PSIM), and finite elements (FE) models. The choice of the type of model results from a trade-off between accuracy and computation time.

In this contribution, analytical models are adopted mainly for three reasons.

First, most of the analytical models that will be considered are available in the literature and well accepted among the researchers community. Some FE studies have also been conducted to confirm that the analytical and FE models show the same result tendencies. Second, analytical models have a lower computation time compared to the other types of models. This allows for exploring the entire search space in a reasonable amount of execution time when they are included in an optimization procedure. It is a key advantage for this work because the optimization procedure based on GA will require computing the values of the considered objectives a high number of times. Third, even if, in principle, analytical models are less accurate than the other types of models, this should not be taken as a limitation, at least in the scope of this study. Indeed, as the existing CAD tool compares together solutions obtained with the same models, a lack of accuracy in the computation of the objectives will be the same for all the solutions, and so will not affect the final choice of the designer.

The typical structure of an SMPS is shown in Figure 3. A DC input voltage is first converted into AC using a DC-AC (inverter) cell composed of power switches and diodes. A medium- or high-frequency transformer, which often comprises multiple windings, provides the electrical isolation and lowers the voltage levels. The AC voltage is then transformed using an AC-DC (rectifier) cell made of diodes and filtered with passive components (inductors and capacitors). Assuming only one output, the specifications of the converter are given by the three variables V_d, V_o, and P_o, respectively, the input and output voltages, and the output power. Heat sinks are associated with both cells in order to keep the junction temperatures of

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the power devices within acceptable limits. The DC output is typically regulated by means of a feedback control loop that employs a pulse-width modulation controller.

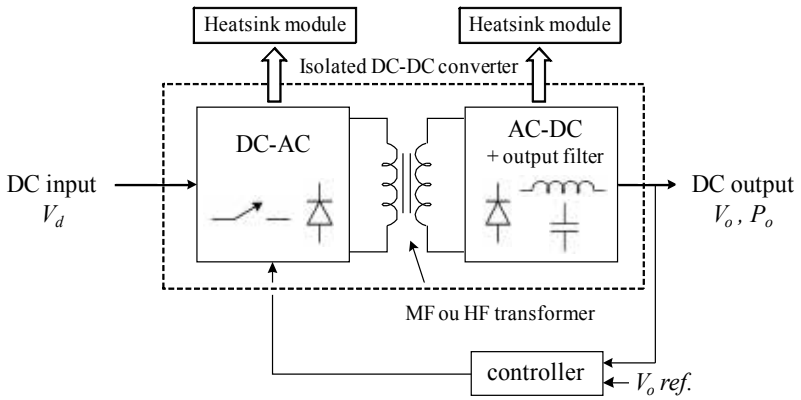

Figure 3. Typical structure of an SMPS with an intermediate medium- or high-frequency transformer.

Designing a system using optimization algorithms implies to use models which represent the different constituting parts of the isolated DC-DC converter under study. Indeed, the optimization procedures require multiple evaluations of several objective functions (e.g., the power losses and mass), while satisfying some constraints. Only electric and thermal models are of concern in this work. For the electrical aspect, the following parts need to be modeled:

- *Converter topology.* The flyback, forward, push-pull, half-bridge, and full-bridge topologies are retained as possible candidates for the realization of the DC-DC converter. The steady-state voltage and voltage waveforms are derived by the solution of ordinary differential equations, under some hypotheses [3].

- *Transformer.* The design of the transformer is based on the well-known area product method [22,23]. The transformer power dissipation has also to be estimated since it influences the temperature rise inside the component. The total power losses are divided into two parts: Joule losses in the windings (which are represented by the Dowell model [24] in the case of plain conductors, and by a modified Dowell model for Litz wire [25,26]) and losses in the magnetic core (modeled by a natural Steinmetz equation [27]).

- *Output filter.* The passive components (inductance and capacitance) are designed in order to limit the current and voltage ripples at the converter output [3].

- *Semiconductor power devices.* Conducting and switching losses have to be evaluated for the power devices, as they influence both the junction temperatures and the overall efficiency of the converter. Relevant data, as, e.g., on-state resistance and energies dissipated during the transitions (under given operating conditions), are stored into the database of the tool. In order to allow for a current sharing between the devices, the possibility to associate switches in parallel must also be taken into account.

For the thermal aspect, the following components need also to be modeled:

- *Heat sink modules*. They have to be designed in order to evacuate the heat produced by the conducting and switching losses of the semiconductor power devices, so that it is possible to keep their junction temperatures within acceptable limits. In this work, thermal resistance models are used, combined with information taken from the cooler manufacturer data sheets [28,29]. The heat transfer modes that will be considered further in the application examples are thermal conduction and natural convection (except, of course, for the space application).
- *Transformer*. In practice, the windings and magnetic core temperatures may not exceed the prescribed limits under the risk of being damaged. Thermal resistance networks are used to estimate the working temperatures and hot spots inside the transformer.

Note that all the employed analytical models are described in more detail in [1,21].

4. Existing CAD tool

The existing CAD tool, previously published by the authors [1,2], is briefly reviewed in this section. The basic structure of the tool, founded on a multiobjective optimization using GA, is shown in Figure 4.

The elitist nondominated sorting genetic algorithm, also known as NSGA-II [30], is used to perform search and optimization (such a choice is duly justified in [1,21]), whereas analytic models are used for the modeling of the power converters. The aim of this tool is to design converters optimized with respect to power loss, mass, and cost (the latter objective will not be considered in this chapter), while ensuring the satisfaction of constraints such as, e.g., appropriate limits on transformer or junctions temperature rise. Typical optimization variables (denoted $\boldsymbol{x}$ in Figure 4) are the switching frequency f_s, the current density J_w in the transformer windings, the maximum flux density B_m in the magnetic core, the transformer size *via* dimensionless coefficients k_1, k_2, k_3, the winding conductor diameter d_s, the core material (among FeSi alloys, ferrite, nanocrystalline material and amorphous material), the conducting material (among copper -Cu- and aluminum -Al-), the type of DC-DC converter topology (among those mentioned in the previous section), the type of semiconductor devices (among silicon-based IGBT and power MOSFET), and the number of these devices associated in parallel per switch N_{dev}, the number of DC-DC converter cells of the same topology which are associated in serial or parallel N_{cell} as well as the kinds of input and output connections (series or parallel) of these cells (see Figure 5 for $N_{cell} = 2$).

First, a random initial population is generated. The objective functions $\boldsymbol{F}(\boldsymbol{x})$ and constraints $\boldsymbol{g}(\boldsymbol{x})$ are evaluated based on the initial population and the specified analytical models of the isolated DC-DC converter. A convergence test is then performed to check for a termination criterion. If this criterion is not satisfied, the reproduction procedure using genetic operators (crossover and mutation) starts. A new population is so generated, and the previous steps are repeated until the termination criterion is verified. Otherwise, the Pareto front, i.e., the

nondominated solutions within the entire search space, is plotted and the optimization procedure ends.

The DC-DC converter modeling part, from which the objective functions are evaluated, is now briefly described. First, the DC-DC converter specifications (input and output voltages, output power, etc.) and the constraints are fed into the computer memory. Then based on the values of some of the optimization variables, the converter topology and the kinds of core and conductor materials are selected. Recall that the design equations of each converter topology and the specifications of the materials are prestored in the computer memory. Once the topology has been chosen, the stresses on the semiconductor power devices and the specifications of the filters and the transformer can be determined. Thus, the semiconductor devices with suitable ratings can be selected from the tool database, and the transformer and filters are designed. Hence, the total power loss of the magnetic components and the semiconductor devices is easily computed by using well-known formulae [31]. Then the heat sink is designed to keep the junction temperature rise of the semiconductor devices within the appropriate limits (typically 125°C for conventional Si-based components).

Finally, it should be noted that the main limitation of the CAD tool here described is that it can only be used in the first stages of the design procedure. In order to use it in the next phases, more accurate models of the converters should be considered.

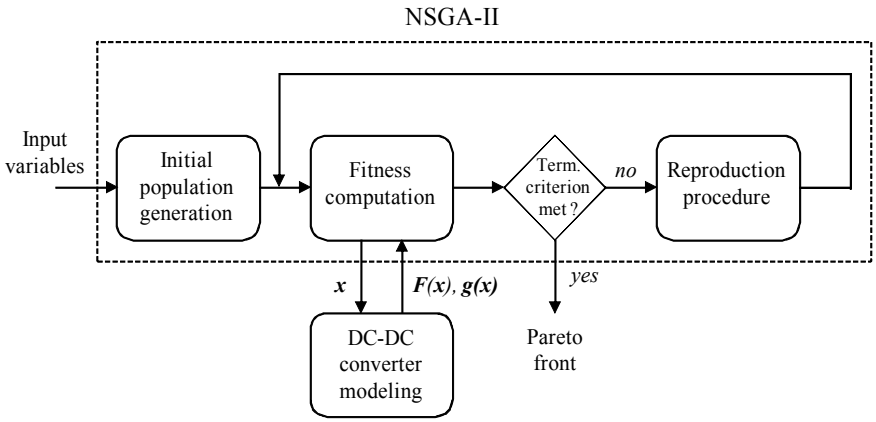

Figure 4. Basic structure of the CAD tool founded on multiobjective optimization using NSGA-II.

5. Design of a high-power DC-DC converter for auxiliary railway power supply

5.1. Specifications

Auxiliary power supplies are used in modern railways coaches to provide a continuous energy supply to auxiliary equipments such as lighting, air conditioning, pressure protection, etc.

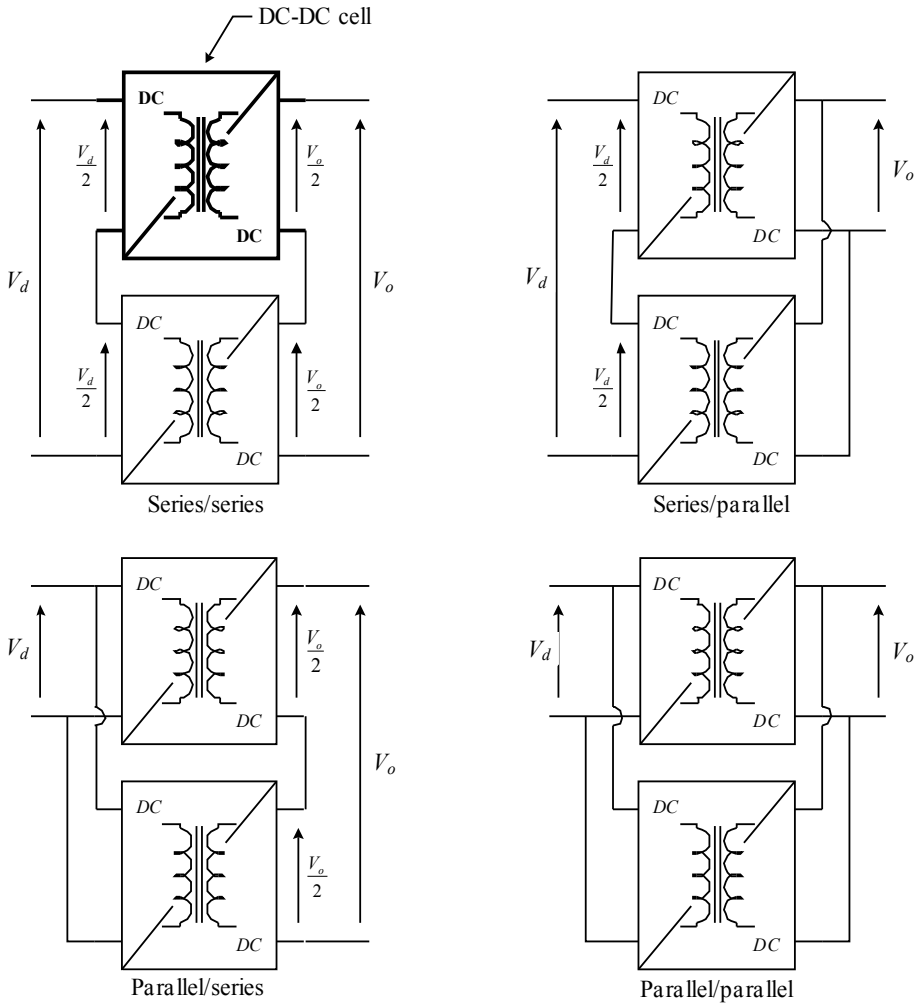

Figure 5. Possible associations between the DC-DC converters cells for $N_{cell} = 2$.

They are directly connected to the catenary and represent the interface between the overhead line and the vehicle onboard low voltage consumers. Currently, the galvanic isolation is realized by a heavy and bulky 50 Hz transformer. However, in order to reduce the size and mass of the devices (filters, transformer, etc.), the trend is to use new structures, which include an intermediate conversion stage using a lightweight MF transformer (typically several kilohertz) [32]. The principle scheme of such a structure to supply a three-phase 400 V AC consumer is illustrated in Figure 6. Note that only the part framed by the dashed line, which represents an SMPS of the type shown in Figure 3, will be subject to the MO optimization.

Some typical electrical specifications of an auxiliary railway SMPS are given in Table 3. These specifications match with a 1.5 kV DC catenary system. The continuous failure-free

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operation of the power supply must be guaranteed within the following limits of the DC supply voltage [33]:

$$0.67\ V_{d,nom} \le V_d \le 1.3\ V_{d,nom} \tag{2}$$

where $V_{d,nom}$ is the conventional nominal value of the catenary voltage.

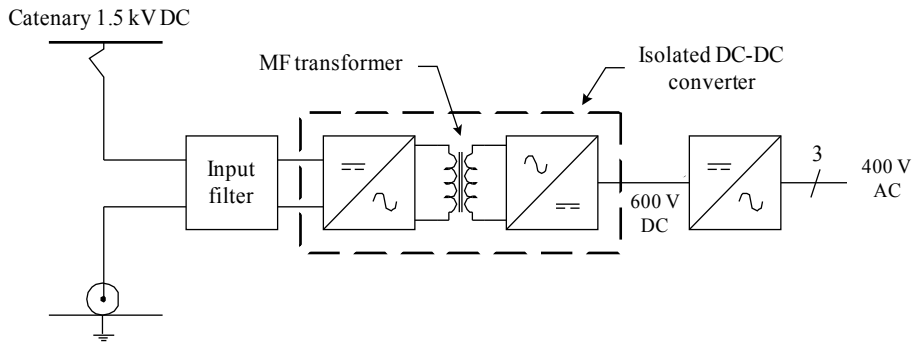

Figure 6. Principle scheme of a high-power SMPS with an intermediate isolated DC-DC conversion stage.

Minimum input voltage	$V_{d,min}$	1 kV
Maximum input voltage	$V_{d,max}$	1.95 kV
DC output voltage	V_o	600 V
DC output current	I_o	167 A
Output power	P_o	100 kW

Table 3. Typical specifications of an auxiliary railway SMPS matching with a 1.5-kV DC catenary system.

The optimization variables (denoted $\boldsymbol{x}$ in the previous section) are listed in Table 4. Recall that, in this contribution, the database of the CAD tool was enriched with WBG semiconductor power devices. Hence, the type of switching semiconductor devices can now be selected among Si IGBT, Si MOSFET, Si MOSFET with SiC antiparallel diode, SiC JFET, and SiC MOSFET. The rectifier diodes can be chosen, as for them, between Si or SiC Schottky devices.

The constraints that have to be ensured are of two natures: thermal and technological. The thermal constraints concern the semiconductor devices (maximum junction temperature limited to 150°C using SiC components) and the MF transformer (maximum temperatures for the windings and the magnetic core which cannot exceed 180°C and 125°C, respectively). From the technological aspect, the lower and upper bounds of each component of x are reported in the third column of Table 4. The current loss factor (defined from the Dowell model) is also

limited to 1.25, and some constraints must be added in order to verify that the windings can be inserted in the window area of the magnetic component.

Variables	Type	Bounds (continuous variables)	String length	Possible values (discrete variables)
Switching frequency f_s	Continuous	[1; 200] kHz	-	-
Transformer winding current density J_w	Continuous	[1; 6] A/mm^2	-	-
Transformer geometrical factor k_1	Continuous	[1; 5]	-	-
Transformer geometrical factor k_2	Continuous	[1; 5]	-	-
Transformer geometrical factor k_3	Continuous	[1; 2]	-	-
Maximum flux density in magnetic core B_m	Continuous	[0.01; B_{sat}] T	-	-
Winding conductor diameter d_s	Continuous	[0.04; 0.56] mm	-	-
Magnetic material	Discrete		2	{0;1;2;3}
DC-DC topology	Discrete		3	{0;1;2;3;4}
Number of parallel semiconductor devices per switch N_{dev}	Discrete		2	{1;2;3}
Type of switching semiconductor devices	Discrete		3	{0;1;2;3;4}
Number of DC-DC cells N_{cell}	Discrete		2	{1;2;3}
Conducting material	Zero-one		1	{0;1}
Input connection (series or parallel)	Zero-one		1	{0;1}
Output connection (series or parallel)	Zero-one		1	{0;1}
Type of rectifier diodes	Zero-one		1	{0;1}

Table 4. Optimization variables for the design of an auxiliary railway SMPS.

5.2. Results using SiC and Si technologies

The Pareto front obtained for the two-objective problem (minimizing the power losses and mass) is shown in Figure 7. These results have been obtained in 140 s CPU time, with a 3.4 GHz processor and 3 Gb RAM. The population size, i.e., the number of individuals in the front, and the number of generations were set to 100 and 500, respectively.

All the optimal solutions combine two DC-DC cells in full-bridge topology (series input and parallel output associations). The series input association permits to use semiconductor devices with lower voltage ratings than the maximum input voltage $V_{d,max}$ (=1.95 kV). The

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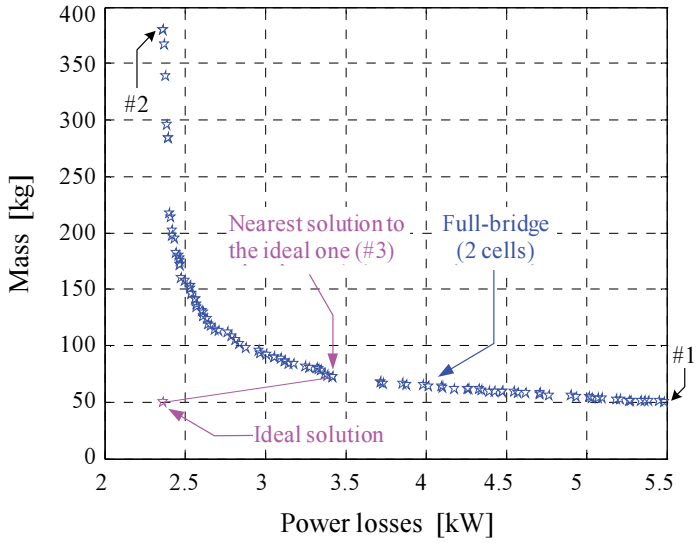

Figure 7. Pareto front of the two-objective problem using SiC and Si devices in the case of the design of a high-power SMPS (blue stars stand for optimal solutions in full-bridge topology).

parallel output association allows for the use of power devices with smaller current capabilities.

For every solution, the number of parallel semiconductor devices (1.2 kV/100 A SiC MOSFET) per switch is two. The rectifier diodes are all Si-based with ratings 1.7 kV/200 A. SiC Schottky diodes are not selected here because, to the best of our knowledge, such current capability is still not available and, in its current state of development, the CAD tool does not offer the possibility to connect several rectifier diodes in parallel.

The values of the other optimization variables are reported in Table 5 for three points of the Pareto front (see solutions 1 to 3 in Figure 7), including solution 3, which is the closest to the ideal one. This utopic solution is constructed by keeping the minimum of each objective separately. As can be seen, some of the variables have converged towards their optimal value. In all cases, the windings are composed of Litz wire (either made of aluminum or copper), with an optimal elementary conductor diameter of 0.2 mm, and the transformer is designed with a ferrite core whose geometrical factor k_3 is approximately 1.6. The maximum flux density B_m in the core is around 25% of the saturation value B_{sat} of the employed ferrites. Such a small value results from a trade-off between the two considered objectives, which can be explained as follows.

According to the area product method, which is used here to model the transformer, its mass m_{TFO} is linked to the maximum flux density by

$$m_{TFO} \propto B_{max}^{-3/4} \tag{3}$$

On the other hand, the natural Steimetz equation permits to express the magnetic loss density (in W/kg) as a function of B_m:

$$P_{magn} \propto B_{max}^{\beta} \tag{4}$$

with β varying between 2 and 2.5, depending on the selected core material. If B_m is doubled, m_{TFO} is multiplied by 0.59 (=$1/2^{3/4}$), whereas P_{magn} is multiplied by a value comprised between 4 and 5.65. Hence, the magnetic losses in the core, $P_{magn} \times m_{TFO}$, are multiplied by a factor between 2.36 and 3.33. Since the mass and the power losses have to be minimized jointly, it can be concluded that the gain in terms of mass with a high value of B_m does not compensate the ensuing losses. This is the reason of the relatively small values obtained for the maximum flux density B_m in this design example.

Note that the values of the switching frequency are not discussed here as a detailed analysis will be conducted in the following subsection.

No.	f_s [kHz]	J_w [A/mm^2]	k_1	k_2	k_3	B_m [T]	d_s [mm]	Magnetic material	Conducting material
1	22.2	3.27	3.11	3.73	1.61	0.09	0.2	Ferrite	Al
2	10.3	3.22	3.03	3.29	1.61	0.11	0.2	Ferrite	Al
3	4.3	2.32	2.41	2.77	1.59	0.13	0.2	Ferrite	Cu

Table 5. Analysis of three solutions of the Pareto front shown in Figure 7.

5.3. Comparison with Si technology only

The optimization procedure is now carried out using Si technology only, with approximately the same execution time as above. Hence, the two Pareto fronts using Si and SiC technologies are shown in Figure 8 for comparison.

Using SiC technology clearly leads to lighter power converters with reduced power losses. Let us compare, for example, the power losses at a given mass (say 100 kg). In Figure 8, the corresponding power converters dissipate 4.5 kW in Si technology against only 2.8 kW taking into account SiC devices, which corresponds to a 1.7% gain in terms of efficiency. Similarly, for a given power loss (say 4 kW), the gain in mass is 53% (150 kg in Si technology against 70 kg with SiC).

A detailed analysis of the two Pareto fronts shows that the only design variable which differs significantly from the use of one or the other technology is the switching frequency f_s. In this vein, Figures 9 and 10 show the variations of the switching frequency along the two Pareto fronts as functions of each objective. As can be seen, f_s is up to 22 kHz for the optimal solutions designed in SiC, against maximum 6.7 kHz using Si devices only.

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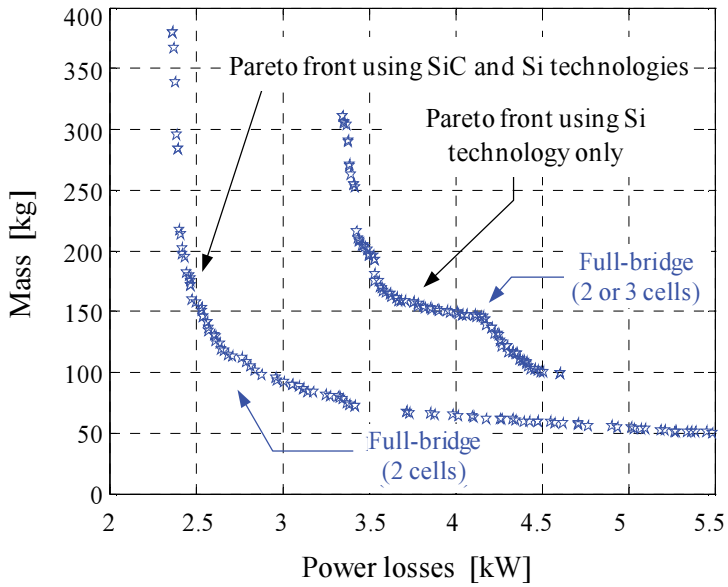

Figure 8. Pareto fronts of the two-objective problem in the case of the design of a high-power SMPS. Comparison between Si only and SiC+Si technologies (blue stars stand for optimal solutions in full bridge topology).

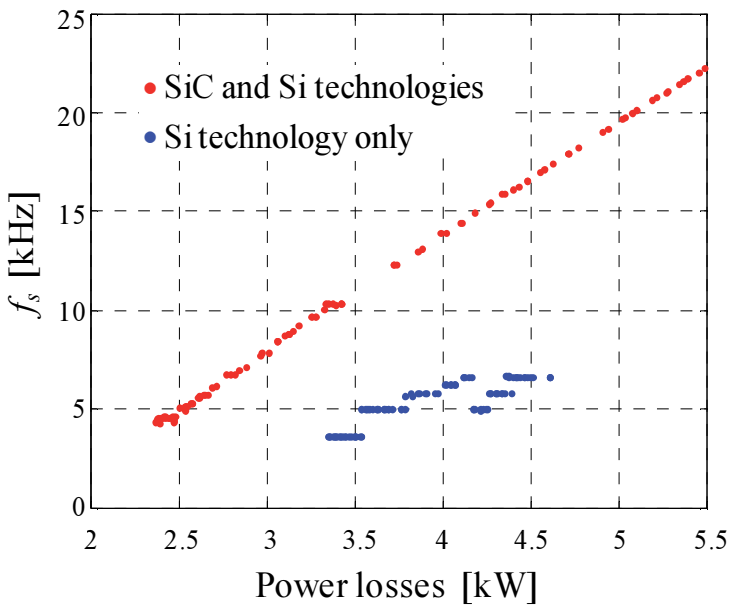

Figure 9. Variation of the switching frequency along the two Pareto fronts shown in Figure 8, as a function of the power losses.

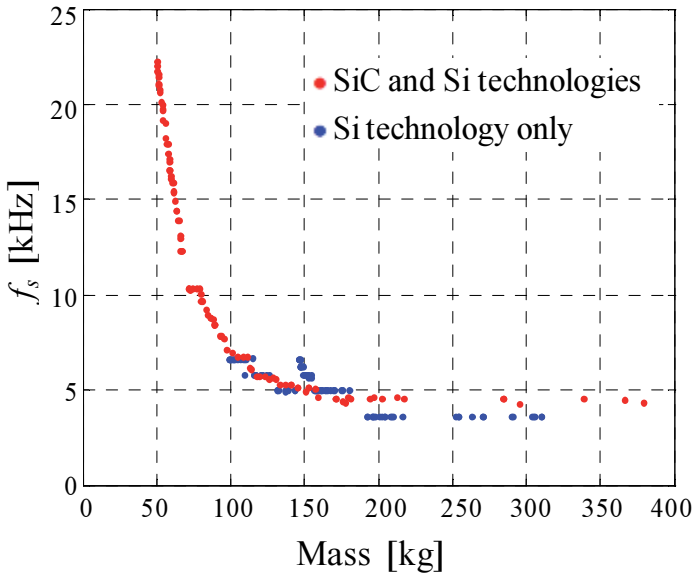

Figure 10. Variation of the switching frequency along the two Pareto fronts shown in Figure 8, as a function of the mass.

Several more comments can be made about the results shown in these figures. First, at a given switching frequency, the power losses are significantly reduced in SiC technology. For instance, a reduction of at least 1 kW is expected at 5 kHz, which corresponds to 1 % gain in efficiency. On the other hand, the masses are practically equal at 5 kHz as, for the considered application, the passive components largely contribute to the overall weight. The mass is, however, significantly lowered at higher values of the switching frequency by use of SiC devices.

Second, the variation of the switching frequency as a function of the power losses in SiC is more or less linear (see Figure 9), which can be explained by the fact that the total power loss is strongly impacted by the switching losses P_{sw}, proportional to f_s. On the other hand, the variation of f_s as a function of the mass can be justified as follows. As said above, the overall mass of the DC-DC converter is mainly dominated by the passive components and, more particularly, the mass of the MF transformer, which is linked to the switching frequency by

$$m_{TFO} \propto f_s^{-3/4} \tag{5}$$

according to the area product method. This result is more or less in line with the shape of the SiC-based evolution represented in Figure 10.

Finally, the power loss distribution (conduction *on* and switching *sw*) related to the devices composing one of the DC-DC cells is shown in Figure 11, considering two solutions of the

Pareto fronts (one on each front in Figure 8) at the same switching frequency of 5 kHz and with the same number of cells. Depending on the technology, the switching devices (*T*) are either 1.2 kV/150 A Si IGBTs or 1.2 kV/100 A SiC MOSFETs. For reasons already mentioned, the rectification stage of the DC-DC cell is made of Si diodes (*D*) with ratings 1.7 kV/200 A, whatever the case. As can be seen in Figure 11, a global power losses reduction of 36.2% is achieved or, even, 47.1% disregarding the losses due the diodes.

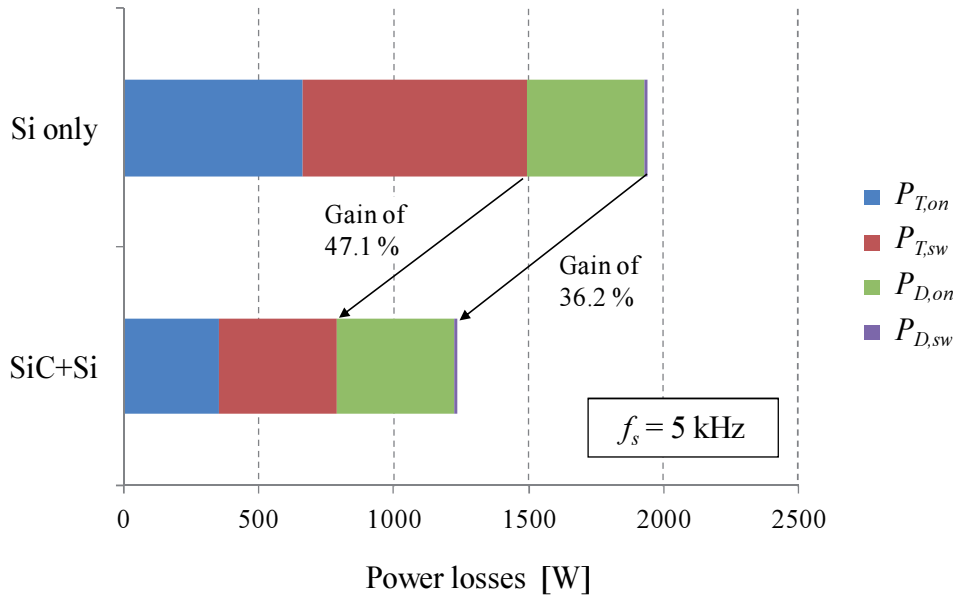

Figure 11. Power losses distribution in the semiconductor devices of one DC-DC cell of the high-power SMPS. Comparison between Si only and SiC+Si technologies, considering two solutions at the same switching frequency.

6. Design of a low-power DC-DC converter for space application

6.1. Specifications

Nowadays, SMPS are more and more used in aeronautics and for space applications. Figure 12 shows, for instance, the simplified architecture of a DC power distribution system embedded in a satellite where the primary power source consists of a solar array and batteries. Among all the electronic equipments connected to the main bus, several DC-DC power converters are used for the power matching between the DC interface and the different loads and batteries. These converters are subject to particular constraints related to the space environment that must be taken into account in the early stages of the design procedure. Typical examples of constraints are the presence of ionizing radiation, the absence of convection cooling, the degassing of certain materials, etc [34]. Their reliability is also of prime importance, which

implies *inter alia* that the converters are most often designed fault-tolerant, and that the power switches must be derated with respect to their current and voltage capabilities.

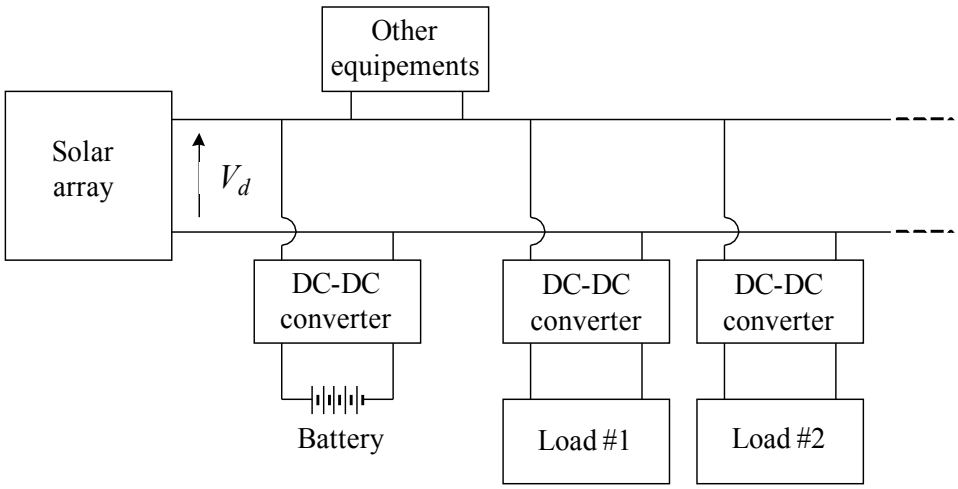

Figure 12. Simplified architecture of a DC power distribution system embedded in a satellite [35].

This section deals with the MO design of an SMPS that can be mounted either on the platform or on the payload side of a satellite (see Figure 13). The power supply has a somewhat more complex structure compared to the previous application example. Indeed, it consists of a cascaded (two stages) DC-DC converter with an input filter [21,36,37]. The front-end stage is used to achieve a step-down (buck) voltage conversion in continuous conduction mode, whereas the back-end stage is a multioutput current-fed converter with a push-pull topology (without output inductor) taken here as an example. The main operational characteristics of the circuit are as follows [37]. First, the switching frequency of the buck stage is twice that of the push-pull converter, which is operating at f_s. Second, one of the converter outputs (say V_{o1}) is controlled by adjusting the duty ratio D_B of the switch T_1. Finally, the switches T_2 and T_3 are controlled alternately with a duty ratio of 0.5 (i.e., the push-pull stage just behaves as a non-regulated DC transformer providing electrical isolation). It is important to keep in mind that other topologies can be chosen to realize the output stage as, e.g., a half-bridge or full-bridge converter. It should also be noted that the SMPS considered here is not fault tolerant, in the sense that there is no redundancy of its components, but it tolerates the short circuit of one switch, whatever the stage it belongs to. Even so, in this case, the availability of the power supply will be lost.

The typical electrical specifications of the above shown SMPS are given in Table 6. These are in accordance with the DC-DC converter data sheet available in [36]. The optimization variables x are reported in Table 7, with their lower and upper bounds. Note that the indices "1" and "2" are chosen to indicate the buck and output stages, respectively. The topology of the latter is considered as an optimization variable. The type of the magnetic core material does

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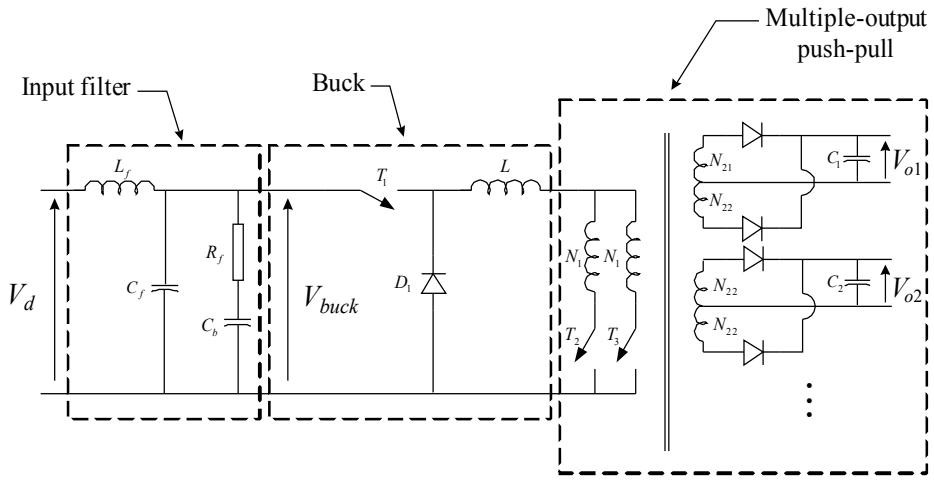

Figure 13. Principle scheme of an SMPS intended for a space application (in push-pull topology regarding the back-end stage).

not appear as an optimization variable here because, for the SMPS under consideration, only ferrite cores should be selected from the database due to technological constraints.

Minimum input voltage	$V_{d,min}$	67 V
Maximum input voltage	$V_{d,max}$	102 V
DC output voltage	V_{o1}	5 V
	V_{o2}	18.3 V
	V_{o3}	-18.3 V
	V_{o4}	6.15 V
	V_{o5}	6.8 V
DC output current	I_{o1}	1.9 A
	I_{o2}	0.65 A
	I_{o3}	0.45 A
	I_{o4}	0.3 A
	I_{o5}	0.3 A
Output power	P_o	33.5 W

Table 6. Typical specifications of an SMPS intended for a space application.

Variables	Type	Bounds (continuous variables)	String length	Possible values (discrete variables)
Switching frequency f_s	Continuous	[50; 250] kHz	-	-
Inductor winding current density $J_{w,1}$	Continuous	[1; 6] A/mm^2	-	-
Transformer winding current density $J_{w,2}$	Continuous	[1; 6] A/mm^2		
Maximum flux density in inductor core $B_{m,1}$	Continuous	[0.01; 0.38] T	-	-
Maximum flux density in transformer core $B_{m,2}$	Continuous	[0.01; 0.38] T		
Inductor wire diameter $d_{s,1}$	Continuous	[0.032; 0.5] mm	-	-
Wire diameter of transformer coil $d_{s,2}$	Continuous	[0.032; 0.5] mm		
DC-DC topology (output stage)	Discrete		2	{0;1;2}
Number of parallel semiconductor devices per switch $N_{dev,1}$	Discrete		2	{1;2;3}
Number of parallel semiconductor devices per switch $N_{dev,2}$	Discrete		2	{1;2;3}
Type of switch T_1	Discrete		3	{0;1;2;3;4}
Type of switches (output stage)	Discrete		3	{0;1;2;3;4}
Number of DC-DC cells N_{cell}	Discrete		2	{1;2;3}
Conducting material	Zero-one		1	{0;1}
Input connection (series or parallel)	Zero-one		1	{0;1}
Output connection (series or parallel)	Zero-one		1	{0;1}
Type of diode D_1	Zero-one		1	{0;1}
Type of rectifier diodes	Zero-one		1	{0;1}

Table 7. Optimization variables for the design of an SMPS intended for a space application.

6.2. Changes to the existing tool

In order to address this design problem, it was necessary to adapt the existing CAD tool to the specific requirements of the SMPS for space application. The main changes to the analytical models have been described in detail in [37]. They are briefly reviewed below:

- *Magnetic components*. The magnetic core is now selected from a database of ferrite cores (instead of being optimized from dimensionless geometric coefficients). In the case of a transformer, the RM ferrite core, which has an area product directly superior to the calculated value, is selected from the database. In the case of an inductor, a toroidal core is chosen instead of an RM type one for reasons of mechanical design. Note also that enameled wire is used for windings instead of Litz wire.
- *Derating of the semiconductor devices*. In order to improve the reliability of the power converters used in space environment, different actions must be taken at the early design stage [38]. Among them, a part stress analysis is always performed taking into account the

maximum operating temperature, which results, in particular, in a reduction of the voltage and/or current ratings of the various components. Thus, for this application, a 50% voltage derating of the semiconductor devices is applied. Their current capability is also derated according to the junction temperature value of the component. A 50% current derating is adopted up to a junction temperature of 70°C and, above this limit, the current capability declines linearly to zero at 110°C.

- *Cooling of the components.* As there is no exchange of heat by convection in the vacuum and radiation is negligible inside the satellite, the thermal models must be modified to take into account only the heat transfer by conduction. For this application, the various components are located on a heat-pipe cooled plate, which is assumed isothermal at 60°C. The thermal model of a semiconductor device is represented with two thermal resistances, one between junction and case and the other between case and cooled plate. Similarly, the cooling of a magnetic component is only by conduction through the core surface in contact with the plate (through an aluminum sole-plate). An equivalent circuit of thermal resistances is adopted to deal with the heat transfers between the various parts of the element itself.

Note also that the design of the input filter shown in Figure 13 was fully described in [39], as well as the optimization of its shunt damping circuit. Thus, in the present contribution, this part of the SMPS is not directly optimized by GA. Instead, the procedure to calculate the filter elements was implemented as exposed in [37].

6.3. Results using SiC and Si technologies

The Pareto front of the two-objective problem using SiC and Si devices is represented in Figure 14. As can be seen, the power losses are reduced as the proportion of SiC devices grows. The CPU time needed to obtain these results was 173 s, which is comparable to the execution time related to the previous application example (with the same population size and number of generations).

All the optimal solutions are designed with only one DC-DC cell (regarding the output stage), which corresponds to either a full-bridge or a push-pull configuration. The half-bridge topology is not retained here because, in that case, a capacitive divider is needed to obtain a voltage source behavior and the output filter inductor cannot be eliminated, which yields a higher number of passive components. It can be observed in Figure 14 that the full-bridge topology is interesting at low loss, but a higher mass since more semiconductor devices are needed, whereas the push-pull architecture is clearly the best trade-off between both objectives. The rectifier diodes are all Si-based with ratings 100 V/3 A for output 1 and 100 V/1 A for outputs 2 to 5. Indeed, the SiC diodes available from the current CAD tool database are rated at least for 600 V/1 A, which is much too high for the output voltage levels specified in Table 6.

The values of the other optimization variables are reported in Table 8 for six particular solutions, including solution 4, which is the closest to the ideal point. Most of them have converged towards their optimal value. In particular, it is noticed that the switching frequency

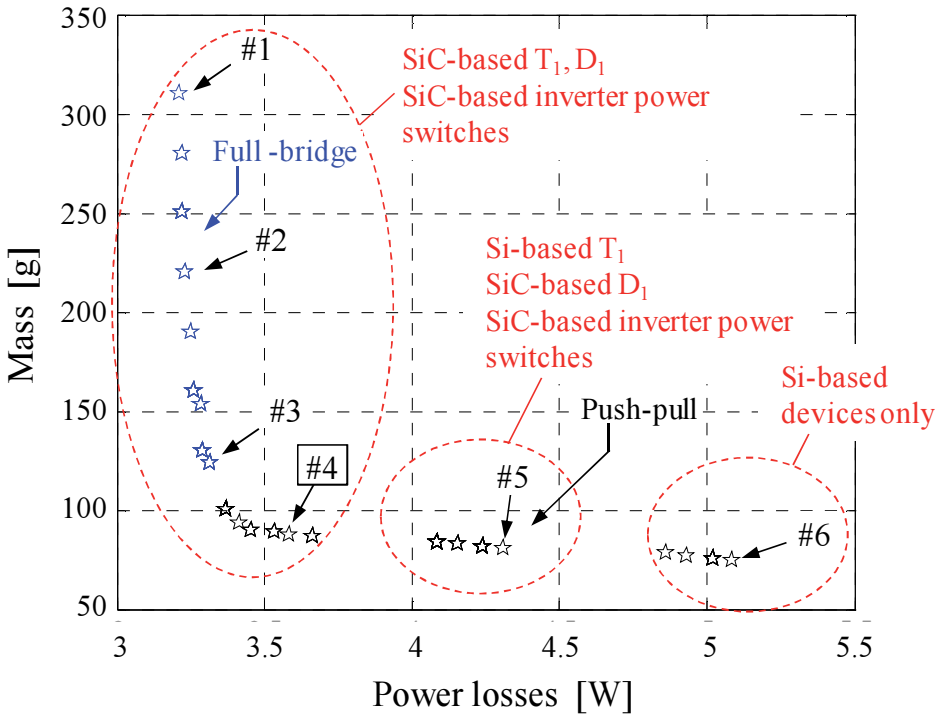

Figure 14. Pareto front of the two-objective problem using SiC and Si devices in the case of the design of a low-power SMPS (blue and black stars stand for optimal solutions in full-bridge and push-pull topologies, respectively).

remains practically unchanged along the Pareto front (but for solution 4 where f_s is equal to 141 kHz), which is in contrast with the previous design example.

In the power supply, the overall mass is distributed among the passive components (transformer, etc.) and the semiconductor power devices. The corresponding repartition is shown in Figure 15 for the six solutions of interest. Unlike the application of an auxiliary railway SMPS, it can be seen that the passive components are no longer the main contributors with respect to that criterion, and for certain solutions, their mass may even be much less than that of the semiconductor devices (see, e.g., solution 1). This can be justified from the fact that the mass of a ferrite core (say of RM8 type), which has a strong impact on the calculation of the mass linked to the passive components, can be estimated at 13 g, whereas the one of a JFET SiC 500 V/5 A is already about 15 g and several of them are needed to constitute only one switch of the output stage.

In the same way, Figure 16 shows the distribution of the power losses among the passive components and the semiconductor power devices. For the latter, the distinction is made between the conducting and switching losses. It can be observed that the total power dissipation is mainly due to the on-state power losses, whatever the solution. The switching losses are, as for them, growing in importance as the proportion of SiC devices decreases from

No.	f_s [kHz]	$J_{w,1}$ [A/mm²]	$J_{w,2}$ [A/mm²]	$B_{m,1}$ [T]	$B_{m,2}$ [T]	$d_{s,1}$ [mm]	$d_{s,2}$ [mm]	Transformer core	Conducting material	Diode D_1	Switch T_1	Switches (output stage)
1	123	2	3.5	0.37	0.05	0.04	0.33	RM8	Al	SiC 600 V/1 A	JFET SiC 500 V/5 A (6 in parallel)	JFET SiC 500 V/5 A (3 in parallel)
2	123	2	3.5	0.37	0.05	0.041	0.33	RM8	Al	SiC 600 V/1 A	JFET SiC 500 V/5 A (4 in parallel)	JFET SiC 500 V/5 A (2 in parallel)
3	123	2	3.5	0.37	0.11	0.04	0.33	RM8	Al	SiC 600 V/1 A	JFET SiC 500 V/5 A (2 in parallel)	JFET SiC 500 V/5 A
4	141	3.2	3.8	0.38	0.19	0.041	0.33	RM6	Al	SiC 600 V/1 A	JFET SiC 500 V/5 A (2 in parallel)	JFET SiC 500 V/5 A
5	124	3.6	3.8	0.38	0.13	0.04	0.33	RM8	Al	SiC 600 V/1 A	MOSFET Si 500 V/10 A (2 in parallel)	JFET SiC 500 V/5 A
6	124	3.6	3.8	0.38	0.22	0.04	0.33	RM7	Al	Si 150 V/1 A	MOSFET Si 500 V/10 A (2 in parallel)	MOSFET Si 500 V/10 A

Table 8. Analysis of six solutions of the Pareto front shown in Figure 14.

solutions 1 to 6, and the power losses in the passive components are about one order of magnitude less than the conduction losses.

6.4. Comparison with Si technology only

For comparison, the two Pareto fronts with and without including the selection of SiC devices in the optimization procedure are shown together in Figure 17. As can be observed, the two Pareto fronts merge each other when the objective of mass is preferred, which is consistent with the results reported in Figure 14 (where the lighter solutions are Si-based only). For a given mass (say 100 g), the power supply dissipates 4.6 W with Si against only 3.4 W, taking into account SiC devices, which corresponds to a 3.6% gain in terms of efficiency. Note also that all the solutions obtained with Si technology only correspond to one DC-DC cell in push-pull topology.

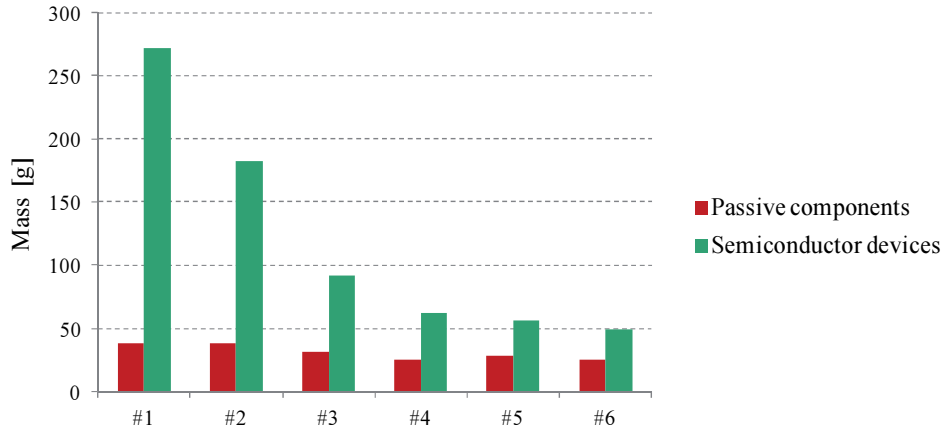

Figure 15. Repartition of the masses between the passive components and the semiconductor power devices for the six particular solutions in Table 8.

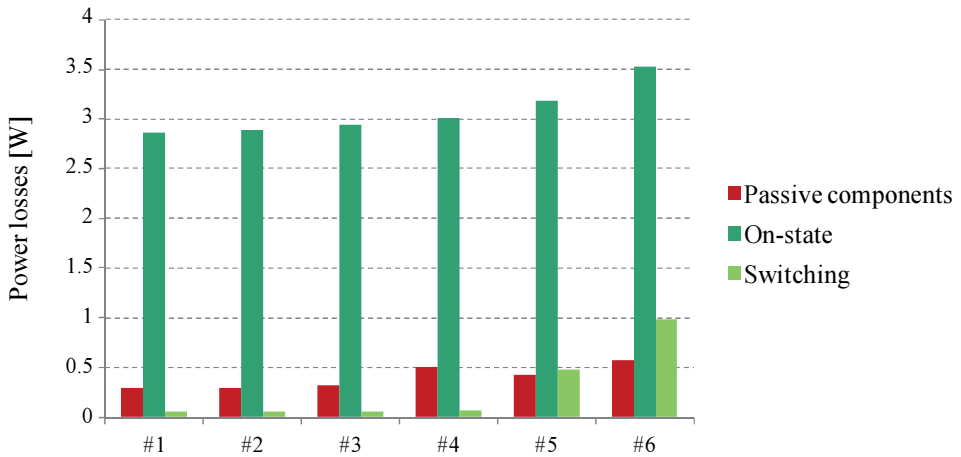

Figure 16. Distribution of the power losses among the passive components and the semiconductor devices (on-state and switching power losses) for the six particular solutions in Table 8.

Finally, Figure 18 compares the power losses in the semiconductor devices, with and without SiC. To that end, two solutions of the Pareto fronts having the same mass of 100 g (one on each front in Figure 17) are selected. The switching frequency is equal to 100.2 kHz for the Si solution and to 119.9 kHz for the SiC one. Globally, a power losses reduction of 25.3% is obtained using SiC JFETs instead of Si MOSFETs as switching devices. As can be observed, the switching losses in the power transistors ($P_{T,sw}$) are more particularly decreased (a gain of 97% is achieved in this case). On the other hand, as above-mentioned, all the rectifier diodes are Si-based, and that even for the solutions designed with SiC components. This is the reason why, in Figure

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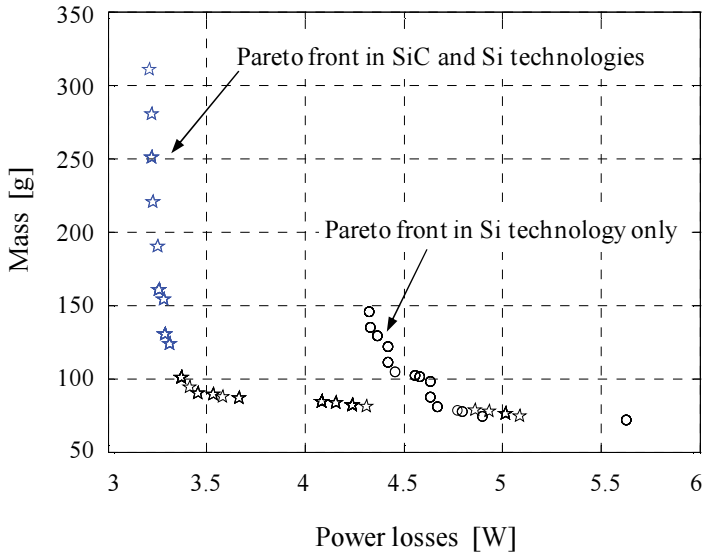

Figure 17. Pareto fronts of the two-objective problem in the case of the design of a low-power SMPS. Comparison between Si only and SiC+Si technologies (Blue and black stars stand for optimal SiC+Si solutions in full-bridge and push-pull topologies, respectively; black circles correspond to Si only solutions in push-pull topology).

18, the conduction losses of the diodes $P_{D,on}$ (≅2.8 W) are practically unchanged from one technology to the another. Still, the use of SiC to implement the freewheeling diode D_1 of the buck stage (the latter operating at twice de switching frequency f_s) allows for gain of 52.5% as regards the turn-off losses of the diodes $P_{D,sw}$.

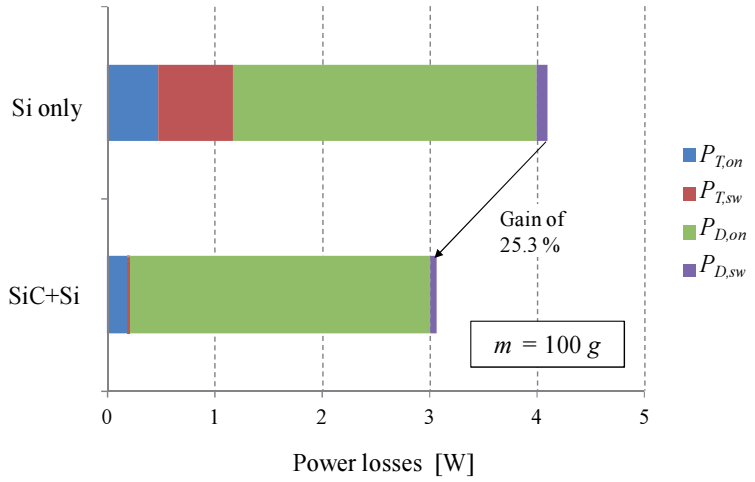

Figure 18. Power losses distribution in the semiconductor devices of the low-power SMPS. Comparison between Si only and SiC+Si technologies, considering two solutions having the same mass of 100 g.

7. Conclusion and perspectives

In this chapter, power losses and mass of optimally designed Si- *vs*. SiC-based isolated DC-DC power converters have been compared in quantitative terms. Two application examples operating at very different output power levels have been studied: a 100 kW auxiliary railway SMPS and a multiple output 33.5 W SMPS intended for a space application. To that end, a CAD tool dedicated to the MO optimization of isolated DC-DC converters and based on genetic algorithms (NSGA-II in particular) has been employed. Fast analytical models have been used to account for the electrical and thermal phenomena occurring inside the power converters. An important effort has been made to enrich the database of the existing tool with WBG devices (mainly SiC) currently available from manufacturers. The results show clearly that the SiC technology leads to the design of lighter SMPS, with less power losses compared to Si technology only. Besides, the use of the MO optimization CAD tool permits to evaluate the gains in terms of power losses and mass from one technology to the other, which is an advantage.

In future work, the packaging aspects using, e.g., analytical formulas accounting for the component integration in the power converter [40] and electromagnetic compatibility considerations (constraints on the voltage and current gradients) should be included in the tool. Performing a sensitivity analysis could be another perspective. Such an analysis would be useful to give a designer with important information about the stability of one particular optimal solution against others. It should also be reminded that the CAD tool used in this study is a predesign tool based on simple and fast analytical models. For example, rapid transients on switches and parasitic capacitive effects in the magnetic components are not taken into account. Once the optimal solution is chosen from the tool and the designer know-how, finer models have to be employed around that particular design configuration in order to refine the solution, at the cost of higher computational burden (performing, e.g., transient circuit simulations or using numerical methods such as the FE technique). Lastly, it should be noted that, in this study, GaN-based power transistors were not selected for the space application because their voltage ratings in the database are still too low. Yet since in a near future the commercial offer concerning WBG components is expected to drastically increase, the tool database will be completed over time and, hence, the design possibilities considerably extended.

Author details

O. Deblecker*, Z. De Grève and C. Versèle

*Address all correspondence to: olivier.deblecker@umons.ac.be

Electrical Engineering Division, Faculty of Engineering, University of Mons (UMONS), Mons, Belgium

http://dx.doi.org/10.5772/61018

References

[1] Versèle C., Deblecker O., Lobry J. A computer-aided design tool dedicated to isolated DC-DC converters based on multiobjective optimization using genetic algorithms. COMPEL: International Journal of Computations and Mathematics in Electrical and Electronic Engineering. 2012; 31(2): 583–603.

[2] Versèle C., Deblecker O., Lobry J. A decision-making aid tool dedicated to the design of auxiliary railway power supplies. European Journal of Electrical Engineering. 2011; 14(4): 421–450.

[3] Mohan N., Undeland T., Robbins W. Power Electronics: Converters, Applications and Design (3rd ed.). Hoboken (NJ): Wiley; 2003.

[4] Millan J., et al. A survey of wide band gap semiconductor power devices. IEEE Transactions on Power Electronics. 2014; 29(5): 2155–2163.

[5] Civrac G. Vers la réalisation de composants haute tension, forte puissance sur diamant CVD. Développement des technologies associées. PhD thesis. Institut National Polytechnique de Toulouse; 2010.

[6] Kaminsky N. State of the art and the future of wide-band gap devices. Proceedings of the 13th Conference on Power Electronics and Applications, EPE'09, September 2009, Barcelona, Spain.

[7] Biela J., et al. SiC versus Si—evaluation of potentials for performance improvement of inverter and DC–DC converter systems by SiC power semiconductors. IEEE Transactions on Industrial Electronics. 2011; 58(7): 2872–2882.

[8] Microsemi. Gallium nitride (GaN) versus silicon carbide (SiC) in the high frequency (RF) and switching power applications. http://www.digikey.com/Web%20Export/Supplier%20Content/Microsemi_278/ PDF/Microsemi_GalliumNitride_VS_SiliconCarbide.pdf?redirected=1 (accessed 2 Dec. 2013).

[9] Ozpinci B., et al. Comparison of wide bandgap semiconductors for power applications. Proceedings of the 10th Conference on Power Electronics and Applications, EPE'03, September 2003, Toulouse, France.

[10] Leroy F., et al. A very high frequency step-down DC/DC converter for spaceborne envelope-tracking SSPA. Proceedings of International Microwave Symposium, IMS'2014, June 2014, Tampa Bay (FL), USA.

[11] De Grève Z., et al. Comparison of the influence of Si and SiC seminconductor devices on power loss and weight of multiobjective optimal designed power converters. International Journal of Applied Electromagnetics and Mechanics. 2013; 43(1–2): 51–64.

[12] Schokley W. Introductory remarks on silicon carbide, a high-temperature semiconductor. Pergamon Press; 1960.

[13] Opzinci B., Tolbert L. M. Comparison of wide-bandgap seminconductors for power electronics applications. http://web.ornl.gov/~webworks/cppr/y2001/rpt/118817.pdf (accessed 19 February 2014).

[14] Mousa R. Caractérisation, modélisation et intégration du JFET de puissance en carbure de silicium dans des convertisseurs haute température et haute tension. PhD thesis, Institut National des Sciences Appliquées de Lyon; 2009.

[15] Bijeev N.V., et al. Design and realization challenges of power supplies for TWT. Proceedings of IEEE International Vacuum Electronics Conference, IVEC'2011, February 2011, Bangalore, India.

[16] Krämer M. C. J. C. M. Gallium nitride-based microwave high-power heterostructure field effect transistors—design, theory and characterization. PhD thesis. Technische Universiteit Eindhoven; 2006.

[17] Lebedev A. A., Chelnokov V. E. Wide-gap semiconductors for high-power electronics. Semiconductors 1999; 33(9): 999–1001.

[18] Baliga B. J. Power semiconductor device figure of merit for high-frequency applications. IEEE Electron Device Letters 1989; 10(10): 455–457.

[19] Schneider H., Sanchez J., Achard J. The diamond for power electronics devices. Proceedings of the 11th Conference on Power Electronics and Applications, EPE'2005, September 2005, Dresden, Germany.

[20] Richmond J. Hard-switching silicon IGBTs ? Cut switching losses in half with silicon carbide Schottky diodes. Applications note: CPWR-AN03 Rev. B; 2003.

[21] Versèle C. Contribution à l'optimisation multiobjectif de convertisseurs électroniques de puissance. Application aux convertisseurs continu-continu isolés. PhD thesis, University of Mons; 2012.

[22] McLyman W. T. Transformer and inductor design handbook (3rd ed.). New York: Marcel Dekker Inc.; 2004.

[23] Hurley W. G., Wölfle W. H., Breslin J. G. Optimized transformer design: inclusive of high frequency effects. IEEE Transactions on Power Electronics. 1998; 13(4): 651–659.

[24] Dowell P. L. Effects of eddy currents in transformer windings. Proceedings of IEEE. Aug. 1966; 113(8).

[25] Gu W.-J., Liu R. A study of volume and weight vs. frequency for high-frequency transformers. Proceeding of the 24th IEEE Power Electronics Specialists Conference, PESC, June 1993, Seattle (WA), USA.

[26] Maniktala S. Switching power supply design and optimization. New York: MacGraw-Hill Education; 2004.

[27] Van den Bossche A., Valchev V. C., Melkebeek J. Measurement and loss model of ferrites with non sinusoidal waveforms. Proceeding of the 35th IEEE Power Electronics Specialists Conference, PESC, June 2004, Aachen, Germany.

[28] Lee S. How to select a heat sink. Aavid technical papers. http://www.aavidthermalloy.com (accessed 19 February 2014).

[29] Extrusion selection guide power profiles for the European market, 2002. http://www.aavidthermalloy.com (accessed 19 February 2014).

[30] Deb K., et al. A fast and elitist multiobjective genetic algorithm: NSGA-II. IEEE Transactions on Evolutionary Computation 2002; 6(2): 182–197.

[31] Application manual by Semikron, 2010. http://www.semikron.com/skcompub/en/application_manual-193.htm (accessed 30 Aug. 2010).

[32] Deblecker O., Moretti A., Vallée F. Comparative study of soft-switched isolated DC-DC converters for auxiliary railway supply. IEEE Transactions on Power Electronics. 2008; 23(5): 2218–2229.

[33] Vinnikov D., Bolgov V. Efficiency optimization of the high-power isolated DC-DC converters through THD and losses reduction in isolation transformers. Proceedings of the International Conference on Renewable Energies and Power Quality, ICREPQ, April 2009, Valencia, Spain.

[34] Santos M., et al. Switch mode power supply design constraints for space applications. Proceedings of the 6th Conference on Telecommunications, ConfTele, May 2007, Peniche, Portugal.

[35] Erickson R. W., Maksimovic D. Fundamentals of Power Electronics (2nd ed.). New York: Springer Science; 2001

[36] LPLC Integrated 40W DC/DC converters, Datasheet Thales Alenia Space, 2009. http://www.thalesgroup.com (accessed 9 Nov. 2012).

[37] O. Deblecker, et al. Multiobjective optimization of a power supply for space application using a flexible CAD tool. Proceedings of the 15th Conference on Power Electronics and Applications, EPE'13—ECCE Europe, September 2013, Lille, France.

[38] Wallecan F. Reliability of Spacecraft Power Systems, 2011. http://www.grepes.be/PDF/ Journee_GREPES_2011_03_Thales.pdf (accessed 9 Nov. 2012).

[39] Middlebrook R. D. Design techniques for preventing input-filter oscillations in switched-mode regulators. Proceedings of the 5th National Solid-State Power Conversion Conf., POWERCON 5, May 1978, San Francisco (CA), USA.

[40] Popovic J. Improving packaging and increasing the level of integration in power electronics. PhD thesis, Delft University of Technology; 2005.

Chapter 6

Novel Developments and Challenges for the SiC Power Devices

Yintang Yang, Baoxing Duan, Song Yuan and Hujun Jia

Additional information is available at the end of the chapter

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Abstract

Silicon Carbide (SiC) is believed to be a revolutionary semiconductor material for power devices of the future; many SiC power devices have emerged as superior alternative power switch technology, especially in harsh environments with high temperature or high electric field. In this chapter, the challenges and recent developments of SiC power devices are discussed. The first part is focused on SiC power diodes including SiC Schottky barrier diode (SBD), SiC PiN diodes (PiN,) SiC junction/Schottky diodes (JBS), then SiC UMOSFETs, DMOSFETs and several MESFETs are introduced, and the third part is about SiC bipolar devices such as BJT and IGBT. Finally, the challenges during the development of SiC power devices, especially about its material growth and packaging are discussed.

Keywords: Silicon Carbide, Power Device, Diode, MOSFETs, MESFETs

1. Introduction

The first-generation and second-generation semiconductor materials are represented by silicon (Si) and gallium arsenide (GaAs), respectively. Wide band gap materials, such as silicon carbide (SiC) and gallium nitride (GaN), are known as the third generation semiconductor materials. SiC was discovered in 1824 by Berzelius during his diamond synthesis experiment. The first use of SiC was as an abrasive. This was followed by electronic applications. In the beginning of the 20th century, SiC was used as a detector in the first radios, and then became

popular since 1907 when Henry Joseph Round produced the first LED by applying voltage to a SiC crystal and observing yellow, green, and orange emissions at the cathode. This attracted much of the electronic researchers' attention and about half a century ago, the potential of SiC in the semiconductor industry was recognized. Compared with Si, the most widely-used semiconductor material, SiC has many remarkable electronic properties including wide band gap, large critical electric field, high thermal conductivity, high electron saturation velocity, chemical inertness, and radiation hardness [1-3]. These excellent properties make SiC very well-suited for high-voltage, high-power, and high-temperature applications.

SiC power devices began to be developed during the 1970s. Based on the efforts of many researchers, great improvement had been achieved in its crystal quality and fabrication technology during the 1980s, then various kinds of SiC devices were developed, and their performance has rapidly improved.

Nowadays, the primary theoretical stage of SiC power devices had been completed. The commercial availability stage is developing rapidly; process technology, such as single-crystal substrate and device fabrication processes, has had great progress. Since 2001, Infineon Corporation started to supply SiC Schottky diodes. Now SiC diodes, MOSFETs, JFTs, BJTs, and other SiC three-terminal devices are available, CREE, Toshiba, STMicroelectronics and other companies have the ability to supply SiC power devices.

However, the main obstacles for the development of SiC-based devices are the quality and costs of SiC materials compared with its Si-based counterparts. With the recent progress in the process of SiC epitaxial materials, it is feasible to obtain high-quality 4H-SiC substrates and epilayers, and thus achieve excellent power performances for SiC power devices. For instance, 100-mm 4H-SiC substrates and epilayers are readily available for manufacturing power devices. Since more and more researchers and companies are paying attention to SiC materials, a massive drop in costs is forthcoming and affordable costs can be expected in the near future; which, in turn, will promote the development of SiC power devices.

2. Silicon carbide diode

Power diodes are the key components in modern power applications. The classical rectification function was upgraded by high demands of turn-on and turn-off speeds. In order to fabricate SiC power devices, ohmic contacts play a very important role in the signal transfer between the semiconductor and the external circuitry. A large number of ohmic contacts materials have been investigated during the last decades, both in terms of structural characterization and electrical performance. For ohmic contacts on the n-type SiC material, the most promising metal is nickel (Ni). It has been demonstrated that Ni films annealed in the range of 900-1000ºC can form good ohmic contacts on n-type SiCs with a specific contact resistance of $1\times10^{-6}\ \Omega\cdot cm^2$ [4]. For the p-type materials, due to the higher Schottky barrier, ohmic contact formation is even more difficult than n-type materials. Much research has been focused on aluminum/titanium (Al/Ti) contacts, which give a specific contact resistance of about $10^{-5}\Omega\cdot cm^2$ [5].

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2.1. Schottky Barrier Diode (SBD)

As a unipolar device, SBD has zero reverse recovery current. Figure 1 shows a general structure of SiC SBD; it is formed by an electrically nonlinear contact between a metal and a semiconductor bulk region. SBD fabricated by SiC offers a new degree in the design of power circuits, which has been commercially available since 2001. The most remarkable advantage of SiC SBD is the continuing increase in blocking voltage and conduction current ratings, which have been increased from the initial 300 V, 10 A and 600 V, 6 A [6] to the current 600 V, 20 A [7]. Furthermore, it is expected that SBD can be applied with a blocking voltage up to 2,000 V (as merged solutions also up to 3 kV) [8]. 4H-SiC with field plate terminal technology had been reported for the first time with a breakdown voltage of 1,750 V [9]. It is even foreseen that this type of diode may replace Si bipolar diodes in medium-power motor drive modules. Due to the absence of reverse recovery charge in SBD, it has an extremely fast turn-on performance, which is well suited for high-speed switching applications and for drastically reducing the dynamic losses for typical circuits. The high thermal conductivity of SiC is also a great advantage for SiC SBD in comparison with Si and GaAs diodes since it allows the SBD to operate at higher current density ratings with smaller size cooling systems. However, its reverse leakage current is large, especially at high temperatures, due to its lower built-in potential barrier.

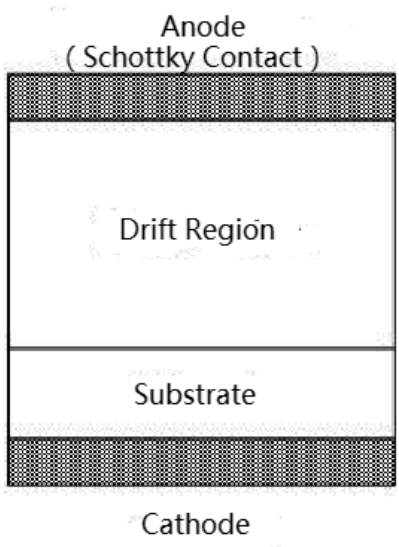

Figure 1. Conventional structure of SiC SBD.

2.2. Silicon carbide PiN diodes (PiN)

Owing to the absence of conductivity modulation effects, the drift region resistance of SBD increases so fast with the rise of breakdown voltage, so the maximum breakdown voltage of SBD cannot compete with PiN diodes due to the unacceptably large ON-state resistance.

Figure 2 shows a general structure of a SiC PiN diode, it consists of a highly doped n-type substrate, a lightly doped n-type epitaxial layer with specified thickness, and a highly doped p-type region for the anode. The advantage of the SiC PiN diode is its low leakage current and low ON-state voltage drop in high current conduction due to minority carrier injection in the epitaxial drift region resulting in conductivity modulation. However, conductivity modulation causes significant reverse recovery current during switching, which is undesirable because it causes additional turn-on loss in the active switch. Since SiC PiN diodes are gaining more and more attention due to its higher breakdown voltage and smaller size and weight, its switching speed has been greatly improved. Recently, Johji Nishio et al. have fabricated the mesa SiC PiN diodes, which have a blocking voltage of 10.2 kV [10]. In 2007, Cree Company has reported a 8.7×8.7 mm^2 SiC PiN diodes with the blocking voltage of 10 kV, as is shown in Figure 3 [11]. However, it has been reported that high power SiC PiN diodes exhibit an increase in the static forward voltage drop after exposing it to long-term operation during the test [12]. Various physical characterization techniques have shown that structural defects would be created in the epilayers during the operation. Encouragingly, Cree researchers have reported [13] that a process modification, which suppresses this degradation phenomenon, has been found but they have not released any details. Tsunenobu Kimoto et al. have reported 15 kV SiC PiN diodes with various junction terminal technologies [14]. In Ref. [15], 4H-SiC PiN had been applied in high temperature and high power circumstance with the breakdown voltage of 1,000 V.

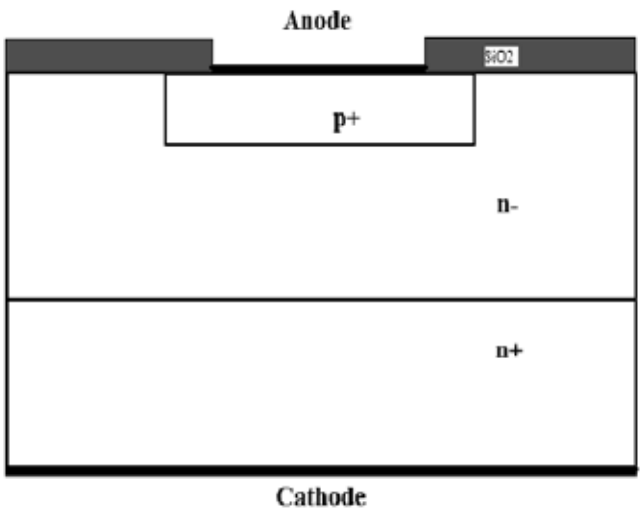

Figure 2. Conventional structure of SiC PiN.

2.3. Silicon carbide junction/schottky diodes (JBS)

Schottky rectifiers are expected to dominate in power devices with a blocking voltage below 3 kV. However, the reverse leakage current of SBD is generally excessive, particularly at high

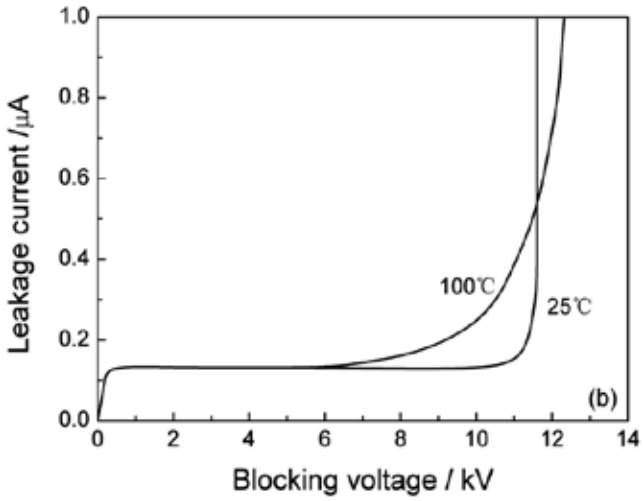

Figure 3. Blocking voltages characteristics of 10 kV SiC PiN diodes [11].

temperatures, due to lower Schottky barrier at high reverse voltage. The second-generation SiC diodes usually combine the attractive benefits of low ON-state voltage drop of a Schottky contact and the high blocking voltage of PiN diodes. These diodes have Schottky-like ON-state and switching behavior and PiN-like OFF-state characteristics at the same time. The basic JBS diode is fabricated by merging a Schottky diode and PiN diode structure [16]. Figure 4 shows a general structure of the SiC JBS; it consists of interleaved Schottky and p+ doped regions.The adjacent pn junction is used to suppress the rise of the electric field at the Schottky junction. When operating at voltages lower than the turn-on voltage of the pn junction, JBS exhibits faster switching speed than PiN diodes due to the absence of minority carrier injection. In recent time, Cree has manufactured a series of JBS with voltage ratings of 300, 600, and 1200 V and single-die current ratings from 1 to 10 Amps. In conclusion, the ON-state and switching characteristics of JBS are similar to Schottky diodes. The blocking characteristic is optimized due to the merged PiN diode structure compared with the SiC SBD.

3. Silicon carbide unipolar devices

3.1. Silicon carbide MOSFETs

Metal oxide semiconductor field effect transistors (MOSFETs) have been of interest since Si devices have become the most successful devices. Due to the excellent material properties of SiC, SiC power MOSFETs can operate at higher switching frequency and operating temperatures compared with conventional Si MOSFETs. It has been expected to be the next-generation switching device to replace conventional Si power devices in many applications. The first SiC power MOSFET was demonstrated in 1994 in the form of a vertical trench gate structure (UMOSFET) [17]. The reported device had a breakdown voltage of 150 V and specific on-

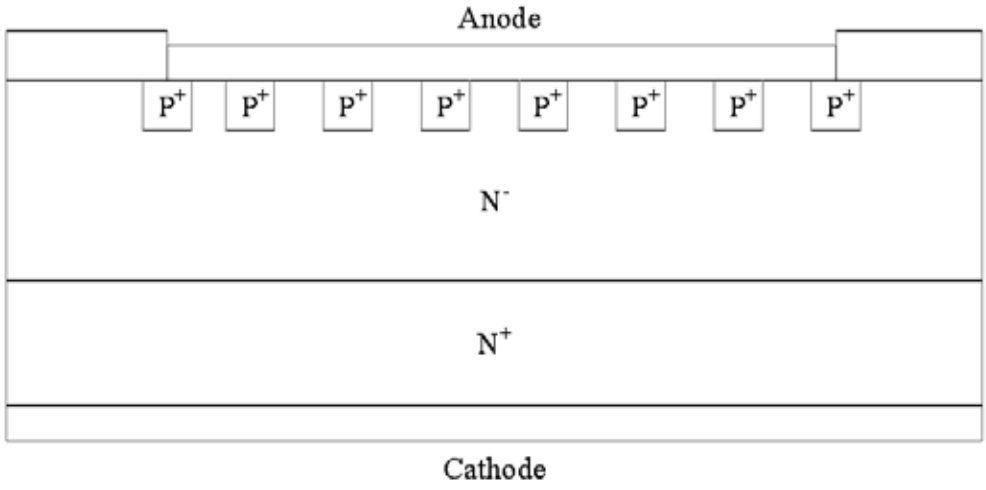

Figure 4. Conventional structure of SiC JBS.

resistance of 3.3 mΩ·cm^2. The breakdown voltage of the device was restricted by the high electric field in the gate oxide at the trench corner. To avoid the high electric field in a UMOSFET, a SiC planar gate MOSFET with a p-base formed by a double implantation MOS process was fabricated (DMOSFET), this 6H-SiC DMOSFET has a breakdown voltage of 760 V based on a 10μm-thick and 6.5×10^{15} cm^3-doped n-type drift layer. [18]. Figure 5 is the schematic diagram of the structure of the typical UMOSFET (UMOS) and DMOSFET (DMOS).

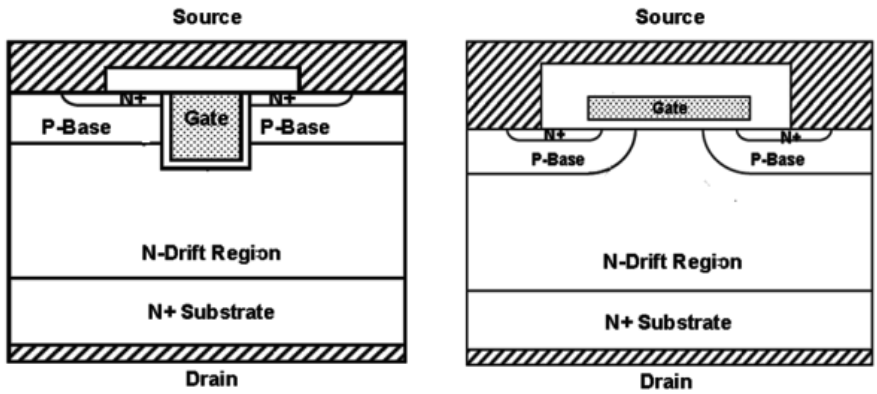

Figure 5. Schematic diagram of SiC (a) UMOS and (b) DMOS.

Later on, a 10 kV, 123 mΩ·cm^2 4H-SiC power DMOSFET was reported [19]. The effective channel carrier mobility is only 22 cm^2/V·s. However, the very low inversion channel electron mobility in 4H-SiC has prevented the fabrication of the low-resistance MOSFETs for many

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years. Besides, electron mobility in the channel has been proved to be low when measured on p-implanted regions due to the implantation damage. SiC has a higher density of dangling Si and C bonds at the SiC/SiO_2 interface due to its higher surface density of atoms per unit area compared with Si. Therefore, various intrinsic defects not related to dopants or impurities can be observed at the SiC/SiO_2 interface, these defects appeared in the energy gap of SiC as traps for electrons leading to the low channel mobility in 4H-SiC. This made the reduction of interface state density at the SiO_2/SiC boundary play a critical role in increasing channel mobility and improving high temperature performance, as well as the reliability of power SiC MOSFETs or IGBTs. In the past few decades, a lot of efforts have been devoted to developing SiC power devices, and great progress has been achieved. With the advanced process technology, there are two approaches that are effective in improving the quality of the metal-oxide-semiconductor interface. One is using nitrogen during post-oxidation annealing and the other is selecting specific crystal faces for the formation of the MOS channel. Now, the SiC MOSFETs with peak mobility of 140 $cm^2/V \cdot s$ and 216 $cm^2/V \cdot s$ in the channel have been fabricated. However, interface state densities are still two orders of magnitude higher than those devices achieved by using Si MOS technology, which has been adopted by Cree to fabricate high-current (2 A), large-area (2 mm^2) lateral MOSFETs. The University of Tokyo has reported a lateral DMOSFET (LDMOSFET) with its blocking voltage and specific on-resistance of 1.5 kV and 54 $m\Omega \cdot cm^2$, respectively [20]. A breakdown voltage of 3,520 V was achieved for the 4H-SiC lateral MOSFETs with specific on-resistance of 600 $m\Omega \cdot cm^2$ [21]. This is the best result for SiC LDMOSFET.

Since 2012, Takuji Hosoi reported an AlON high-k gate dielectric technology implemented into both planar and trench SiC MOSFETs. The high-k gate dielectric technology can efficiently reduce the gate leakage and its higher dielectric breakdown field would be beneficial in improving the devices' reliability and channel carrier mobility. In 2013, a 1,600 V/150 A 4H-SiC DMOSFETs are presented by Lin Cheng. The SiC DMOSFET with smaller chip size shows superior static and dynamic performance over the commercially available 1,200 V/200 A trench gate Si IGBT from 25°C up to 200°C. In 2014, Ryota Nakamura presented a 1,200 V 4H-SiC MOSFETs with double-trench structure SiC MOSFETs. The trench structure can reduce the on-resistance by about 50% from 25℃ to 150℃.

3.2. Silicon carbide MESFETs

For the SiC power metal semiconductor field effect transistors (MESFETs), the breakdown voltage is a very important parameter that allows the power devices to achieve a specific power density and power conversion. Figure 6 is the schematic diagram of the conventional SiC MESFET. Prior research has proposed many techniques to improve the breakdown voltage [22, 23]. In order to optimize the surface electric field and improve the breakdown voltage, new technologies had been proposed, which includes the REBULF (reduced bulk field) [24] and complete 3D Reduced SURface Field (RESURF) [25]. The high breakdown had been obtained on the ultra-thin epitaxial layer with the REBULF technology. It can be ensured that these new technologies can be transplanted directly onto SiC power MESFETs. Thus, several new SiC power MESFETs had been designed to optimize the characteristic of the breakdown voltage, specific on-resistance, frequency, and transconductance.

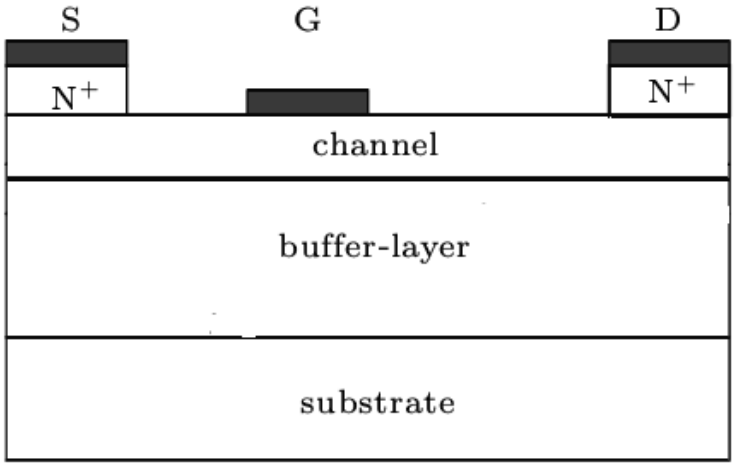

Figure 6. Schematic diagram of the conventional SiC MESFET structure.

Figure 7 is the schematic diagram of the structure of the Buffer-Gate SiC MESFETs structure [26]. Compared with the conventional 4H-SiC MESFETs (Figure 6), a low-doped, gate-buffer layer is introduced between the gate and channel layer. In Buffer-Gate 4H-SiC MESFETs, the gate length is 0.7 μm. Meanwhile, the thickness and doping concentration for the channel layer are 0.26 μm and 1.7×10^{17} cm^{-3}; between the gate and channel is the gate-buffer layer that has a thickness of 0.15 μm and doping concentration of 1×10^{15} cm^{-3}.

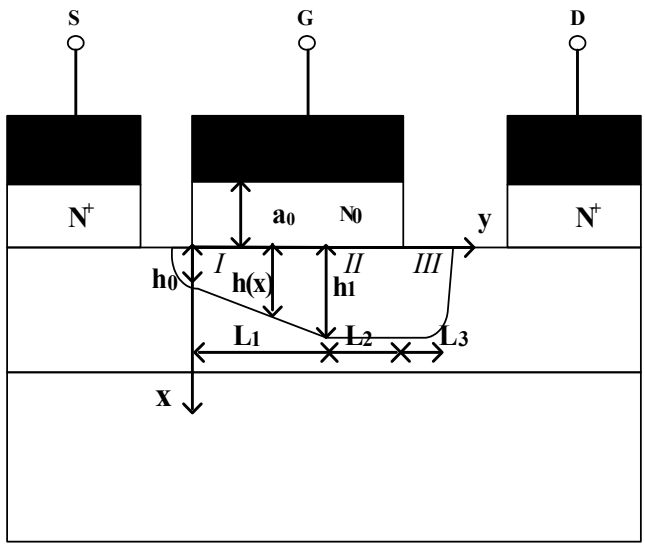

Figure 7. Schematic diagram of the structure of the Buffer-Gate SiC MESFET in saturation mode operation.

The channel current in the channel for the structure above can be expressed by (1):

$$I_C = qWn(\mathrm{x})\mu(\mathrm{E})\mathrm{E}(\mathrm{x})\left[a - h(\mathrm{x})\right] \tag{1}$$

Where q is the magnitude of the electronic charge, W is the channel width, a is the channel layer thickness, $E(x)$ is the lateral electric field strength, and $n(x)$ is the electron concentration of the channel. $h(x)$ is the thickness of the depletion layer in the channel layer and obtained by solving the 1-D Poisson's equation (2):

$$h(\mathrm{x}) = a_0\left(1 - \frac{N_0}{N_D} + \frac{V(\mathrm{x}) + V_G + V_{bi}}{\frac{qN_D}{2\varepsilon}a_0^2}\right) - a_0 \tag{2}$$

Where N_0 is the uniform doping concentration of the gate-buffer layer, which is smaller than N_D, a_0 is the gate-buffer layer thickness, and ε is the dielectric constant. $V(x)$ is the potential at the point x away from the source, V_G is the gate bias and V_{bi} the build-in voltage. To solve the 2-D Poisson's equation:

$$u_1(\mathrm{V_G}, \mathrm{V_D}) = \frac{h_1}{a} = \sqrt{\left(1 - \frac{N_0}{N_D}\right)\frac{a_0^2}{a^2} + \frac{V(\mathrm{L_1}) + V_G + V_{\mathrm{bi}}}{V_p}} - \frac{a_0}{a} \tag{3}$$

$$V(\mathrm{L}+\mathrm{L_3})\text{-}\mathrm{V}(\mathrm{L_1}) = \left(\frac{2(au_1 + a_0)}{\pi} + \frac{\mathrm{L_3}}{3}\right)\mathrm{E_s}\sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\exp\left(\frac{-\pi \mathrm{L_3}}{2(au_1 + a_0)}\right) + \\ + \frac{\mathrm{E_s}}{3}\left(2\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) + 1\right) \tag{4}$$

$$\mathrm{L_3}^2\left[\frac{qN_D a u_1}{\varepsilon} - E_s\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) + \frac{E_s}{\eta}\sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\left(1 + \tan\left(\frac{\pi a_0}{2(au_1 + a_0)}\right)\right)\right] \\ = (au_1)^2 E_s\left[\exp\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right) - 1 - \sinh\left(\frac{\pi \mathrm{L_2}}{2(au_1 + a_0)}\right)\exp\left(\frac{-\pi \mathrm{L_3}}{2(au_1 + a_0)}\right)\right. \tag{5}$$

$$\eta = \tan\left(\frac{\pi a_0}{2(au_1 + a_0)}\right)\cos\left(\frac{\pi a u_1}{2(au_1 + a_0)}\right) + \sin\left(\frac{\pi a u_1}{2(au_1 + a_0)}\right) \tag{6}$$

$$V\left(L+L_3\right)=V_D-I_C R_D \tag{7}$$

From equations (1-7), the drain current can be achieved when the structure parameters (L, W, a, a_0, N_D, N_0) and bias voltage (V_G,V_D) are given.

ISE TCAD is used in the simulation. To obtain accurate results, several basic physical models such as band gap and electron affinity models, generation-recombination models, quantization models, and incomplete ionization models are utilized, which precisely describe the material properties. Figure 8 (a) shows the effect of the gate-buffer layer on the current in the channel. It reveals that the drain current increased as the gate-buffer layer gets thicker at first, but if the thickness of the gate-buffer layer gets thicker than 0.3 μm, this correlation doesn't exist, the drain current is saturated. And the heavier the doping concentration is the bigger the drain-saturated current is. This is because the decrease of the depletion layer thickness in the channel decreased with the increase of the doping concentration and thickness of the gate-buffer layer dcrease so the channel width would increase, which makes the drain current get bigger. Figure 8 (b) shows the breakdown characteristics for the two structures. It can be seen that the breakdown voltage (V_b) of the Buffer-Gate SiC MESFETs is significantly increased, compared with that of the conventional structure (a_0=0μm, shown in Figure 5). This is because the breakdown happens at the gate corner near to the drain side due to the electric field crowding here for both structures. Different from the conventional 4H-SiC MESFETs, Buffer-Gate SiC MESFETs have an inserted lower-doped gate-buffer layer that makes the surface electric field more uniform, so the electric field peak at the gate corner is also lowered. Figure 8 (c) shows the electric field distribution. The mechanism for the suppression of the electric field at the gate corner in the Buffer-Gate SiC MESFETs is similar to the lightly-doped drain (LDD) in the MOSFETs [27].

The schematic diagram of the GDSE (Gate-Drain Surface Epitaxial layer) MESFETs is shown in Figure 9 [28]. Compared with the conventional 4H-SiC MESFETs, a low-doped p-type surface epitaxial layer is introduced between the gate and drain, which has a doping concentration two orders lower than that of the channel layer. As the layer has been introduced, firstly, the electric field peak at the gate corner will be reduced by the build-in potential in the p-n junction between the p-type epitaxial layer and n-type channel layer or n^+ cap layer, which makes the electric field distribution more uniform. Secondly, due to the much lower doping concentration of the p-type epitaxial layer, most of the depletion region in the p-n junction lies in the p-type region. Therefore, the gate-drain p-type epitaxial layer has little bad effect on the current density.

As mentioned above, the two-dimensional simulator ISE TCAD is used, to precisely describe the surface trap effect along the SiC/SiO_2 interfaces. The density and capture cross section of the near interface trap(NIT) are set to 5.3×10^{12} cm^{-2} and 1×10^{-19} cm^2, while the density and capture cross section of the deep interface trap(DIT) are set to 1.2×10^{13} cm^{-2} and 1.4×10^{-15} cm^2 [29, 30]. Schottky barrier tunneling (SBT) and initial trap populating (ITP) are taken into account for transient investigation. Similar studies concerning these mechanisms can be found elsewhere and the accuracy of relevant models has been verified [31].

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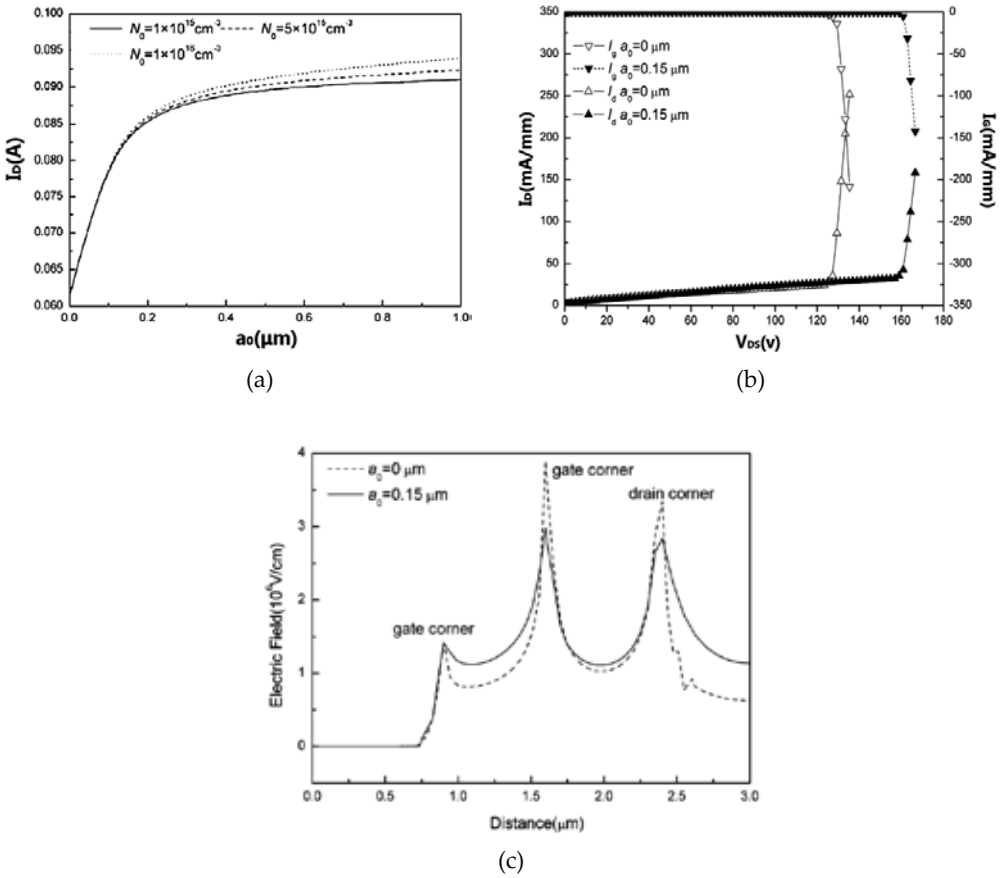


Figure 8. (a) Dependence of the drain current on the gate-buffer layer for N_0=1×10^{15} cm^{-3} N_0=5×10^{15} cm^{-3} and N_0=1×10^{16} cm^{-3}.V_{GS}=0 V, V_{DS}=5 V. (b) The simulated breakdown characteristics for a_0=0 μm (open) and a_0=0.15 μm (filled). (c) The distribution of the surface electric field for a_0=0 μm (dash) and a_0=0.15 μm (solid).

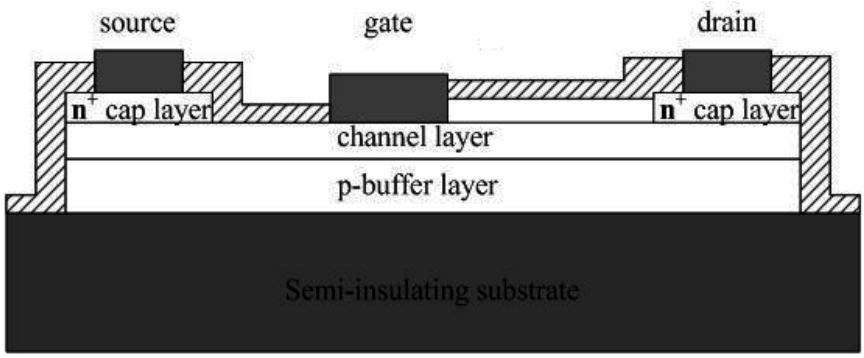
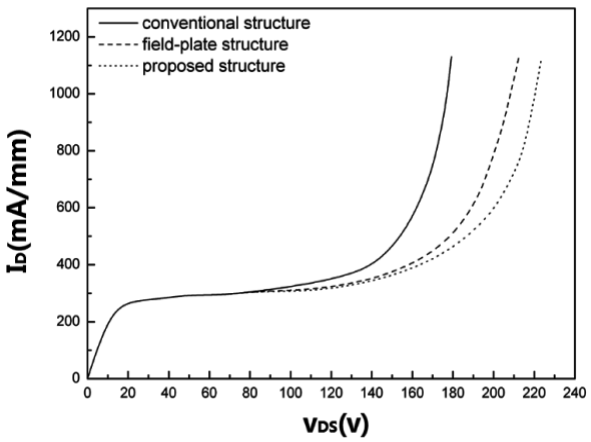
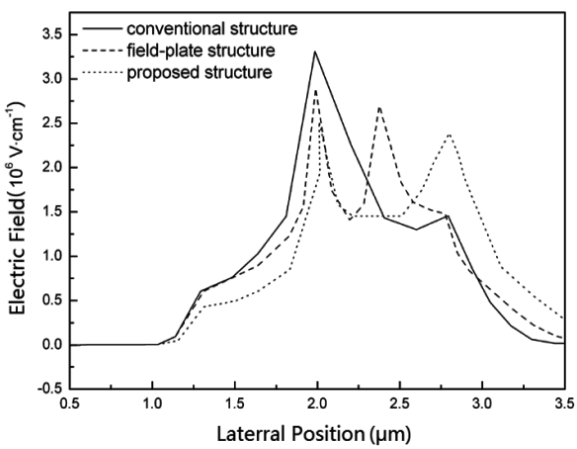


Figure 9. The schematic diagram of MESFETs with gate-drain surface epi-layer [28].

The introduced p-type spacer layer has a thickness of 0.1 μm and a doping concentration of 3×10^{15} cm^{-3}, the thickness and doping concentration of the n-type channel used as the conductive channel for device operation is 0.22 μm and 3×10^{17} cm^{-3}. And the buffer layer is 0.6 μm thick with a doping concentration of 5×10^{15} cm^{-3}. The breakdown characteristics and surface electric field distribution are shown in Figure 10. It had been shown that the breakdown voltage of the GDSE structure is the largest one for the three structures in Figure 10 (a) owing to the inserted lower-doped p-type epitaxial layer the electric field peak at the gate corner is significantly lowered (i.e., the surface electric field is more uniform), so the breakdown voltage for the GDSE MESFETs increased as is shown in Figure 10 (b).



(a)



(b)

Figure 10. Comparison of the (a) breakdown voltage and the (b) surface electric field for the conventional, field-plated, and the GDSE structure.

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The schematic diagram of the L-gate 4H-SiC MESFETs with partial p-type spacer is shown in Figure 11. Compared with the conventional 4H-SiC MESFETs, the L-gate and partial p-type spacer are introduced. The L-gate structure has lower and upper gates that effectively controls a thinner and a thicker part of the channel, respectively. It can decrease the gate capacitance and reduce the depletion layer under the gate, which makes the conduct channel under the L-gate wider, so the saturation drain current increases effectively. Since the p-n junction formed between the p-spacer and the n-channel also leads a distinct reduction of the gate-drain capacitance, the proposed structure has a significant improvement of the DC and RF performances compared with conventional SiC MESFETs.

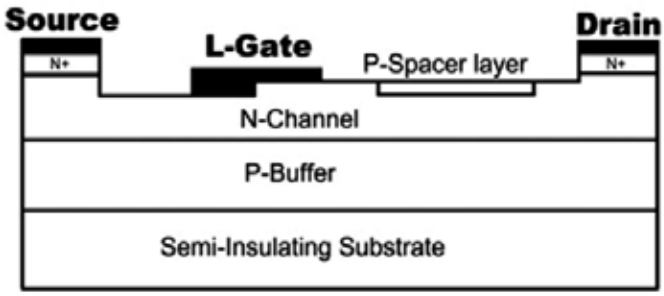

Figure 11. The schematic diagram of the L-gate 4H-SiC MESFETs with partial p-type spacer.

Figure 12 (a) shows the simulated output characteristics of C-MESFET, L-gate-MESFET, and LP-MESFET under the gate bias (V_{GS}) vary from 0 V to -12 V with a step of 4 V. It can be seen that due to the thicker gate-drain drift region and wider channel region outside the L-gate, the LP-MESFET has a higher saturation drain current (I_{Dsat}) than that of conventional ones at V_{GS}=0 V. It also should be noted that the p-n junction formed between the p-spacer and n-channel that leads to a reduction in effective thickness of the gate-drain drift region slightly decreases the saturated drain current of the LP-MESFET comparing with that of the L-gate-MESFET.

Figure 12 (b) shows the three-terminal breakdown characteristics for 4H-SiC C-MESFET, L-gate-MESFET, and LP-MESFET simulated with an applied V_{GS}=V_T. The drain current (I_D) and the gate leakage current (I_G) with respect to V_{DS} are displayed for the three MESFETs. It can be seen that the drain current will increase with the gate leakage current increasing, this illustrates that the breakdown of 4H-SiC MESFETs at the applied V_{GS} occurs at the gate-drain drift region, which is because the electric field for all the structures crowding at the gate corner near the drain. Therefore, owing to the extension of gate metal on the surface acted as a field plate resulting in a gradual field distribution, the high electric field peak at the bottom edge of gate toward the drain side is suppressed, the MESFETs with a L-Gate has an improvement of the breakdown voltages shown in Figure 11 (a) [32]. It can be seen that the breakdown voltages are 250 V for the C-MESFET, 360 V for the L-gate-MESFET, and 340 V for the proposed structure LP-MESFET, which is 36% higher than that of C-MESFET. The maximum output power density Pmax for the 4H-SiCC-MESFET, L-gate-MESFET, and LP-MESFET at V_{GS}=4 V and V_{DS}=40 V is

4.2 W/mm, 9.1 W/mm, and 8.2W/mm, respectively. Output power density of the LP-MESFET structure is about 95% larger than that of the C-MESFET structure. [33].

Figure 12 (c) shows the simulated C_{GD} versus frequency at V_{DS}=40 V and V_{GS}=-5 V. It can be seen that the C_{GD} of the LP-MESFET structure is smaller than that of the C-MESFET structure and the L-gate-MESFET structure. As is known to all, the C_{GD} consists of depletion layer capacitance and drift region diffuse capacitance. From the device structure, we can see that the partial p-type spacer has a distance from the gate edge towards the drain, so the decrease of C_{GD} is not derived from the reducing depletion layer extension to drain. That means the reducing C_{GD} is mainly attributed to the decreased gate-drain drift region diffused capacitance brought by the partial p-type spacer.

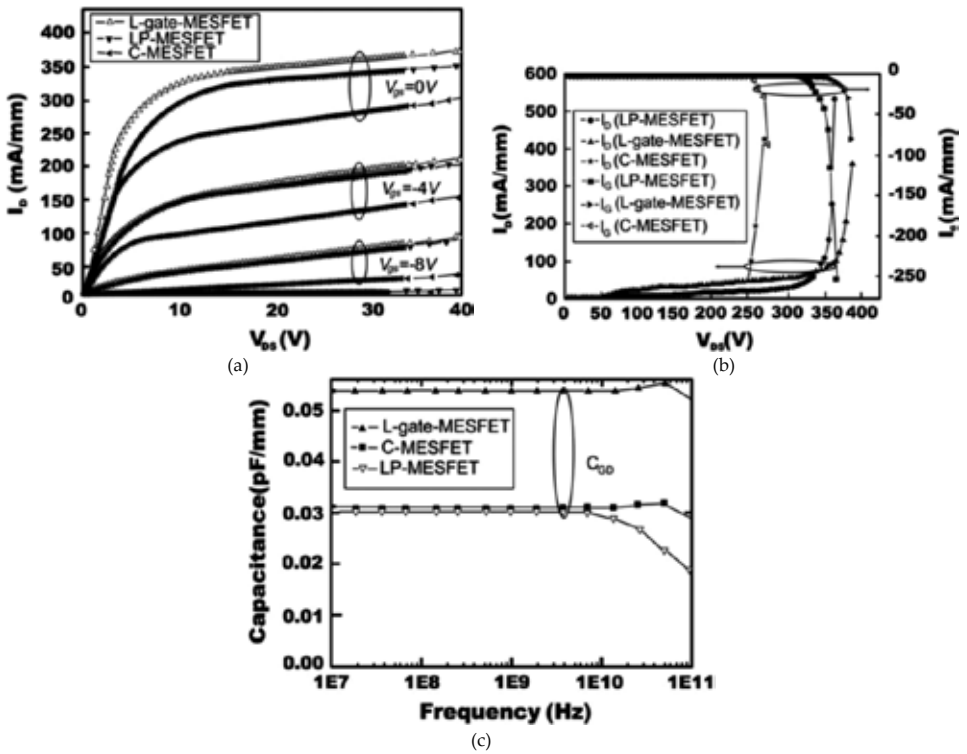

Figure 12. (a) The simulated I_D-V_{DS} characteristics of different structures. (b) Simulated three-terminal breakdown characteristics for 4H-SiC C-MESFET, L-gate-MESFET. and LP-MESFET. (c) Dependences of the simulated drain-gate capacitance (C_{GD}) on the frequency of the three structures under DC bias conditions of V_{DS}=40 V and V_{GS}=-5 V.

4. Silicon carbide bipolar devices

There has been great progress in SiC bipolar power devices such as BJT and IGBT. SiC BJT exhibits 20~50 times lower than Si BJT in switching losses and ON-state voltage. In Si BJT, the

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second breakdown is widespread, which significantly affects the devices' performance. However, it is negligible in SiC BJT since the critical current density is 100 times lower than that of Si BJT. Moreover, the base region and collector region are allowed to be fabricated very thin so as to improve the current gain and switching speed due to the large critical electric field of SiC material. The Cree company has reported another 4H-SiC BJT with its current gain of 44, blocking voltage of 3.2 kV, and specific on-resistance of 8.1 $m\Omega \cdot cm^2$ [34]. The driving circuit of SiC BJT is complex compared with that of a MOSFET. However, its manufacturing process is simpler than that of a JFET. In the area of SiC IGBT, Q. Zhang has reported a UMOSFET 4H-SiC IGBT with a blocking voltage and specific on-resistance of 10 kV and 175 $m\Omega \cdot cm^2$ at 25°C [35]. In 2007, Purdue University fabricated a p-IGBT with a p-region width of 175 μm, as high as 20 kV in blocking voltage [36]. This IGBT can provide approximately twice the ON-state current as MOSFETs at 177°C, which is superior to the IGBT based on the Si. In the same year, Cree reported a SiC n-IGBT with a blocking voltage of 12 kV, and its switching characteristic is shown in Figure 13 in comparison with that of Si-IGBT [37].

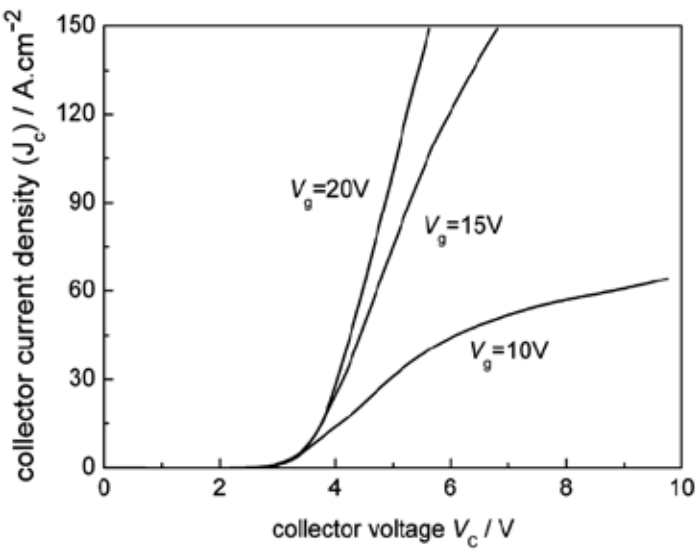

Figure 13. 12kV 4H-SiC N-IGBT ON-state characteristics [35].

Since key technologies, such as low mobility in the inverse channel layer and reliability of the gate oxide layer with the high electric field, have not been overcome, SiC MESFETs (or JFETs) and BJTs may be the only widespread SiC devices commercially. At present, process technologies, such as injection, oxidation, and etching processes, should be improved in order to optimize device structures. In the long run, researchers should focus their attentions on the process theory and technology of gate oxidation for fabricating superior MOSFETs and IGBTs.

5. Forthcoming challenges for silicon carbide power devices

5.1. Defects for silicon carbide materials

Reducing and eliminating the defects density in the SiC wafer is a knotty task, which is the main reason that is limiting the wafer dimension. There has been significant development in reducing and eliminating defects density. Cree has been supplying 4-inch SiC wafers with zero micro-pipe since 2007. Now, the research of defects is focusing on the effects of dislocation, such as screw dislocation, basal plane dislocations, edge dislocation, and other defects on the characteristics of the devices.

5.2. Challenges for silicon carbide power devices

This technical review is one of the series of reports on semiconductor power devices. Three IETE articles have been reported on the application of electric field modulation to silicon and silicon-on-insulator power devices [36,37]. There are two bottleneck techniques in SiC MOSFETs that need to be broken down, the low electron mobility in the inversion channel layer and gate oxide reliability with high temperature or high electric field. The recent reported electron mobility is 30-250 $cm^2/V \cdot s$, which does not manifest the advantage of the SiC MOSFET. Therefore, special gate oxidation technologies are needed to eliminate the SiC/SiO_2 interface defects and increase the mobility of the electron in the inversion layer, such as the post-oxidation annealing in the H_2 environment, and gate oxidation or annealing in NO or N_2O environment. It is unknown what causes the current gain instability; one possible reason may be the stacking fault in the epitaxial base region. The new SiC power devices can be designed by applying the electric field modulation effect. Electric field modulation had been proposed by the authors for the first time [38-40]. Several new structures for the silicon power devices and AlGaN/GaN HEMTs had been reported, which can be used to design new SiC power devices [41-47].

The packaging of the SiC power device is also a pressing problem. The packaging reliability for SiC devices will be a key factor affecting the performance of the circuits once the material and process challenges are overcome. Packaging reliability is also important when the devices operate at high temperatures (≥ 200°C) or the coolant temperature require the operation temperature should above today's limits of ~150°C. For example, the automotive motor drives using engine coolant, oil and gas drilling and extraction, avionics power supplies, space power supplies, and military applications. It's important to increase the power handling capability to reduce the expensive chip area and cooling cost. Thus, new package materials for high temperature application are necessary.

As the great reduction of switching energy is attained by very fast switching and when SiC power devices are applied in the fast switching area, the internal electromagnetic parasitic issues between the device and package should be taken into account. The advanced power module architectures are very important.

During the application of SiC power devices, people should think about the high electric field issue. Due to the high device internal electric field, the field stress in the passivation layer and

at the chip surfaces is so high that the average electric field for the chip/gel interface at the terminal edge is around 3 times higher than the SiC diode. With such high surface field strengths, any contamination in the form of particles or mobile ions may lead to possible electrochemical driven corrosion processes; any material defect in the passivation layers and any delamination/insufficient adhesion of encapsulation may become extremely critical. This makes the advanced insulation technology of great importance.

6. Conclusion

In conclusion, SBD has an extremely fast turn-on performance due to the absence of reverse recovery charge, which is well suited for high-speed switching applications, drastically reducing the dynamic losses of typical circuits, and yet minimizing the size of cooling systems. The SiC PiN diodes have the characteristics of low gate leakage current and high breakdown voltage, and thus can be used as switches in high voltage and low frequency circumstances. The JBS shows the ON-state and switching characteristics similar to Schottky diodes and blocking characteristics similar to PiN diodes. MESFETs have superior RF performance compared to JFETs due to the reduced gate capacitance and higher transconductance. SiC BJT exhibits much lower switching losses and ON-state voltage than Si BJT. Unless the electron mobility in the inverse channel layer and reliability of the gate oxidation layer are broken through, SiC MOSFETs will not be commercially widespread.

Author details

Yintang Yang, Baoxing Duan*, Song Yuan and Hujun Jia

*Address all correspondence to: bxduan@163.com

Key Laboratory of the Ministry of Education for Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an, China

References

[1] T. Hiyoshi, T. Kimoto. "Elimination of the major deep levels in n- and p-Type 4H-SiC by two-step thermal treatment," Appl. Phys. Exp., vol. 2, pp. 091101, Sep 2009.

[2] W. Lee, K. Chu, C. Huang, L. Lee, M. Tsai, K. Lee, and F. Zhao. "Design and fabrication of 4H-SiC lateral high-voltage devices on a semi-insulating substrate," IEEE Trans. Electron Devices, vol. 59, pp. 754-760, Mar 2012.

[3] W. C. Kuan, W. S. Lee, C. Y. Cheng, C. F. Huang, F. Zhao, L. S. Lee, Y. S. Chen, C. Y. Lee, and M. J. Tsai. "Demonstration of Lateral IGBTs in 4H-SiC," IEEE Electron Device Letters, vol. 34, pp. 286-288, Feb 2013.

[4] S. Y. Han, K. H. Kim, J. K. Kim, H. W. Jang, K.H. Lee, N. K. Kim," Ohmic contact of formation mechanism of Ni on n-type 4H-SiC" Appl. Phys. Lett., vol. 79, pp. 1816-1818, June 2001.

[5] R. Kakbaakov, L. K. Kolaklieva, N. Hristeva, G. LePoeva, K. Zekentes. "Thermally stbale low resistivity ohmic contacts for high power and high temperature SiC device applications," in 23rd Int Conf Microelectron, Nis, Yugoslavia pp. 205-208, May 2002.

[6] S. Yoshida, K. Sasaki, E. Sakuma. "Schottky barrier diodes on 3C-SiC," Appl. Phys. Lett., vol. 46, pp. 766-768, Aug 1985.

[7] G. H. Glover. "Charge multiplication in Au-SiC(6H) Schottky junction," Appl. Phys., vol. 46, pp. 4842-4844, Oct 1975.

[8] C. E. Weitzel, J. W. Palmour, C. H. Carter Jr., et al. "Silicon carbide high-power devices," IEEE Trans. Electron Devices, vol. 43, pp. 1732-1741, Oct 1996.

[9] A. S. S. Kumta, E. Rusli, and J. H. Xia. "Field-plate-terminated 4H-SiC Schottky diodes using Al-based high-k dielectrics," IEEE Trans. Electron Devices, vol. 56, pp. 2925-2934, Dec 2009.

[10] J. Nishio, C. Ota, T. Hatakeyama, T. Shinohe, K. Kojima, S. Nishizawa, and H. Ohashi. "Ultralow-loss SiC floating junction Schottky barrier diodes (super-SBDs)," IEEE Trans. Electron Devices, vol. 55, pp. 1954-1960, Aug 2008.

[11] S. Dimitrijev, P. Jamet. "Advances in SiC Power Technology," Microelectronics Reliability, vol. 43, pp. 225-233, Aug 2007.

[12] J. P. Bergman, H. Lendznmann, P. A. Nilsson, U. Lindefelt, and P. Skytt. "Crystal Defects as Source of Anomalous Forward voltage Increase of 4H-SiC Diodes," Materials Science Forum, vol. 435-456, pp. 299-302, Sept 2001.

[13] S. G. Muller, M. F. Brady, W. H. Brixius, G. Fechko, R. C. Glass, D. Henshall, and C. H. Carter. "High quality SiC substrate for semiconductor devices: From research to industrial production," Materials Science Forum, vol. 389-393, pp. 23-28, Oct 2002.

[14] H. Niwa, G. Feng, J. Suda, and T. Kimoto. "Breakdown characteristics of 15-kV-class 4H-SiC PiN diodes with various junction termination structures," IEEE Trans. Electron Devices, vol. 59, pp. 2748-2752, Oct 2012.

[15] F. Zhao, M. M. Islam, P. Muzykov, A. Bolotnikov, and T. S. Sudarshan. "Optically activated 4H-SiC p-i-n diodes for high-power applications," IEEE Electron Device Letters, vol. 30, pp.1182-1184, Nov 2009.

[16] L. Zhu and T. P. Chow. "Advanced High-Voltage 4H-SiC Schottky Rectifiers," IEEE Trans. Electron Devices, vol. 55, pp. 1871-1874, Aug 2008.

[17] [17]J. W. Palmour, J. A. Edmond, H. Kong, and C. Charter, “Vertical power devices in silicon carbide,” in Proc. Silicon Carbide Rel. Mater., Inst. Phys. Conf., Oct. 1994, pp. 499-502.

[18] [18]J. N. Shenoy, J. A. Cooper, and M. R. Melloch, “High-voltage double implanted power MOSFET’s in 6H-SiC,” IEEE Electron Device Lett., vol. 18, no. 3, pp. 93-95, Mar. 1997.

[19] [19]S. H. Ryu et al., “10-kV, 123-mΩcm^2 4H-SiC power DMOSFETs,” IEEE Electron Device Lett., vol. 25, no. 8, pp. 556-558, Aug. 2004.

[20] I. M. Nobor, J. Suda, and T. Kimoto. "4H-SiC double RESURF MOSFETs with a record performance by increasing resurf dose," in International Power Semiconductor Devices and ICs. Digest, Florida, pp.263-266, May 2008.

[21] W. S. Lee, C. W. Lin, M. H. Yang, C. F. Huang, J. Gong, and Z. Feng. "Demonstration of 3500-V 4H-SiC Lateral MOSFETs," IEEE Electron Device Letters, vol. 32, pp. 360-362, May 2011.

[22] X. B. Chen and K. O. S. Johnny. "Optimization of the Specific On-Resistance of the COOLMOS^{TM}," IEEE Trans. Electron Devices, vol. 48, pp. 344-348, Jan 2001.

[23] G. Sameh, K. Nassif, and C. A. T. Salama. "Super-junction LDMOST on a silicon-on-sapphire substrate," IEEE Trans. Electron Devices, vol. 50, pp. 1385-1391, Aug 2003.

[24] B. X. Duan and Y. T. Yang. "REBULF Super Junction MOSFET with N+ buried layer," Micro & Nano Letter, vol. 6, pp. 881-883, Nov 2011.

[25] B. X. Duan and Y. T. Yang. "Low specific on-resistance power MOS transistor with multi-layer carrier accumulation breaks the limit line of silicon," IEEE Trans. Electron Devices, vol. 58, pp. 2057-2060, Jul 2011.

[26] X. J. Zhang, Y. T. Yang, B. X. Duan, B. Chen, C. C Chai, and K. Song. "New 4H silicon carbide metal semiconductor field effect transistor with the buffer layer between the gate and channel,” Chinese Physics B, vol. 21, pp. 017201, Jan 2012.

[27] K. Song, C. C Chai, Y. T. Yang, B. Chen, X. J. Zhang, and Z. Y. Ma. "Effects of gate-buffer combined with a p-type spacer structure on silicon carbide metal semiconductor field-effect transistors," Chinese Physics B, vol. 21, pp. 17202, Jan 2012.

[28] K. Song, C. C. Chai, Y. T. Yang, X. J. Zhang, and B. Chen. "Improvement in breakdown characteristics of 4H-SiC MESFET with a gate-drain surface epi-layer and optimization of the structure," Acta. Phys. Sin., vol. 61, pp. 27201-27206, Jan 2012.

[29] H. O. Olafsson, F. Allerstam, and E. O. Sveinbjornsson. "On shallow interface states in n type 4H-SiC metal-oxide-semiconductor structures," Materials Science Forum, vol. 444, pp. 1005, March 2002.

[30] F. Allerstam and E. O. Sveinbjornsson, "A study of deep energy-level traps at the 4H-SiC/SiO_2 interface and their passivation by hydrogen," Materials Science Forum, vol. 600, pp. 755-758, Feb 2009.

[31] H. Hjelmgren, F. Allerstam, K. Andersson. "Transient simulation of microwave SiC MESFETs with improved trap models," IEEE Trans. Electron Devices, vol. 57, pp. 729-732, March 2010.

[32] H. Y. Cha, Y. C. Choi, L. F. Eastman, and M. G. Spencer. International Journal of High Speed Electronics and Systems 14 (2004) 884-889.

[33] B. X. Duan, B. Zhang, Z. J. Li. Solid State Electronics 49 (2005) 1965-1968.

[34] S. Krishnaswami, A. Agarwal, J. Richmond, C. Capell, S. H. Ryu, J. Palmour, B. Geil, D. Katsis, C. Scozzie. "High temperature characterization of 4H-SiC bipolar junction transistors," Materials Science Forum, vol. 527-529, pp. 437-440, Nov 2005.

[35] Q. Zhang, H. R. Chang, M. Gomez, C. Bui, E. Hanna, J. A. Higgins, T. Isaacssmith, J. R. Williams. "10 kV Trench Gate IGBTs on 4H-SiC," in International Symposium on Power Semiconductor Devices and ICs. Digest, Santa Barbara, pp. 303-306, May 2005.

[36] Y. Sui, X. Wang, J. A. Cooper. "High-Voltage Self-Aligned p-Channel DMOS-IGBTs in 4H-SiC," IEEE Electron Device Letters, vol. 28, pp. 728-730, Aug 2007.

[37] J. Palmour. "Advances in SiC Power Technology." in DARPA MTO Symposium, San Jose, CA., pp.78-80, March 2007.

[38] B. X. Duan, Y. T. Yang, and B. Zhang. "A development summarization of the power semiconductor devices," IETE Technical Review, vol. 28, pp. 503-510, Nov-Dec 2011.

[39] B. X. Duan, Y. T. Yang, and B. Zhang. "The application of the electric field modulation and charge shielding effects to the high voltage Si LDMOS," IETE Technical Review, vol. 29, pp. 276-281, Jul-Aug 2012.

[40] B. X. Duan and Y. T. Yang. "Power VDMOS transistor with the step oxide trench breaks the limit line of silicon," Micro & Nano Letter, vol. 6, pp. 777-780, Sep 2011.

[41] B. X. Duan, Y. T. Yang, and B. Zhang. "High Voltage REBULF LDMOS with N+-Buried Layer," Solid-State Electronics, vol. 54, pp. 685-688, Jul 2010.

[42] B. X. Duan, B. Zhang, and Z. J. Li. "A New Partial SOI Power Device Structure with P-type Buried Layer," Solid-State Electronics, vol 49, pp. 1965-1968, Dec 2005.

[43] B. X. Duan, Y. T. Yang, and B. Zhang, and X. F. Hong. "Folded Accumulation LDMOST (FALDMOST): New Power MOS Transistor with Very Low Specific On-resistance," IEEE Electron Device Letters, vol. 30, pp. 1329-1331, Dec 2009.

[44] B. X. Duan, Y. T. Yang, and B. Zhang. "New Super Junction LDMOS with N-Type Charges Compensation Layer," IEEE Electron Device Letters, vol. 30, pp. 305-307, March 2009.

[45] B. X. Duan, B. Zhang, and Z. J. Li. "New Thin-Film Power MOSFET'S with a Buried Oxide Double Step Structure," IEEE Electron Device Letters, vol. 27, pp. 377-379, May 2006.

[46] B. X. Duan and Y. T. Yang. "Breakdown voltage analysis for the new RESURF AlGaN/GaN HEMTs," Sci China Inf Sci, vol. 55, pp. 473-479, Feb 2012.

[47] B. X. Duan and Y. T. Yang. "Breakdown voltage analysis of $Al_{0.25}Ga_{0.75}N$/GaN high electron mobility transistors with the partial silicon doping in AlGaN layer," Chinese Physics B, vol. 21, pp. 057201-057208, May 2012.

Section 3

Novel SiC Devices

Chapter 7

High-responsivity SiC Ultraviolet Photodetectors with SiO_2 and Al_2O_3 Films

Feng Zhang

Additional information is available at the end of the chapter

http://dx.doi.org/10.5772/61019

Abstract

Silicon carbide (SiC) has shown considerable potential for ultraviolet (UV) photodetectors due to its properties such as wide band gap (3.26 eV for 4H-SiC), high break down electric field and high thermal stability. 4H-SiC-based UV photodetectors such as Schottky, metal-semiconductor-metal (MSM), metal-insulator-semiconductor (MIS) and avalanche have been presenting excellent performance for UV detection application in flame detection, ozone-hole sensing, short-range communication, etc. Generally, the most widely used antireflection coating and passivation layer for 4H-SiC-based photodetectors are native SiO_2 grown by heating 4H-SiC in O_2 in order to improve the absorption and passivation of photodetectors. Nevertheless, the thermally grown SiO_2 single layer suffers from high reflection, large absorption and inaccurate thickness. Therefore, in this chapter, UV antireflection coatings were designed, fabricated and applied in order to reduce optical losses and improve the quantum efficiency (QE) of 4H-SiC-based photodetectors. The important results will be introduced as follows:

According to transparent range, extinction coefficient, refractive index, mechanical properties and chemical reliability, Al_2O_3 and SiO_2 films were selected in tens of optical film materials as antireflection coatings on 4H-SiC-based UV photodetectors. SiO_2 film was designed between Al_2O_3 film and 4H-SiC substrate and Al_2O_3 film was deposited on SiO_2 film according to its reliability. The optical thicknesses of Al_2O_3 and SiO_2 film were designed according to the admittance matching technology. Al_2O_3/SiO_2 films were deposited on 4H-SiC substrates by using electron-beam evaporation according to the film's design. The minimum reflectance of the films was 0.25% at 276 nm, which is the minimum attained so far. The minimum reflectance shifted to shorter wavelengths with the increase of annealing temperature due to reduction of film thickness. The surface grains appeared to get larger in size and the root mean square (RMS)

roughness of the annealed films increased with annealing temperature but was less than that of the as-deposited. Although the Al_2O_3/SiO_2 film was kept amorphous, there were diffusion that Al silicates and Si suboxides were formed at the interface between films and 4H-SiC substrate.

4H-SiC-based MSM UV photodetectors with Al_2O_3/SiO_2 films have been fabricated and compared with SiO_2/4H-SiC MSM detectors. The photocurrent of the former was twice as large as the latter, while the dark current was also larger. The Al_2O_3/SiO_2/4H-SiC devices showed a peak responsivity of 0.12 A/W at 290 nm under 20 V, which was twice as much as that of MSM detectors. The internal and external QE of the Al_2O_3/SiO_2/4H-SiC devices were 50% and 77% at 280 nm, respectively, which are the highest attained so far for 4H-SiC-based MSM photodetectors. The responsivity of the Al_2O_3/SiO_2/4H-SiC devices agreed well with their surface reflectance of 240–300 nm.

The Al_2O_3/SiO_2 films prepared by oxidation and electron-beam evaporation were applied on 4H-SiC-based MIS photodiodes. The dark current of the devices was 1 pA, which was larger than that of SiO_2/4H-SiC detectors due to undercutting of the mesa sidewall. But the photocurrent of the former was 2.8 nA, which is 2.8 times as large as that of the latter. There were slight gains in these two devices with the increase of backward bias voltage. The peak responsivities of Al_2O_3/SiO_2/4H-SiC and SiO_2/4H-SiC devices were 49 mA/W at 270 nm and 23 mA/W at 260 nm, respectively, corresponding to external QEs of 23% and 15%. The peak responsivities of these two devices agreed well with their minimum surface reflectances.

Keywords: Photodetectors, Antireflection coatings, Refraction index, Band gap, Transparent range

1. Introduction

Silicon carbide (SiC) has been considered to be a new generation semiconductor material for optoelectronic and power devices due to its wide band gap (3.26 eV for 4H-SiC), high break down electric field (3.0 MV/cm for 4H-SiC) and high thermal stability (4.9 W/cm K for 4H-SiC). In the recent decade, SiC-based ultraviolet (UV) photodetectors have been improved and developed greatly with all sorts of structures including Schottky diodes[1-3], metal-semiconductor-metal (MSM)[4-6], p-i-n[7-9], metal-insulator-semiconductor (MIS)[10] and avalanche photodiodes (APD)[11-13] for application in flame detection, ozone-hole sensing, short-range communication, etc. Generally, the photons can be absorbed in 4H-SiC overall below 360 nm except that more than 20% of them are reflected, as shown in Figure 1(a). Meanwhile, the absorption coefficient of the 4H-SiC is larger than 1000 below a wavelength of 300 nm and the penetration length of the previously mentioned UV light in 4H-SiC is below 4 μm, as depicted in Figure 1(b). Thus, high-quality antireflection (AR) coatings and clean interface between 4H-SiC and coatings are needed for reducing optical loss on the surfaces and interfaces in these SiC-based photodetectors. The recent results showed that the internal quantum efficiency of

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SiC photodetectors had reached 100%. Thus, improvement of external quantum efficiency of SiC photodetectors is particularly important and significant, which can be approached by depositing AR coatings.

The most widely used AR coatings for SiC-based photodetectors is silicon dioxide (SiO_2), which is thermally grown by oxidizing the surface of SiC in a furnace at 1100°C–1300°C[14]. The reflection can be reduced to below 8% in the range of 220–380 nm. Although the SiO_2 layer usually has good passivation quality, its optical properties such as large absorption, uncertain refractive index, inaccurate film thickness and high reflection cannot be controlled ideally. Therefore, it is necessary to redesign and grow the AR coatings for 4H-SiC UV photodetectors.

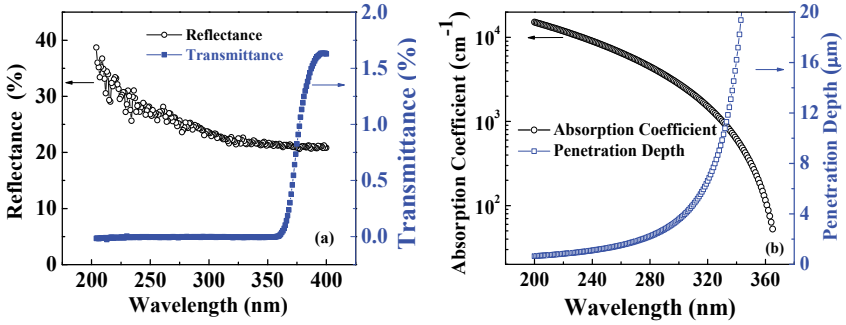

Figure 1. (a) The transmittance and reflectance spectra on a 4H-SiC surface without any coatings and (b) reflectance spectra of thermally grown SiO_2 single layer in the 200–400 nm spectral range.

2. Selection of AR coatings

There are many factors that need to be considered for the selection of UV AR coatings for 4H-SiC photodetectors including transparent range, refraction index, mechanical and chemical properties, etc. Although there are hundreds of materials that can be prepared for AR coatings, few of them are suitable for 4H-SiC in UV range.

Material	Transparent Range (μm)	Refraction Index	Knoop Hardness (×9.8 N/mm^2)
MgF_2	0.21–10	1.32–1.39	430
BaF_2	0.19–13	1.2–1.47	82
CaF_2	0.15–12	1.36–1.42	163
Al_2O_3	0.2–8	1.60–1.80	2100
SiO_2	0.16–9	1.45–1.55	780
HfO_2	0.22–12	1.95–2.15	1000

Table 1. Optical and Mechanical Properties of Several Coating Materials in UV Range

2.1. Transparent range

Transparent range is the first and most important factor for 4H-SiC UV photodetectors, which means that AR coatings need to be transparent in the UV range especially at 200–400 nm. Only several oxides and fluorides can satisfy the condition such as Al_2O_3, SiO_2, HfO_2, CaF_2, BaF_2, MgF_2, etc., as shown in Table 1. These materials have a large band gap so that the UV photons do not have adequate energy to achieve transition. Extinction coefficient is another factor that can characterize the transparent level of an optical film. The lower the extinction coefficient is, the better the transmittance of the film. The extinction coefficient is related to the crystal structure of the AR coatings. Generally, polycrystalline films have the largest extinction coefficients, amorphous films have lower extinction coefficients and single crystal lowest extinction coefficients. UV AR coatings have higher requirements on transmittance and extinction coefficients than visible AR coatings, thus only a few materials can meet the requirements, as shown in Table 1.

2.2. Refraction index

Refraction index is another important parameter for an optical material to be applied in photodetectors, which is required to match that of substrates so that AR effect can be achieved. Generally, refraction index increases with the decrease of the wavelength. The relationship between refraction index (n) and wavelength (λ) is[15]

$$n(\lambda) = A_1 + A_2 / \lambda^2 + A_3 / \lambda^4 \tag{1}$$

where A_1, A_2 and A_3 are undetermined coefficients. Refraction index is also related to the density of optical materials, in which those with a higher density usually have a higher refraction index. Take Al_2O_3 for example, the refraction index of the Al_2O_3 film prepared by physical vapor deposition (PVD) or chemical vapor deposition (CVD) is lower than that of sapphire due to its lower density.

2.3. Mechanical property and stability

SiC is a superstable material with ultrahigh hardness, which is only lower than that of diamond. Thus, its AR coatings require suited mechanical property and high stability. Generally, fluorides such as CaF_2, BaF_2 and MgF_2 are very soft materials, although their transparent ranges are adequately wide, as shown in Table 1, which are not suitable for SiC photodetectors. Oxides are probably the most suitable materials because they not only have high hardness but also high stability. It is necessary to notice that some oxides such as MgO have suitable transparent range and hardness but it is not stable and reacts with CO_2 in the air, which cannot be used for AR coatings. Oxides such as Al_2O_3 and HfO_2 have ultrahigh hardness, as shown in Table 1, which are good choices for SiC photodetectors.

2.4. Electronic property

In photodetectors, AR coatings are also used as passivation layers to restrain the leakage current. Thus, electronic properties of the AR coatings are also significant for 4H-SiC UV photodetectors. Excellent coatings have wide band gap, high dielectric constant, high critical electric field and high conduction band gap. As shown in Table 2, some materials such as HfO_2 have high dielectric constant but its critical electric field and conduction band gap are low. Meanwhile, other materials such as AlN and Si_3N_4 have ideal critical electric field and conduction band gap but narrow band gap and low dielectric constant.

Under comprehensive evaluation, though dielectric constants are not adequate high, Al_2O_3 and SiO_2 are materials that not only have wide band gap and ideal transparent range but also suitable refractive index, high critical electric field and conduction band gap, which is the most suitable optical material as AR coatings for application in SiC UV photodetectors.

Material	Band Gap (eV)	Transparent Range (μm)	Refractive Index	Dielectric Constant	Electric Field (MV/cm)	Conduction Band Offset (eV)
4H-SiC	3.26	0.40–10	2.62–3.0	9.7	3.0	0
SiO_2	9.0	0.20–9	1.45–1.55	3.9	13	2.7
Al_2O_3	8.8	0.20–8	1.60–1.80	9.0	13	2.0
AlN	6.2	0.30–7	1.65–1.93	8.5	13	1.7
HfO_2	5.7	0.32–12	1.88–2.15	25	6.7	0.7
Si_3N_4	5.3	0.32–7	1.95–2.15	7.5	10	1.6

Table 2. Optical and Electronic Parameters of 4H-SiC and Dielectrics[16, 17]

3. Design of AR coatings

Design of AR coatings is the procedure to determine the thickness and refractive index of the optical materials. Admittance matching method was used to design AR films for 4H-SiC photodetectors. The reflection will happen when the incidence of UV light is from one material to another due to the mismatch of the refraction indices. The relationship between admittance (Y) and refraction index (N) is $Y = N (\varepsilon_0/\mu_0)^{1/2}$. Thus, admittance matching is important and significant for the design of the AR coatings.

3.1. Single-layer AR coating

Single-layer AR coating is considered at first due to it is the simple system, as shown in Figure 2. The reflection coefficient of single-layer AR coating is

$$r = \frac{r_1 + r_2 \exp\left(-2i\delta_1\right)}{1 + r_1 r_2 \exp\left(-2i\delta_1\right)} \tag{2}$$

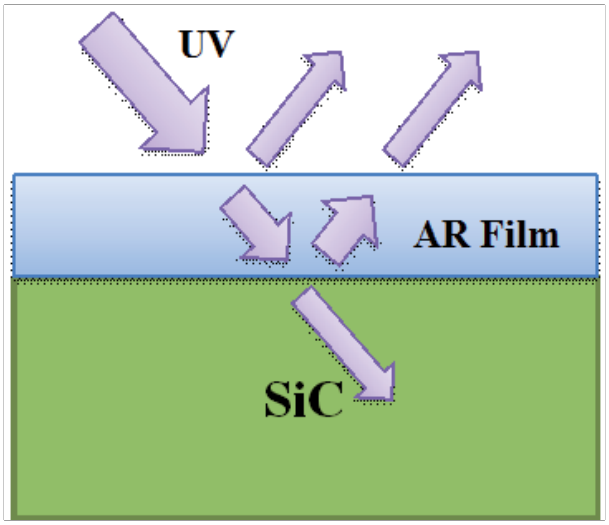

Figure 2. Incidence of UV light from a single-layer AR film to a SiC substrate (multiple reflections in AR films are ignored).

where r_1 and r_2 are reflection coefficients of surfaces of substrate and AR film, which can be presented as $r_1 = \frac{n_0 - n_1}{n_0 + n_1}$ and $r_2 = \frac{n_1 - n_2}{n_1 + n_2}$. δ_1 is the phase thickness of single-layer AR coating and can be presented as $\delta_1 = \frac{2\pi}{\lambda} n_1 d_1 \cos\theta_1$. Then the reflectance R is

$$R = |r|^2 = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos 2\delta_1}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos 2\delta_1} \tag{3}$$

Thus, when the light beam performs vertical incidence, the sufficient condition of $R = 0$ at some wavelength λ_0 for single-layer AR coating is

1. Optical thickness of the coating is $\lambda_0/4$, that is $n_1 d_1 = \lambda_0/4$.
2. The refraction index n_1 of the coating must satisfy $n_1 = \sqrt{n_0 n_2}$.

If satisfying these two conditions, the coating is matching to the substrate and incident medium.

3.2. Double-layer AR coatings

Refraction indices of a substrate and an incident medium are n_3 and n_0, respectively. And refraction indices of double-layer AR coatings are n_1 and n_2, respectively, as shown in Figure 3. Then the interference matrix is

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$$\begin{pmatrix} B \\ C \end{pmatrix} = \begin{pmatrix} \cos\delta_1 & i\sin\delta_1 / n_1 \\ in_1 \sin\delta_1 & \cos\delta_1 \end{pmatrix} \begin{pmatrix} \cos\delta_2 & i\sin\delta_2 / n_2 \\ in_2 \sin\delta_2 & \cos\delta_2 \end{pmatrix} \begin{pmatrix} 1 \\ n_3 \end{pmatrix} \tag{4}$$

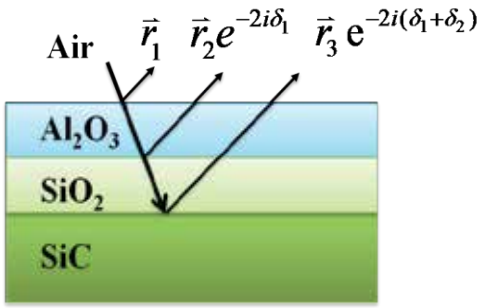

Figure 3. Incidence of UV light from double-layer AR films to a SiC substrate (multiple reflections in AR films are ignored).

$$Y = \frac{C}{B} \tag{5}$$

If $Y = n_0$, the $R = 0$, the two following equations can be obtained:

$$\tan\delta_1 \tan\delta_2 = \frac{n_1 n_2 \left(n_3 - n_0\right)}{n_1^2 n_3 - n_0 n_2^2} \tag{6}$$

$$\frac{\tan\delta_2}{\tan\delta_1} = \frac{n_2 \left(n_0 n_3 - n_1^2\right)}{n_1 \left(n_2^2 - n_0 n_3\right)} \tag{7}$$

The equations can be transformed into

$$\tan^2\delta_1 = \frac{\left(n_3 - n_0\right)\left(n_2^2 - n_0 n_3\right) n_1^2}{\left(n_1^2 n_3 - n_0 n_2^2\right)\left(n_0 n_3 - n_1^2\right)} \tag{8}$$

$$\tan^2\delta_2 = \frac{\left(n_3 - n_0\right)\left(n_0 n_3 - n_1^2\right) n_2^2}{\left(n_1^2 n_3 - n_0 n_2^2\right)\left(n_2^2 - n_0 n_3\right)} \tag{9}$$

Generally, there are three cases for the solutions:

1. Set $\delta_1=\delta_2=\frac{\pi}{2}$, if the light beam performs vertical incidence, the optic thicknesses of the two films are both $\lambda_0/4$, that is, $n_1d_1=n_2d_2=\lambda_0/4$, one of the n_1 and n_2 can be fixed at first, another can be solved by Equations (2) and (3).

2. Set n_1 and n_2, according to Equations (2) and (3), δ_1 and δ_2 can be solved. The refraction indices are fixed to solve the thickness of the two films. For the system of air, Al_2O_3, SiO_2 films and 4H-SiC substrate under the vertical incidence of light with the wavelength of $\lambda_0=280$ nm, the refraction indices are $n_0=1.000$, $n_1=1.685$, $n_2=1.495$, $n_3=2.995$, according to (2) and (3), $\delta_1=(2n-1)\frac{\pi}{2}$, $\delta_2=n\pi$ (n = 1, 2, 3...), n = 1 is selected to reduce the optical absorption of the films.

3. Set $\delta_1=\frac{\pi}{2}$, $\delta_2=\pi$, that is, $n_1d_1=\lambda_0/4$ and $n_2d_2=\lambda_0/2$. In this case, the reflectance of the light beam is not influenced by the second layer. However, this layer has an achromatic effect for the light beam with a wavelength of λ_0. Therefore, for the system of air, Al_2O_3, SiO_2 films and 4H-SiC substrate, the third case is the same as the second. The second layer SiO_2 film has no contribution to the reflectance of the light beam. The Al_2O_3 film is the layer that reduces the reflectance.

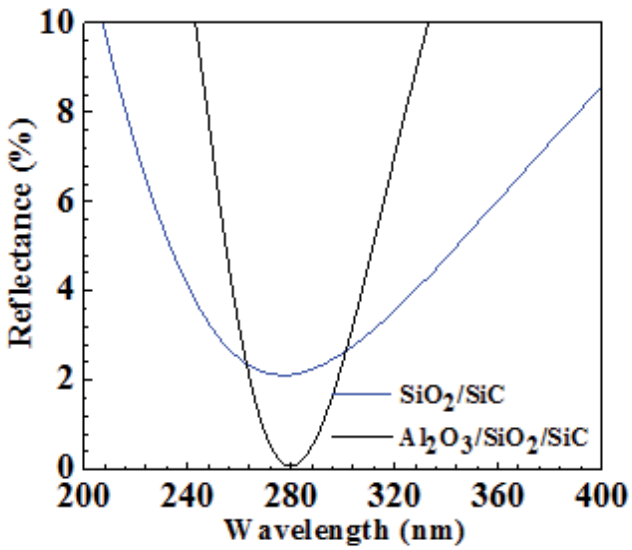

Figure 4. Reflectance spectra of designed Al_2O_3/SiO_2 double and SiO_2 single AR coatings.

Comparison of reflectance has been made between Al_2O_3/SiO_2 double layer and SiO_2 single layer, as shown in Figure 4. (1) The reflectance of the Al_2O_3/SiO_2 film (0.071%) has lower value than that of SiO_2 film (2.1%). (2) The reflectance spectrum of the Al_2O_3/SiO_2 film is narrower than that of SiO_2 film, which indicates that there is a better selection of the wavelength for the

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Al_2O_3/SiO_2 film. Therefore, the Al_2O_3/SiO_2 film is more suitable as the AR coating for the 4H-SiC-based photodetectors.

4. Growth of AR coatings

4.1. Thermal oxidation

SiO_2 formed by thermal oxidation of SiC is most widely used as AR coatings in SiC UV photodetectors. As shown in Figure 5, the SiC wafers are put into the middle of the furnace with permanent temperature. Dry and wet oxygen (with H_2O) are used to oxidize the SiC at 1100°C–1300°C. The oxidation rate is nonlinear and very low that 40-nm-thick SiO_2 layer usually takes 4 h. With the increase of thickness, the oxidation rate is greatly reduced. Although the oxidized SiO_2 is the densest state compared to the other growth methods and the leakage current of SiC devices with the layer is the lowest, absorption is also the largest especially in Si suboxides, which are usually formed at the interface between SiO_2 and SiC. People added NO, N_2O[18, 19], $POCl_3$[20], etc., during the oxidation, which can reduce the sub-oxides and interface states. However, the absorption of the films still cannot be ignored. Thus, the oxidized SiO_2 is suitable for passivation layer not for AR coatings on the window of SiC UV photodetectors.

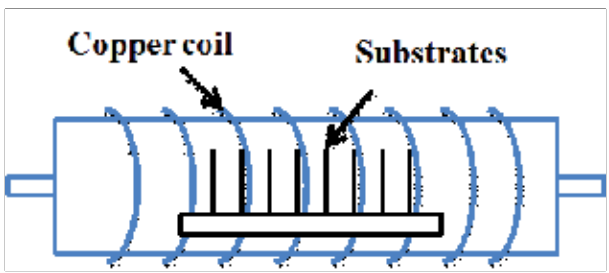

Figure 5. Thermal oxidation system for SiC up to 1300°C.

4.2. Electron beam evaporation

Electron beam evaporation is a physical vapor deposition that is applied to deposit oxides, fluorides, metals, etc. The electron beam is used to heat the surface of bulk materials to be vapor state and then the vapor deposit on the dome with lots of substrates, as illustrated in Figure 6. The AR coatings prepared by electron beam evaporation usually have high transmittance and low absorption, which perfectly meet the requirement of the AR coatings so that optical films are widely deposited and grown by using this technique. A shortcoming of the technique is that the deposited films are not as dense as that prepared by other techniques such as oxidation and sputtering, which may induce large leakage current in the 4H-SiC photodetectors. Therefore, the electron beam evaporation can be applied to grow AR coatings on the

windows of the 4H-SiC photodetectors but is not suitable for deposition of passivation layer to reduce the leakage current.

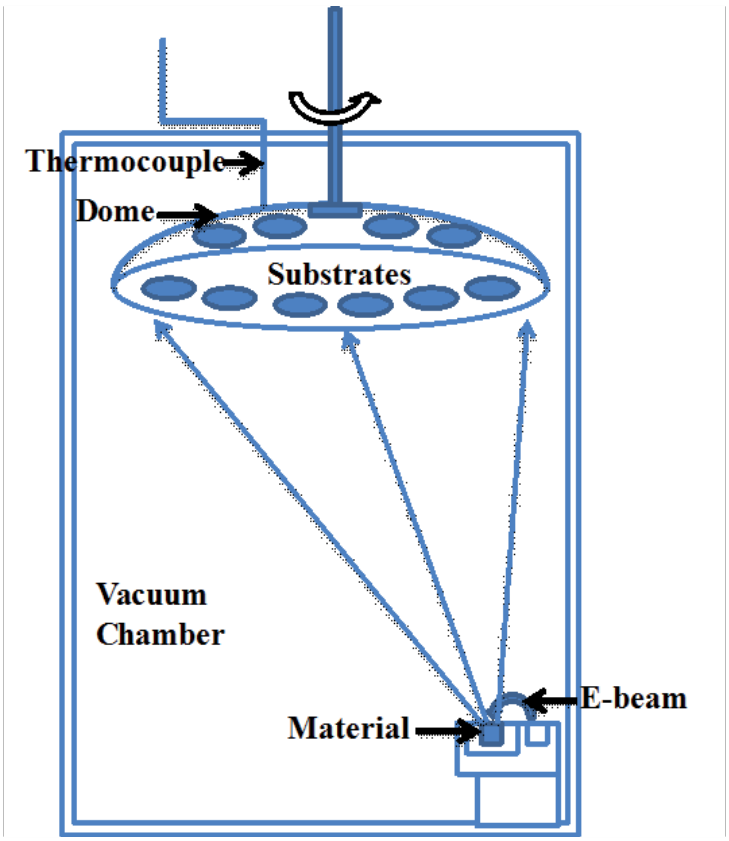

Figure 6. Cross-section view of electron beam evaporation system.

4.3. Atomic layer deposition

Atomic layer deposition (ALD) is a special chemical vapor deposition that is widely applied in microelectronic and optoelectronic fields to deposit oxides, nitrides, metals, etc[21-23]. As illustrated in Figure 7, the precursors and oxidants are pulsed into the chamber successively to deposit on the surface of the substrates monolayer by monolayer and cleaned by inert gases such as nitrogen during the deposition. A deposition sequence is usually that oxidants → nitrogen → precursors → nitrogen.

The precursors and oxidants do not meet and react with each other directly, otherwise, that would be a typical chemical vapor deposition. Al_2O_3[24], SiO_2[25] and HfO_2[26] films are usually grown by using ALD as gate dielectrics in microelectronic fields, which are so uniform that they can be deposited on a rough surface with almost the same thickness by using this technique. The leakage current can also be restrained well through the deposition. Optical

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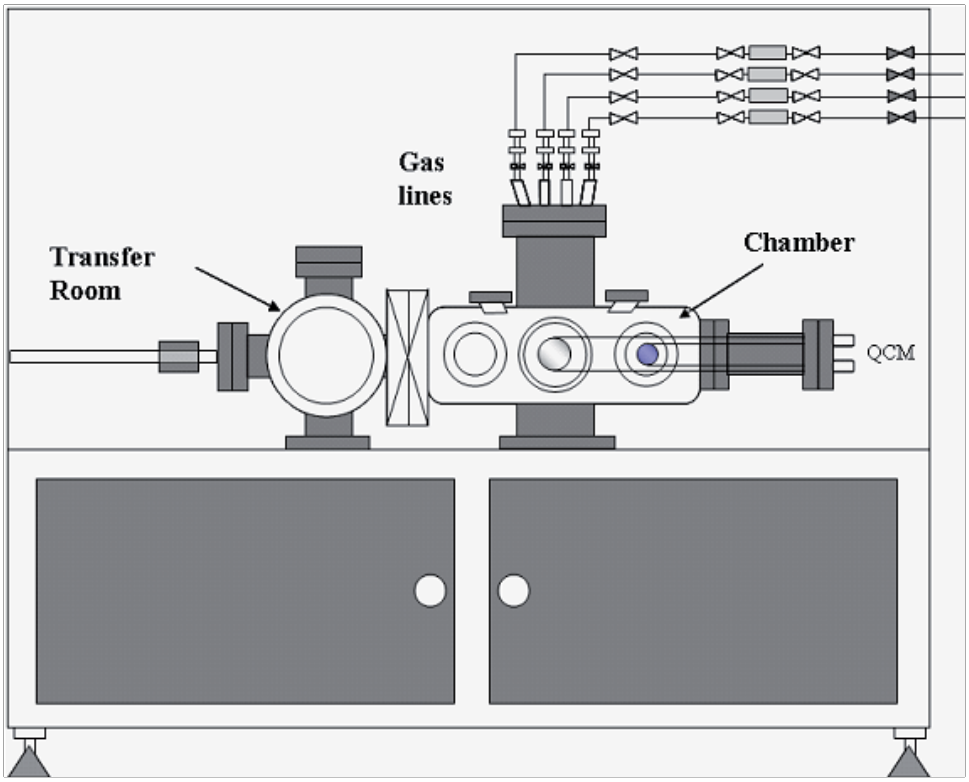

Figure 7. Atomic layer deposition system with *in situ* quartz crystal microbalance.

properties of ALD films[27, 28] were examined and demonstrated that ALD can be an advanced technique to balance the optical and electrical properties of thin films. In order to get the best optical and electrical properties, thermal oxidation and electron beam evaporation were both applied to deposit Al_2O_3 and SiO_2 AR films. SiC UV photodetectors with Al_2O_3 and SiO_2 AR films are studied and demonstrated in the following sections.

5. SiC Photodetectors with Al_2O_3 and SiO_2 films

5.1. 4H-SiC MSM photodetectors with Al_2O_3 and SiO_2 films

Two 4H-SiC MSM photodetectors were separately fabricated with electron beam-evaporated Al_2O_3/SiO_2 double-layer films and thermal SiO_2 single-layer films for comparison, which were prepared on two identical n-type 4H-SiC wafers with epilayers of 3.4 μm and doping level of 3.0×10^{15} cm^{-3}. One of them was oxidized at 1150°C in an O_2 atmosphere for 4 h. The final thickness of the SiO_2 layer was approximately 40 nm, as measured by an ellipsometer. SiO_2 and $A1_2O_3$ layers were successively deposited on the other wafer by electron beam evaporation. The final thicknesses of the $A1_2O_3$ and SiO_2 films were 42 nm and 96 nm, respectively,

which are quarter-wave and half-wave of the UV wavelength of 280 nm corresponding to calculated peak responsivity. Then, the reflectance spectra of these samples were measured by a commercial spectrophotometer. After confirmation of the spectra, the device fabrication process was immediately performed on two samples. Lithography and wet etching were done on the samples, then interdigitated electrodes were deposited by sputtering Au and Ni with a width and spacing of 2 and 2 μm, as shown in Figure 8. Finally, Au bonding pads were deposited on the ends of the electrodes. The spectral response measurements were performed on the devices by using a light source of LAX 1450 M Xe lamp and an Actron SpectraPro-2500i monochromator. The output power of the monochromatic light was measured and calibrated by a Si 222 photodetector. Then the light was illuminated on these two MSM photodetectors. The current-voltage (I–V) characteristics of these devices were measured by using an electrometer and sourcemeter.

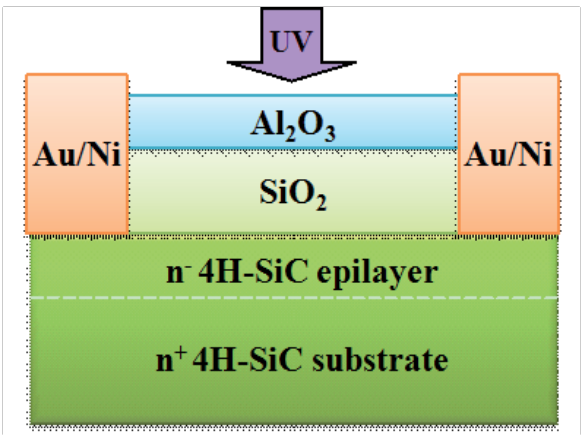

Figure 8. A cross-sectional view of 4H-SiC MSM photodetectors with Al_2O_3 and SiO_2 films deposited by using electron beam evaporation.

These two Al_2O_3/SiO_2/4H-SiC and SiO_2/4H-SiC MSM devices both exhibit excellent optoelectronic properties, as presented in Figure 9(a). The photocurrent of Al_2O_3/SiO_2/4H-SiC devices are approximately double that of SiO_2/4H-SiC due to the lower reflection and absorption of Al_2O_3/SiO_2 films. Meanwhile, the photocurrent of SiO_2/4H-SiC devices increased with increasing voltage, which may be attributed to the charge traps at the interface between SiO_2 and 4H-SiC. The dark current of the SiO_2/4H-SiC (around 0.50 pA) was lower than that of the Al_2O_3/SiO_2/4H-SiC devices (7.5 pA at 10 V), as shown in Figure 9(b), which is attributed to the fact that the thermally grown SiO_2 layer on 4H-SiC substrates was denser than the electron beam evaporated Al_2O_3/SiO_2 films to restrain the leakage current of the devices.

Spectral responses of Al_2O_3/SiO_2/4H-SiC and SiO_2/4H-SiC MSM photodetectors were measured under reverse voltage from 5 to 20 V, as shown in Figure 10(a). The peak responsivity of Al_2O_3/SiO_2/4H-SiC photodetectors is 0.12 A/W at 20 V, which is more than twice that of SiO_2/4H-SiC (0.055 A/W at 20 V) due to the lower reflection on Al_2O_3/SiO_2/4H-SiC surface, as shown in Figure 10(b). Both devices achieved high UV to visible rejection ratio of $>10^3$. The

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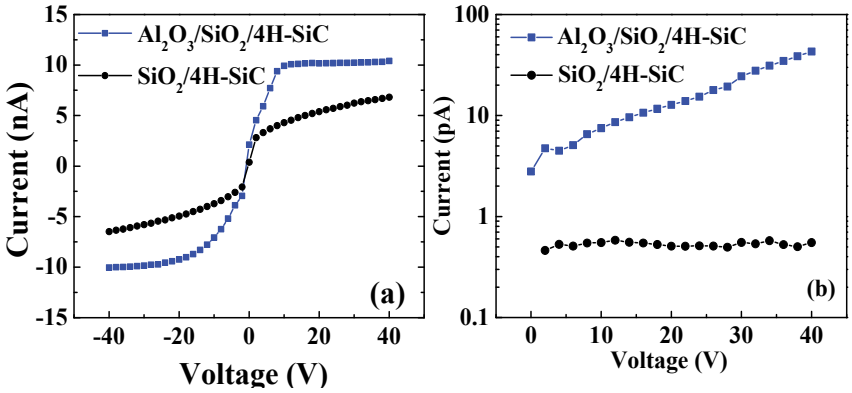

Figure 9. (a) Photocurrent and (b) dark (leakage) current of 4H-SiC MSM photodetectors with Al_2O_3/SiO_2 double-layer and thermal SiO_2 single-layer films. Reproduced with permission from Ref. [5].

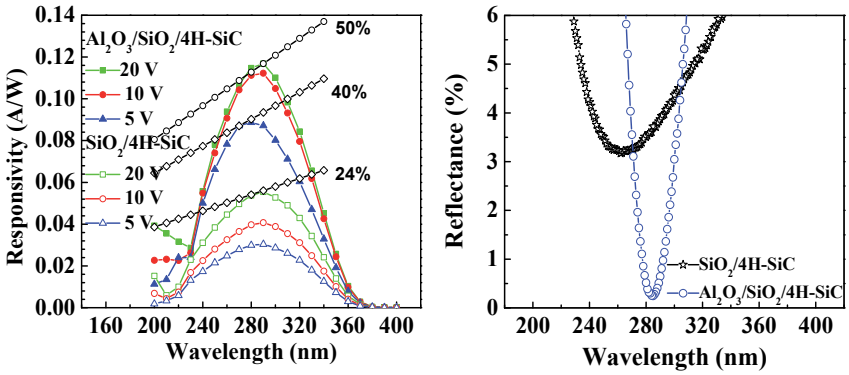

Figure 10. (a) Spectral response and external quantum efficiency of SiO_2/4H-SiC and Al_2O_3/SiO_2/4H-SiC MSM photodetectors under reverse voltages from 5 to 20 V. (b) Reflection spectra of the thermally grown SiO_2 layer and evaporated Al_2O_3/SiO_2 films on 4H-SiC from 200 to 400 nm. Reproduced with permission from Ref. [5].

minimum reflectance of SiO_2/4H-SiC was 3.2% at 262 nm, more than twelve times higher than that of Al_2O_3/SiO_2/4H-SiC (0.25% at 284 nm close to the reference wavelength 280 nm). However, the peak responsivity of the SiO_2/4H-SiC detectors was kept at a wavelength of 290 nm with the increasing voltage, which mainly relied on the thickness of the active epilayer (3.4 μm). The penetration depths of 4H-SiC were approximately 2.8 and 3.6 μm at the wavelengths of 290 and 300 nm, respectively, which indicates that photons can penetrate the active layer at the wavelength of 300 nm. Meanwhile, the shorter-wavelength light was also absorbed by the thermally grown SiO_2 layer and the difference of reflectance between 260 nm and 290 nm was very small. Therefore, the wavelength corresponding to peak responsivity is 290 nm in SiO_2/4H-SiC devices. The same phenomenon and analysis can also be observed and used in the Al_2O_3/SiO_2/4H-SiC detectors.

The external quantum efficiency η_e of photodetectors can be obtained from $\eta_e \cong 1241R/\lambda$ [29], where R is the responsivity in A/W and λ is the wavelength in nanometer. The maximum external quantum efficiency of the Al_2O_3/SiO_2/4H-SiC UV photodetectors was approximately 50% at 280 nm, which is twice as much as that of SiO_2/4H-SiC devices, as shown in Figure 10(a). These results were consistent with the reflectance of the Al_2O_3/SiO_2/4H-SiC, which achieved the minimum of 0.25% at 280 nm on Al_2O_3/SiO_2/4H-SiC and was just 1/14 of SiO_2/4H-SiC, as shown in Figure 10(b). The relationship between external quantum efficiency η_e and internal η_i of MSM photodetectors can be expressed by the following equation:

$$\eta_e = \eta_i(1-R)\left[1-\exp(-\alpha d)\right]\left[W_s/(W_f+W_s)\right] \tag{10}$$

where R is the reflectance of photodetectors, α and d are the absorption coefficient and thickness of the active layer, W_f and W_s are separately the widths of electrodes and spacing. The internal quantum efficiencies were calculated to be 77% and 38% at 280 nm for Al_2O_3/SiO_2/4H-SiC and SiO_2/4H-SiC photodetectors, respectively. The highest quantum efficiency was obtained for 4H-SiC-based MSM photodetectors with Al_2O_3/SiO_2 films, which indicates that the Al_2O_3/SiO_2 AR coatings can improve the optical and electrical properties efficiently.

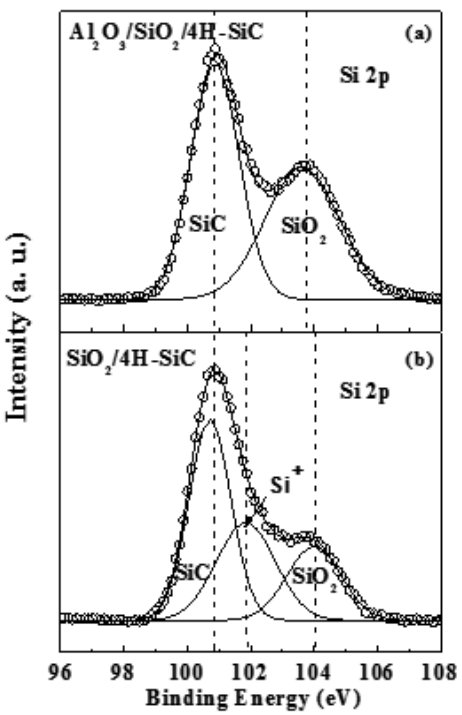

Figure 11. X-ray photoelectron spectra of (a) electron beam evaporated Al_2O_3/SiO_2 films and (b) thermally grown SiO_2 layer.

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The absorption of Al_2O_3/SiO_2 films was ignored in the above expression because of the low extinction coefficients (10^{-5}) of the coatings prepared by electron beam evaporation and inexistence of Si suboxides, as shown in Figure 11(a). While the absorption of the thermally grown SiO_2 layer cannot be ignored due to the larger density and Si sub-oxides such as Si^+ at the SiO_2/4H-SiC interface, as shown in Figure 11(b), which are the reasons for the low quantum efficiency of SiO_2/4H-SiC photodetectors.

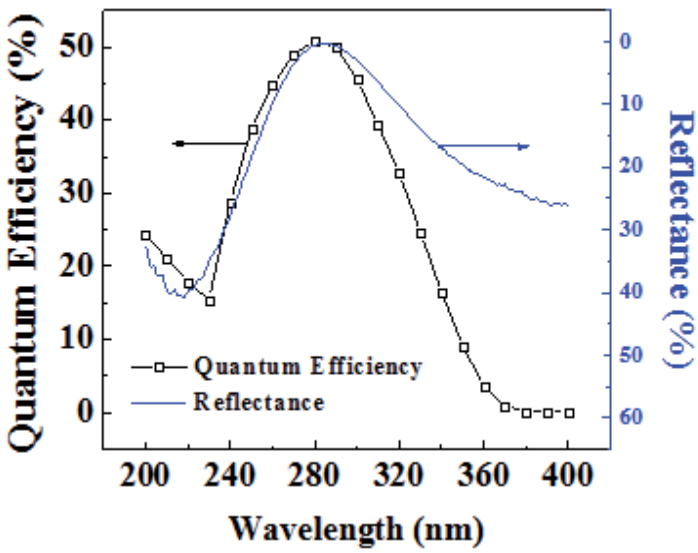

Figure 12. Comparison of spectral response and reflection spectra of Al_2O_3/SiO_2/4H-SiC MSM UV photodetectors. Reproduced with permission from Ref. [5].

Comparisons between reflectance and response spectra were made in the Al_2O_3/SiO_2/4H-SiC photodetectors to examine the spectral restriction effect of the Al_2O_3/SiO_2 films, as shown in Figure 12. The spectral response is not exactly consistent with the reflectance from 200 to 240 nm, which may be due to the influence of the surface recombination. Then the variation of the spectral response matches the reflectance from 240 to 300 nm, which indicates that reflection is the dominant factor when the photons can be absorbed by the active layer completely as discussed above. Spectral response is not consistent with the reflectance from 300 to 380 nm, which is attributed to the fact that the photons can only be absorbed partly by the epilayer so that the photon absorption became dominant and the restriction effect of Al_2O_3/SiO_2 films weakened.

The 4H-SiC MSM photodetectors with Al_2O_3/SiO_2 AR coatings and SiO_2 layer were fabricated and demonstrated. The highest responsivity and maximum external quantum efficiency were obtained with the Al_2O_3/SiO_2 films, which proved that the design and application of Al_2O_3/SiO_2 films on the 4H-SiC MSM photodetectors are successful. The optical and electrical properties of the Al_2O_3/SiO_2 films prepared by electron beam evaporation will be further studied in 4H-SiC MIS photodetectors.

5.2. 4H-SiC MIS Photodiodes with Al_2O_3 and SiO_2 films

Two 4H-SiC MIS UV photodetectors with Al_2O_3/SiO_2 and SiO_2 films were fabricated on 4H-SiC wafers with a structure of 250 nm p type ($N_A = 1.6 \times 10^{19}$ cm^{-3}) top layer and 2300 nm n type ($N_D = 5 \times 10^{15}$ cm^{-3}) epitaxial layer on an n type ($N_D = 1 \times 10^{20}$ cm^{-3}) substrate. The substrate and epilayers both have orientations of 8° off the Si face (0001). Photoactive windows (200 × 200 μm^2) were defined by using inductively coupled plasma (ICP) etcher. Wafers were oxidized in oxygen in the same conditions mentioned in the fabrication of MSM photodetectors and 40 nm SiO_2 layers were obtained. Lithography and wet etching were carried out on the SiO_2 layers until 6 nm left, as shown in Figure 13. Then Au and Ni/Au electrodes were deposited on the top and backside of 4H-SiC wafers and annealed at 1050°C in Ar for 5 min to get the ohmic contact. 42 nm thick Al_2O_3 and 48 nm thick SiO_2 films were deposited as AR coatings on one 4H-SiC wafer by electron-beam evaporation. Thus, the final thicknesses of $A1_2O_3/SiO_2$ stack films were 42 and 88 nm, respectively. Then the reflection spectra of SiO_2 and $A1_2O_3/SiO_2$ films on 4H-SiC substrates were examined by using a commercial spectrophotometer, respectively. Finally, the SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC MIS photodetectors were finished.

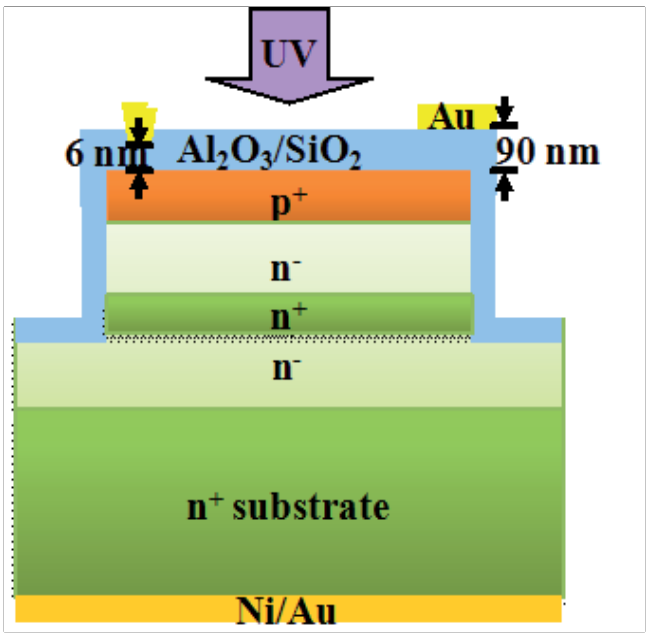

Figure 13. A cross-sectional schematic of 4H-SiC MIS photodetectors with Al_2O_3/SiO_2 films.

Photocurrents of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC MIS detectors are shown in Figure 14(a). The photocurrents of $A1_2O_3/SiO_2$/4H-SiC device was almost triple as much as that of SiO_2/4H-SiC at 10 V, which is attributed to the fact that more photons can be absorbed by the devices with lower reflectance of $A1_2O_3/SiO_2$ films and generate more electron-hole pairs than the device with thermally grown SiO_2 layer.

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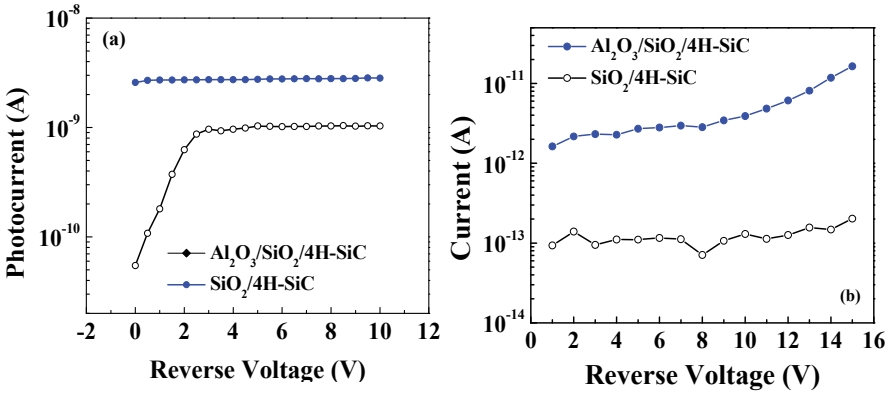

Figure 14. (a) Photocurrent and (b) leakage current of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC MIS photodetectors. Reproduced with permission from Ref. [10].

The MIS photodetectors are actually a combination of MIS and p-i-n devices. Thus, the photocurrent was determined by both MIS and p-i-n structures in the devices. When the SiO_2 layer in MIS was tunneled at a certain voltage, p-i-n junction restrained the tunneling currents so that the photocurrent was constant, as illustrated in Figure 14(a). However, the photocurrent of $A1_2O_3/SiO_2$/4H-SiC saturated form 0 V while that of S/4H-SiC saturated from 2.5 V, which is attributed to the fact that lots of electrons were trapped in the evaporated $A1_2O_3/SiO_2$ films as described above, and the charges made holes accumulate on the surface of 4H-SiC substrate and tunneled through the SiO_2 layer. Therefore, built-in field and depletion regions were formed in the p-i-n structure and photocurrent can be generated without voltage applied, which is called the normally-on mode. However, the charges in SiO_2/4H-SiC photodetectors were few so that the carriers could not tunnel through the SiO_2 layer. A certain voltage needs to be applied on the device to achieve this purpose, which can be recognized as normally-off mode.

Leakage (dark) currents of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC MIS photodetectors were measured from 0 to 15 V to examine the electrical property of these films, as shown in Figure 14(b). Good passivation property of SiO_2/4H-SiC was achieved for that the leakage current was lower than 0.13 pA at 10 V. However, the leakage current of the $A1_2O_3/SiO_2$/4H-SiC MIS device was 3.9 pA at 10 V, nearly 30 times higher than that of SiO_2/4H-SiC device, which is due to the fact that the electron beam-evaporated $A1_2O_3/SiO_2$ films were not as dense as the thermally grown SiO_2 layers and had trapped charges when the films were prepared. Thus, the electrical properties of the electron beam evaporated $A1_2O_3/SiO_2$ films need to be further improved.

The spectral response of the 4H-SiC UV detectors with $A1_2O_3/SiO_2$ and SiO_2 films were measured and studied in the wavelength range from 200 to 400 nm. The peak responsivities of these devices were 30 mA/W at 260 nm with a single SiO_2 layer and 50 mA/W at 270 nm with $A1_2O_3/SiO_2$ double-layer, respectively, as shown in Figure 15(a). The surface reflectances of the two coatings on 4H-SiC substrate are shown in Figure 15(b). The minimum reflectance of $A1_2O_3/SiO_2$ films is 0.34% nm and only 1/10 of single SiO_2 layer, which agrees well with the

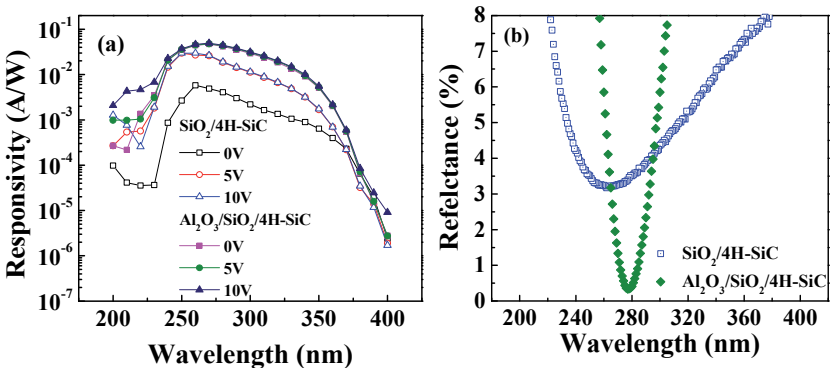

Figure 15. (a) Spectral response of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC MIS detectors from 200 to 400 nm at 0 to 10 V. (b) Reflection spectra of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC in the spectral range of 200–400 nm. Reproduced with permission from Ref. [10].

AR coatings designed above. It is interesting that the peak responsivity of the $A1_2O_3/SiO_2$/4H-SiC detectors is not at the wavelength of 280 nm, which corresponds to the minimum reflectance of the $A1_2O_3/SiO_2$ films. The following reasons can be considered. First, the active region length in the device is 2.25 μm, including the thickness of depletion region and hole diffusion length. The penetration depths of the wavelength at 270 and 280 nm are 1.83 and 2.30 μm[30], respectively, so that the 270 nm UV light can be absorbed completely. Thus, the peak responsivity of the $A1_2O_3/SiO_2$/4H-SiC MIS photodetectors is at the wavelength of 270 nm. Meanwhile, the diffusion length of the electron is approximately 21 μm, which is longer than the nonintentionally doped n-type epilayer so that the electrons can approach the bottom electrode easily. The responsivity of these two devices was not as much as above MSM photodetectors because the carriers need to tunnel through the 6 nm SiO_2 insulator in the MIS detectors, which reduced the quantum efficiency and responsivity. Nevertheless, the leakage current of the MIS device was improved greatly, which is only 1/5 of the MSM device. The UV-to-visible rejection ratios in MIS detectors also achieved 2×10^3 by using the $A1_2O_3/SiO_2$ double-layer AR coatings, which is the highest in 4H-SiC-based MIS photodetectors and is attributed to good passivation property of thermally grown SiO_2 layer and $A1_2O_3/SiO_2$ double-layer and low leakage current.

In the wavelength from 250 to 380 nm, the responsivity of 4H-SiC MIS detectors with $A1_2O_3/SiO_2$ film is higher than that of with SiO_2 film, as shown in Figure 15(a). The wavelength range is even wider than the lower reflectance region (260 to 300 nm) of the $A1_2O_3/SiO_2$ films, as shown in Figure 15(b). I-V characteristics of these two devices were performed without UV exposure to study the wideband higher response. Ohmic conduction mechanism is dominant according to the current curve-fitting in the low electric field, as illustrated in Figure 16(a). Fowler–Nordheim (FN) tunneling is converted to the main conduction mechanism in both devices with increasing electric field (E), which can be expressed by[31]

$$J = A \bullet E^2 \exp\left(-B / E\right) \tag{11}$$

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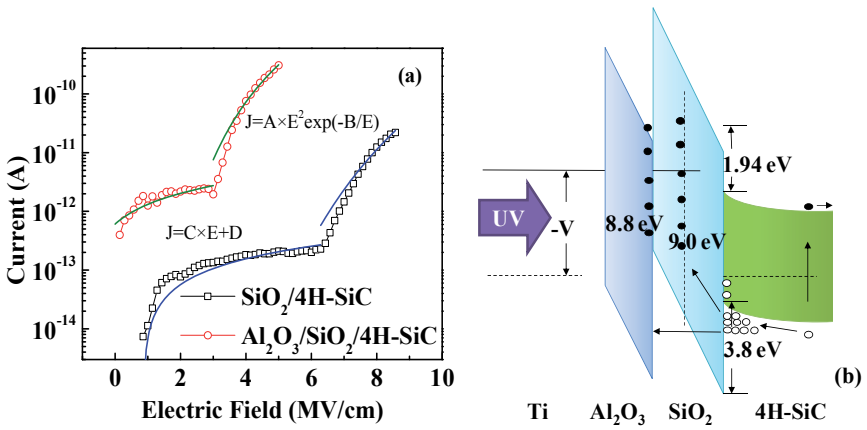

Figure 16. (a) I-V characteristics of SiO_2/4H-SiC and $A1_2O_3/SiO_2$/4H-SiC photodetectors without UV exposure and (b) band alignment of $A1_2O_3/SiO_2$/4H-SiC structure under UV exposure in accumulation state. Reproduced with permission from Ref. [10].

where $A = q^3 m_{SiC}/(8\pi h m_i \Phi_B)$ and $B = 4(2m_i\Phi_B^3)^{1/2}/(3q\hbar)$. q is the electron charge, m_{SiC} and m_i are effective electron masses in 4H-SiC and SiO_2, respectively. h ($\hbar$) is the (reduced) Planck constant, and Φ_B is the barrier height of SiO_2 on 4H-SiC. The Φ_B was calculated to be 1.94 eV by using Equation (10). Then, the valence band offset was 3.8 eV by using $E_v = E_{SiO2} - E_{4H\text{-}SiC} - \Phi_B$, where E_v, E_{SiO2} and $E_{4H\text{-}SiC}$ are valence band offset, band gaps of SiO_2 and 4H-SiC, respectively. Then, band alignments of the $A1_2O_3/SiO_2$/4H-SiC and SiO_2/4H-SiC were obtained, as shown in Figure 16(b). Tunneling probability (T) was increased through the electrons trapped in evaporated $A1_2O_3/SiO_2$ films attract more holes. The responsivity (R_{rep}) of the MIS photodetectors is determined by $R_{rep} = (\lambda/1241)\bullet(1 - R - A_{film})\bullet T$. where λ is wavelength of incident light, R and A_{film} are reflectance and absorptance of AR coatings, respectively. According to the expression, the tunneling probability of holes in the SiO_2 films was lower than in the $A1_2O_3/SiO_2$ films so that high spectral response range can be wider than low reflectance region.

4H-SiC-based MIS UV photodetectors with thermally grown SiO_2 layer and evaporated $A1_2O_3/SiO_2$ films were fabricated and demonstrated. Low leakage current and high UV-to-visible rejection ratios >2 × 10^3 had been achieved for these devices. The 4H-SiC MIS photodetectors with $A1_2O_3/SiO_2$ AR coatings presented higher responsivity and quantum efficiency, which demonstrate that the design and deposition of Al_2O_3/SiO_2 films are effective and significant for the 4H-SiC UV photodetectors.

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Author details

Feng Zhang

Address all correspondence to: fzhang@semi.ac.cn

Key Laboratory of Semiconductor Material Sciences, Institute of Semiconductors, Chinese Academy of Sciences, Beijing, People's Republic of China

References

[1] F. Yan, X. B. Xin, S. Aslam, Y. G. Zhao, D. Franz, J. H. Zhao, *et al.* 4H-SiC UV photo detectors with large area and very high specific detectivity. Ieee Journal of Quantum Electronics 2004; 40 1315-1320.

[2] M. Mazzillo, G. Condorelli, M. E. Castagna, G. Catania, A. Sciuto, F. Roccaforte, *et al.* Highly Efficient Low Reverse Biased 4H-SiC Schottky Photodiodes for UV-Light Detection. Ieee Photonics Technology Letters 2009; 21 1782-1784.

[3] A. Sciuto, F. Roccaforte, S. Di Franco, V. Raineri, and G. Bonanno. High responsivity 4H-SiC Schottky UV photodiodes based on the pinch-off surface effect. Applied Physics Letters 2006; 89.

[4] Y. K. Su, Y. Z. Chiou, C. S. Chang, S. J. Chang, Y. C. Lin, and J. F. Chen. 4H-SiC metal-semiconductor-metal ultraviolet photodetectors with Ni/ITO electrodes. Solid-State Electronics 2002; 46 2237-2240.

[5] F. Zhang, W. F. Yang, H. L. Huang, X. P. Chen, Z. G. Wu, H. L. Zhu, *et al.* High-performance 4H-SiC based metal-semiconductor-metal ultraviolet photodetectors with Al(2)O(3)/SiO(2) films. Applied Physics Letters 2008; 92.

[6] W. C. Lien, D. S. Tsai, D. H. Lien, D. G. Senesky, J. H. He, and A. P. Pisano. 4H-SiC Metal-Semiconductor-Metal Ultraviolet Photodetectors in Operation of 450 degrees C. Ieee Electron Device Letters 2012; 33 1586-1588.

[7] X. P. Chen, H. L. Zhu, J. F. Cai, and Z. Y. Wua. High-performance 4H-SiC-based ultraviolet p-i-n photodetector. Journal of Applied Physics 2007; 102.

[8] X. F. Liu, G. S. Sun, J. M. Li, J. Ning, Y. M. Zhao, M. C. Luo, *et al.* Vertical PIN ultraviolet photodetectors based on 4H-SiC homoepilayers. Physica Status Solidi C - Current Topics in Solid State Physics, Vol 4, No 5 2007; 4 1609-1612.

[9] J. F. Cai, X. P. Chen, R. D. Hong, W. F. Yang, and Z. Y. Wu. High-performance 4H-SiC-based p-i-n ultraviolet photodiode and investigation of its capacitance characteristics. Optics Communications 2014; 333 182-186.

[10] F. Zhang, G. S. Sun, H. L. Huang, Z. Y. Wu, L. Wang, W. S. Zhao, *et al.* High-Performance 4H-SiC-Based Metal-Insulator-Semiconductor Ultraviolet Photodetectors With SiO2 and Al2O3/SiO2 Films. Ieee Electron Device Letters 2011; 32 1722-1724.

[11] F. Yan, J. H. Zhao, and G. H. Olsen. Demonstration of the first 4H-SiC avalanche photodiodes. Solid-State Electronics 2000; 44 341-346.

[12] X. Y. Guo, L. B. Rowland, G. T. Dunne, J. A. Fronheiser, P. M. Sandvik, A. L. Beck, *et al.* Demonstration of ultraviolet separate absorption and multiplication 4H-SiC avalanche photodiodes. Ieee Photonics Technology Letters 2006; 18 136-138.

[13] X. G. Bai, H. D. Liu, D. C. McIntosh, and J. C. Campbell. High-Detectivity and High-Single-Photon-Detection-Efficiency 4H-SiC Avalanche Photodiodes. Ieee Journal of Quantum Electronics 2009; 45 300-303.

[14] F. Zhang, H. L. Zhu, W. F. Yang, Z. Y. Wu, H. J. Qi, H. B. He, *et al.* Al2O3/SiO2 films prepared by electron-beam evaporation as UV antireflection coatings on 4H-SiC. Applied Surface Science 2008; 254 3045-3048.

[15] H. A. Macleod. Thin-Film Optical Filters: Institute of Physics Publishing; 2001.

[16] R. Singh. Reliability and performance limitations in SiC power devices. Microelectronics Reliability 2006; 46 713-730.

[17] M. E. Levinshteĭn, S. L. Rumyantsev, and M. Shur. Properties of advanced semiconductor materials : GaN, AlN, InN, BN, SiC, SiGe: Wiley; 2001.

[18] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev. Mechanisms responsible for improvement of 4H-SiC/SiO2 interface properties by nitridation. Applied Physics Letters 2003; 82 568-570.

[19] P. Jamet, S. Dimitrijev, and P. Tanner. Effects of nitridation in gate oxides grown on 4H-SiC. Journal of Applied Physics 2001; 90 5058-5063.

[20] D. Okamoto, H. Yano, T. Hatayama, and T. Fuyuki. Removal of near-interface traps at SiO2/4H-SiC (0001) interfaces by phosphorus incorporation. Applied Physics Letters 2010; 96.

[21] H. Kim. Atomic layer deposition of metal and nitride thin films: Current research efforts and applications for semiconductor device processing. Journal of Vacuum Science & Technology B 2003; 21 2231-2261.

[22] F. Zhang, G. S. Sun, L. Zheng, S. B. Liu, B. Liu, L. Dong, *et al.* Interfacial study and energy-band alignment of annealed Al2O3 films prepared by atomic layer deposition on 4H-SiC. Journal of Applied Physics 2013; 113.

[23] R. L. Puurunen. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. Journal of Applied Physics 2005; 97.

[24] C. M. Tanner, Y. C. Perng, C. Frewin, S. E. Saddow, and J. P. Chang. Electrical performance of Al2O3 gate dielectric films deposited by atomic layer deposition on 4H-SiC. Applied Physics Letters 2007; 91.

[25] S. M. George, A. W. Ott, and J. W. Klaus. Surface chemistry for atomic layer growth. Journal of Physical Chemistry 1996; 100 13121-13131.

[26] M. H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D. H. Ko, *et al.* Thermal stability and structural characteristics of HfO2 films on Si (100) grown by atomic-layer deposition. Applied Physics Letters 2002; 81 472-474.

[27] J. Aarik, H. Mandar, M. Kirm, and L. Pung. Optical characterization of HfO2 thin films grown by atomic layer deposition. Thin Solid Films 2004; 466 41-47.

[28] Y. Kim, S. M. Lee, C. S. Park, S. I. Lee, and M. Y. Lee. Substrate dependence on the optical properties of Al2O3 films grown by atomic layer deposition. Applied Physics Letters 1997; 71 3604-3606.

[29] B. K. Ng, J. P. R. David, R. C. Tozer, G. J. Rees, F. Yan, C. Qin, *et al.* Performance of thin 4H-SiC UV avalanche photodiodes. Iee Proceedings-Optoelectronics 2003; 150 187-190.

[30] S. G. Sridhara, R. P. Devaty, and W. J. Choyke. Absorption coefficient of 4H silicon carbide from 3900 to 3250 angstrom. Journal of Applied Physics 1998; 84 2963-2964.

[31] K. Y. Cheong, J. H. Moon, H. J. Kim, W. Bahng, and N. K. Kim. Current conduction mechanisms in atomic-layer-deposited HfO(2)/nitrided SiO(2) stacked gate on 4H silicon carbide. Journal of Applied Physics 2008; 103.

Chapter 8

Silicon Carbide for Novel Quantum Technology Devices

Stefania Castelletto, Lorenzo Rosa and
Brett C. Johnson

Additional information is available at the end of the chapter

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Abstract

Silicon carbide (SiC) has recently been investigated as an alternative material to host deep optically active defects suitable for optical and spin quantum bits. This material presents a unique opportunity to realise more advanced quantum-based devices and sensors than currently possible. We will summarise key results revealing the role that defects have played in enabling optical and spin quantum measurements in this material such as single photon emission and optical spin control. The great advantage of SiC lies in its existing and well-developed device processing protocols and the possibilities to integrate these defects in a straightforward manner. There is particular current interest in nanomaterials and nanophotonics in SiC that could, once realised, introduce a new platform for quantum nanophotonics and in general for photonics. We will summarise SiC nanostructures exhibiting optical emission due to multiple polytypic bandgap engineering and deep defects. The combination of nanostructures and in-built paramagnetic defects in SiC could pave the way for future single-particle and single-defect quantum devices and related biomedical sensors with single-molecule sensitivity. We will review relevant classical devices in SiC (photonics crystal cavities, microdiscs) integrated with intrinsic defects. Finally, we will provide an outlook on future sensors that could arise from the integration of paramagnetic defects in SiC nanostructures and devices.

Keywords: Silicon carbide deep defects, Paramagnetic properties, Optical-detected magnetic resonance, Single-photon sources

1. Introduction

The most common and technologically advanced SiC polytypes are 4H-SiC and 6H-SiC with hexagonal structures and 3C-SiC with a zinc-blende crystal structure (cubic). High-quality

bulk single-crystal 3C-SiC can be grown epitaxially on different substrates, most notably on silicon. This has led to many exciting devices fabricated with this particular polytype[1]. SiC has a wide bandgap (2.4-3.2 eV depending on the polytype), a high thermal conductivity, the ability to sustain high electric fields before breakdown and the highest maximum current density, making it ideal for high-power electronics [2]. More recently, it has become a notable material in the field of quantum computing and spintronics as several of its intrinsic defects are associated with an electron spin that can be used as quantum bit [3, 4]. To enhance solid-state quantum systems scalability, a fully integrated device with quantum control should be built; thus, quantum systems should be part of the material used to fabricate the final device. Other solid-state quantum systems fully integrated into a functional device[5–7] operate at cryogenic temperatures (4 K or below), limiting their engineering and scalability. A room temperature solid-state "qubit" is the nitrogen vacancy (NV) centre[8] in diamond; yet diamond is not mature for standard device fabrication protocols. SiC, on the other hand, is widely used in LEDs (commonly as a substrate for GaN films), power electronics and microelectromechanical and nano-electromechanical systems (MEMs, NEMs) [9, 10] and has well-developed device processing protocols which are compatible with industry standards. In addition, nanostructures can be formed in SiC such as nanoparticles, quantum dots, nanowires and nanopillars. The ability to grow SiC on silicon provides an unprecedented advantage which facilitates the fabrication of nanophotonic cavities[11, 12]. As a compound semiconductor, SiC harbours a rich assortment of optically active intrinsic and extrinsic defects that can be used as quantum systems.

In this chapter, we will summarise key findings and the main properties of deep optical and paramagnetic defects in bulk SiC that very recently have prompted novel quantum effects such as single-photon source (SPS) and quantum coherence control of their spin[13–17]. We will review defects with optical emission used in quantum spintronics and quantum optics, optically detected resonance methods applied to these defects, the achievement of coherent control of ensemble and single spins and their present spin coherence times. We will review single-photon emission from nanostructures of silicon carbide[18, 19]. We will review recent nanophotonics advances[20–30] in this material to achieve defect integration and enhancement. Other applications of the engineered defects in quantum technologies are also summarised. Some challenges still remain before this material can fully realise its potential in advancing quantum technology. In the summary, we critically analyse present challenges based on the reported results and provide an outlook of likely future investigations that can lead to successful application of SiC for quantum devices.

2. Deep defects in SiC with quantum properties

Many deep-energy-level defects within the bandgap give rise to radiative recombination in SiC with photoluminescence (PL) from the UV to the infrared. The dual compound nature and the existence of nonequivalent lattice sites in different polytypes (quasi-cubic, k, and hexagonal, h) give rise to a large variety of possible PL. Here, we will discuss only recently investigated defects that provided so far experimental evidence of quantum effects[14–16]. These defects are intrinsic defects, known as silicon vacancies (V_{Si})[31–33], divacancies ($V_{Si}V_C$)[34] and carbon antisite-vacancy pair ($C_{Si}V_C$)[35, 36]. In Figures 1-3, we show the atomistic defect structure and the presently understood energy levels corresponding to so far identified quantum systems in 4H, 6H and 3C polytypes. These defects coincide with

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the most commonly previously observed intrinsic defects in the material. They can be created in ensemble by neutron or electron irradiation, followed by annealing, as well as they can be created during growth. Recent experimental challenges rely in their creation as isolated systems or individual defects with their correlation to the ensemble level for their identification in bulk SiC. For this to be reliable, due to the large variability properties of the bulk material, which also can present many defects at the same time, the purity of the pristine wafer resulted to be essential. Therefore, the isolation of single defects as quantum systems was performed in high purity 4H intrinsic SiC. These defects act as radiative recombination centres within the bandgap with a PL achieved by out-of-resonance excitation with a laser. The PL is typically characterised by a sharp zero-phonon line (ZPL) and phonon side bands (PSB) at longer emission wavelengths. Recombination centres are modelled as a quantum system with ground, excited and metastable states (a two- or three-level system). These defects can have different ZPLs in the first instance according to the polytype, which provides nonequivalent crystallographic sites in the matrix. Additionally, the material doping can influence the emission wavelength. They are often characterised by a charge state which also can influence the spectral location of the ZPL peak. The charge state is also associated to the spin state (mostly of the ground state) of the defect, which can be observed from PL measurements as a reduction/enhancement (depending on the mechanism of the population of the energy levels) of the PL, when probed with the application of an additional magnetic field or a microwave excitation in resonance with the spin sublevels. Other defects also yielding quantum properties are not yet presently completely identified. The main effect on the variation of the defects ZPLs is related to the polytype, whether the defect occupies an axial position in the lattice (orientation along the c-axis, hh or kk lattice location) or an off-axis position (hk, kh orientation basal); thus, at least 2^n ZPLs can be present for n-nonequivalent crystallographic site positions. In addition, the symmetry of the defects can give rise to other ZPLs with an excited state split by Jahn-Teller distortion, reducing the symmetry and introducing additional ZPLs. V_{Si} consists of a missing silicon atom in the matrix. In 4H-SiC, V_{Si} shows two ZPLs (two nonequivalent sites) stable up to 500-600°C; in addition, two possible charge states are known. The ZPL, known as V_1, emits at 862.2 nm, while V_2 emits at 917.0 nm. These lines have been associated to a negative charge state, while the neutral charge state has ZPLs at 859.0 nm and 861.7 nm, respectively. Both defects are quite common in 4H- and 6H-SiC, as well as in 3C. The V_{Si} negative charge in 4H and 6H has a high spin (S=3/2) ground state, shown in Figure 1(c)[32]. V_{Si} ZPL emissions in 6H-SiC are known as V_1,V_2 and V_3 lines, owning to the three nonequivalent sites (h,k_1,k_2; see Figure 1) at 865 nm, 887 nm and 906 nm, respectively.

The closest pair of V_{Si} and carbon vacancy V_C, the divacancy $V_{Si}V_C$, can form during the migration of the isolated vacancies. PL arising from $V_{Si}V_C$ is attributed to its neutral charge state ($V_{Si}V_C^0$) and has several ZPLs in 4H- and 6H-SiC. In 4H-SiC, the $V_{Si}V_C$ defects possess four ZPLs (stable up to 1,500°C) associated to specific PL at 997.5 nm, 1013.6 nm, 1050.7 nm and 1053.9 nm. These ZPLs are related the axial (hh, kk) and basal (hk, kh) location in the lattice (see Figure 2). Other ZPLs in a similar wavelength range have been recently found [38] denominated PL5 (1043 nm) and PL6 (1039 nm) due to their unknown origin. In 6H-SiC, the $V_{Si}V_C$-defect-known ZPLs are at 998.7nm, 1010.9 nm, 1030 nm, 1048.7 nm and 1074.6nm. ZPLs obtained in irradiated 6H samples at 1,139 nm; 1,135 nm; 1,124 nm; 1,108 nm; and 1,093 nm were found to have quantum characteristics similar to the ($V_{Si}V_C^0$)[39] and were associated with UD2 defect, previously known in 4H- and 6H-SiC[40, 41].

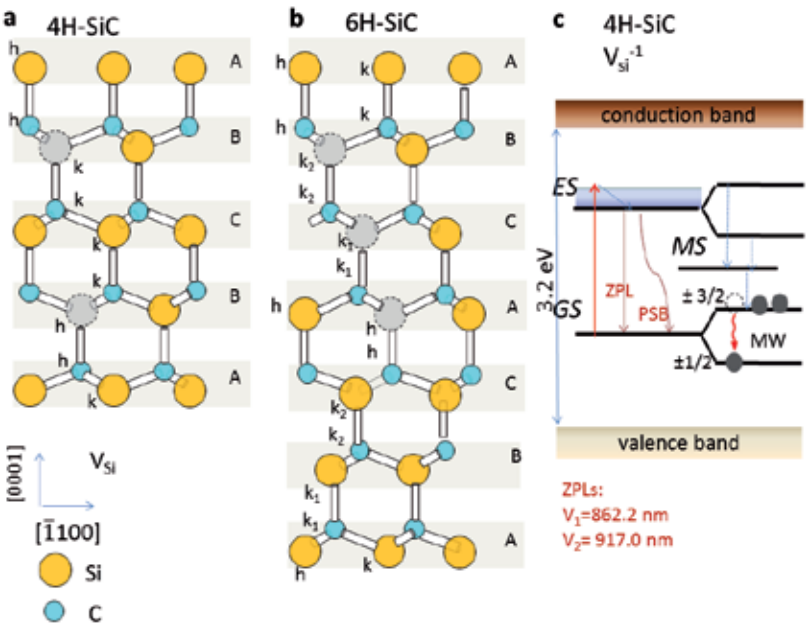

Figure 1. Representation of the atomic structure of the V_{Si} in the SiC lattice in **a** 4H and **b** 6H polytypes, located in different nonequivalent sites (k,h in 4H) and (h, k_1,k_2 in 6H). **c** Visualisation of the energy levels in the negatively charged state of the V_{Si} for 4H, where the ground state (GS), excited state (ES) and metastable state (MS) structures are visualised, with the ZPL, PSB and spin level of the high spin S=3/2 ground state. A microwave transition in the GS is responsible for the PL enhancement of the ZPL in the presence of a microwave excitation (MW). Both 4H and 6H polytypes containing these defects have been used for quantum control of the ground state spin[16, 37]

In a dual element semiconductor, the antisite-vacancy complex is an intrinsic defect. The defect possesses C_{3v} symmetry if C_{Si} is along the c-axis (on-axis configurations, $C_{Si}V_C$(kk) and $C_{Si}V_C$(hh)), while it has C_{1h} symmetry if C_{Si} is out of the c-axis (off-axis configurations, $C_{Si}V_C$(kh) and $C_{Si}V_C$(hk)) in 4H-SiC (see Figure 3**a**). Its PL was found to be in the 648-678 nm range and initially attributed to its neutral charge state[36]. It has been known as AB lines found in both 4H- and 6H-SiC with also different doping. According to recent modelling, the neutral charged state of the $C_{Si}V_C$ defect associated to the AB lines should not have any visible PL; therefore, the visible PL is attributed to the positive charge state of this defect with S=1/2. Eight ZPLs were associated with the $C_{Si}V_C$ in 4H-SiC, labelled as A_1 = 648.7 nm, A_2 =651.8 nm, A_3 = 665.1 nm, A_4=668.5 nm, B_1 = 671.7 nm, B_2 =673.0 nm, B_3 =675.2 nm and B_4 = 676.5 nm. The eight AB PL lines in 4H-SiC can naturally account for the four ground-state configurations (hh, kk, hk, kh) where each possesses two ZPLs due to the splitting of the excited state.

3. Single-photon source in bulk material

Over the past decade, single-photon generation has been observed in many physical systems such as single molecules[42], quantum dots[43, 44], diamond colour centres[45] and others[46, 47]. The generation and detection of single photons play a central role in the foundation of quantum mechanics. Additionally, an efficient and high-quality single-photon

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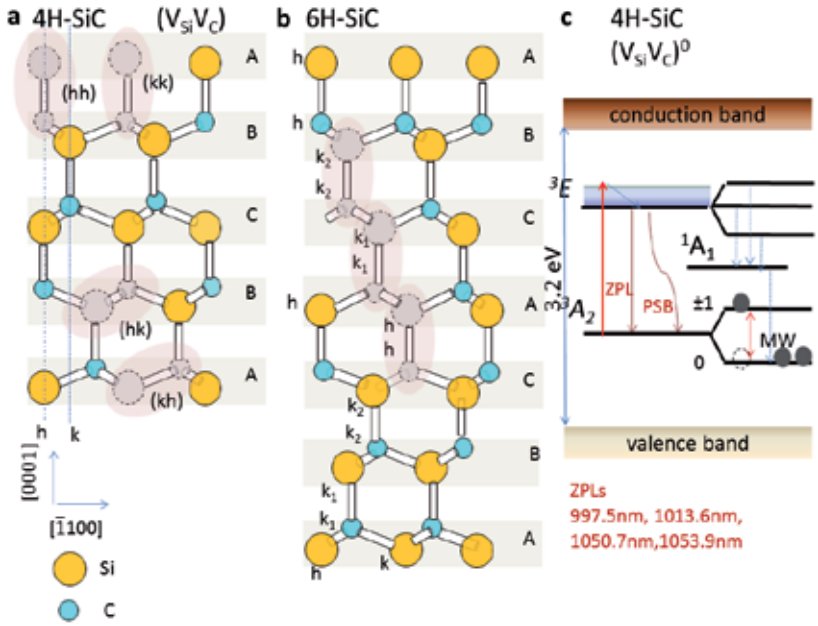

Figure 2. Representation of the atomic structure of the $V_{Si}V_C$ in the SiC lattice in **a** 4H and **b** 6H polytypes, located in different nonequivalent sites (k, h in 4H) and (h, k_1,k_2 in 6H).**c** Visualisation of the energy levels in the neutral state of the ($V_{Si}V_C^0$) for 4H, where the ground state ($^3A_2$), excited state (^3E) and metastable state ($^1A_1$) structures are visualised, with the ZPL, PBS and spin level of the high spin S=1 ground state. A microwave transition in the GS is responsible for the PL enhancement of the ZPL in presence of a microwave excitation (MW). Both 4H and 6H polytypes containing these defects have been used for quantum control of the ground state spin [15, 38, 39]

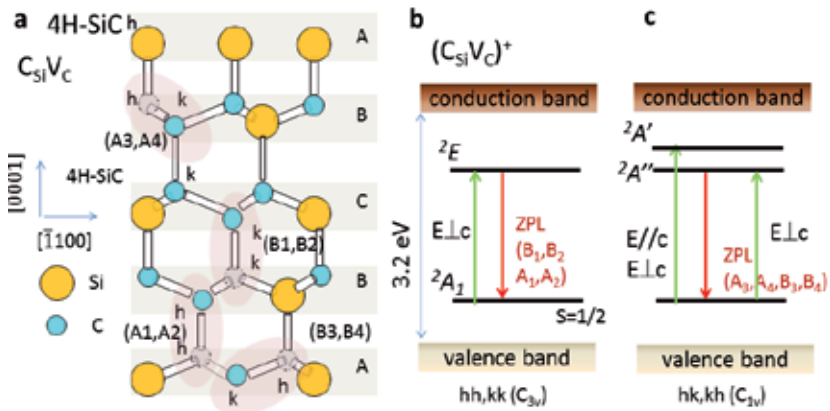

Figure 3. Representation of the atomic structure of the $C_{Si}V_C$ in the SiC lattice in **a** 4H, located in different nonequivalent sites (k, h in 4H). Visualisation of the energy levels in the positive charge state of the ($C_{Si}V_C^+$) for 4H, where the ground state ($^2A_1$) and excited state (^2E) are visualised, with the ZPLs in the axial **b** and basal **c** defects position [14]

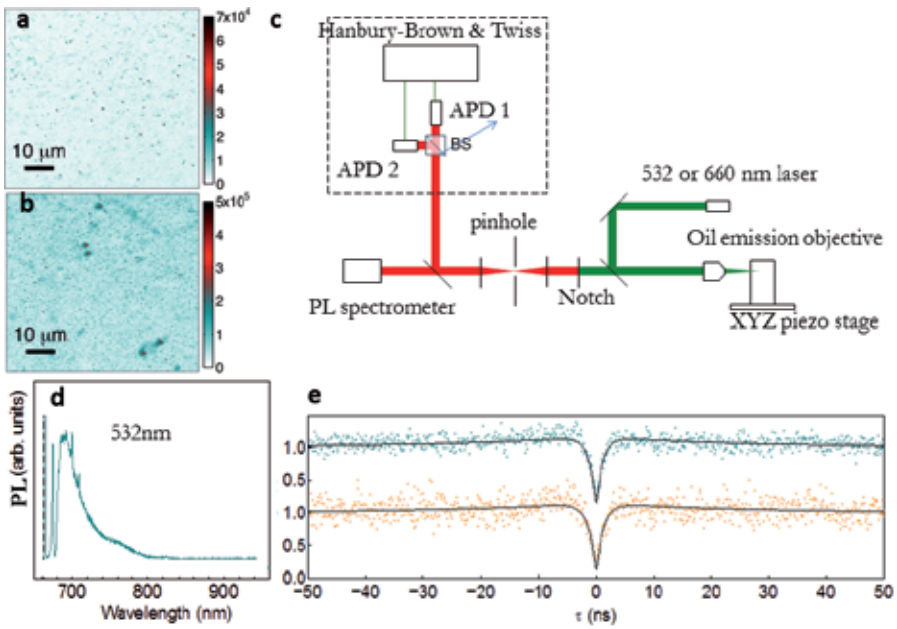

Figure 4. Confocal maps of **a** untreated sample that occasionally shows native defects whose origin is yet unclear and **b** confocal map showing irradiated generated single defects with a low temperature annealing of 300 °C. The colour code indicates much brighter emitters in the irradiated samples. **c** Experimental set-up.**d** Typical room temperature PL of the SPS. **e** Photon correlation of two SPSs in the irradiated sample excited at 532 and 660 nm. The reduction of photon coincidence at zero delay time below 0.5 indicates the presence of single-photon statistics

source operating at room temperature is needed to ensure secure communication channels via the implementation of protocols of quantum key distribution. SPSs are needed to establish quantum photonics communication networks[48]. At the present, SiC has provided in bulk materials SPS from all the defects discussed in Section 1, isolated in ultrapure 4H-SiC. The first observation of single-photon statistics from SiC was associated with the PL from a single C antisite-vacancy pair. This defect is the brightest single-photon emitter in a bulk solid state system operating at room temperature, showing up to 10^6counts/s at saturation, indicating a high quantum efficiency and occurring in the region 650-700 nm. The single-photon emission corresponds to a 3-level atomic system, due to the presence of a metastable state. The brightness is associated to the polarisation selection rules of these defects, most of the time parallel to the excitation electric field, as well as to the dipole strength (short radiative lifetime of 1.5 ns). The defect has been isolated using confocal microscopy in electron-irradiated high-purity, semi-insulating (HPSI) SiC along the main axis (1,000) from a 3-inch wafer, containing $V_C \sim 10^{14}/cm^3$, B$\sim 10^{14}/cm^3$, N and other defects$< 10^{14}/cm^3$. Electron irradiation with energy of 2Mev was used to create defects deeper in the material, and fluences of 10^{13}-$10^{14}cm^{-3}$ were used for the single-defect creation. In Figure 4, the confocal maps, experimental set-up, typical PL and photon correlation measured using a Hanbury Brown and Twiss interferometer indicate SPS. PL at room temperature in single emitters was compared to ensemble generated with electron fluences of $10^{17}cm^{-3}$, showing high similarity when excited at 532 nm.

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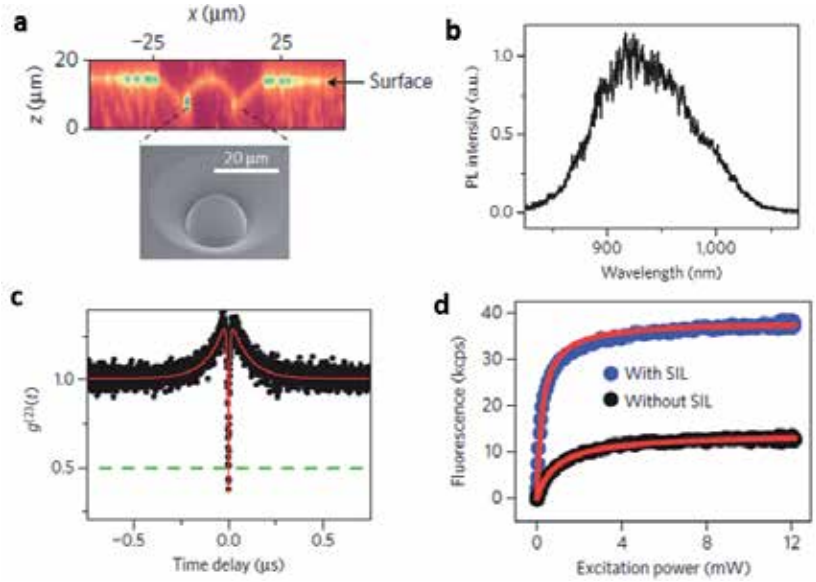

Figure 5. Confocal map of **a** a solid immersion lens (SIL) containing a single V_{Si} defect and the SIL SEM image. **b** PL at room temperature of the V_{Si}.**c** Photon correlation of defect PL in the irradiated sample. The reduction of photon coincidence at zero delay time below 0.5 indicates the presence of single-photon statistic. **d** Photon count rate from a single defect versus excitation power with and without the SIL. Images reproduced with permission from Macmillan Publishers Ltd: Nature Materials [16], copyright (2015)

V_{Si} denoted as V_2 lines with ZPL at 917 nm in bulk 4H-SiC has also been isolated [16], using confocal microscopy exciting the substrate by a 730 nm laser. The defect at the single level was created by electron irradiation and low-temperature annealing in vacuum. Due to the geometry of the defect location in the material cut along (1,000) axis, this defect could not be excited with the laser polarisation along to the defect axis, yielding a very low count rate at the single-photon level (15,000counts/s) at saturation. A solid immersion lens of 20 μm diameter was milled using a Ga focussed ion beam in the material to increase the collection efficiency of the single photons, proving an enhancement of a 2.5 factor. Similar results are shown of isolation of this defect in 4H by [17]; in this case, the defect was created using neutron irradiation, and a clear increase of the number of defects with radiation fluences was observed. Similar count rate and PL broad emission in the 900 nm region was observed for the single emitter. A lifetime of 6.1 ns was determined and perfect photo-stability was observed. In Figure 5, we show the main properties of this defect as a SPS.

Divacancies were also isolated from 120 μm 4H-SiC single-crystal epitaxial film grown on an n-type 4H-SiC substrate. The substrate was grown by hotwall chemical vapour deposition, a technique used to create commercial quality, multilayer electronic structures at the wafer scale. The epilayer is optimised to have no basal plane dislocations or polytype inclusions and a very low (5 10^{13}cm^{-3}) unintentional dopant density. The epilayer was mechanically separated from the substrate, polished and diced and then irradiated with 2 MeV electrons at a range of fluences 5 $\times 10^{12}$ cm^{-2} to 10^{15}cm^{-2}. Annealing was used to achieve the migration of the vacancy to form the defects. Superconducting nanowire-based single-photon detectors able to detect the infrared emission were integrated into a home-built confocal microscope.

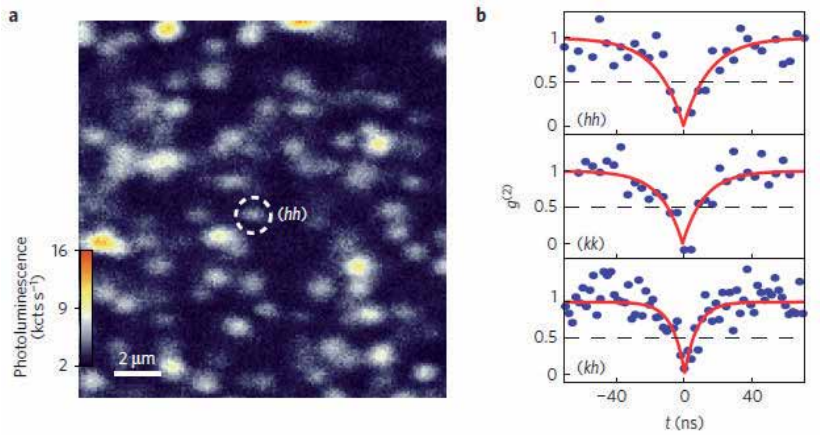

Figure 6. Confocal map of **a** a 4H-SiC membrane irradiated at 10^{13} cm^{-3} electron fluence. PL is collected by a confocal at a depth of 20 μm at a temperature of 20 K. PL spots were mostly identified as divacancies, though not all bright spots correspond to isolated single defects. **b** Photo-correlation $g^{(2)}(\tau)$ measurements for single divacancy defects located corresponding to (hh), (kk) and (kh) sites. Fits to a simple two-level model are shown. Images reproduced with permission from Macmillan Publishers Ltd: Nature Materials [15], Copyright (2015)

Excitation was performed with 975 nm continuous-wave laser. The sample was cooled to 20 K to observe distinct bright spots in a scanning PL image, as shown in Figure 6. The optical lifetimes of the neutral divacancies is 14±3 ns. The measured count rates were very low in the range of 3000-5000 counts/s, due to detector losses ($\sim$ 28% detection efficiency) in the spectral region of their ZPLs and the low collection efficiency from low NA objective in the cryostat. In addition, because of a high background due to polishing artifacts it was required to focus deep (20 μm) below the SiC surface to observe isolated single emitters, which added another 20-30% optical losses.

4. Single-photon sources in nanomaterials

SiC nanomaterial scientific interest is motivated by the material larger potentials at the nanoscale in optoelectronics as an efficient ultraviolet emitter. SiC nanomaterial has also generated interest for its biocompatibility in nanomedicine or as emitting nanoprobes for imaging[49–51]. PL spectra of SiC nanostructures and nanopowder have been largely studied. The most common PL origin due to subgap emission is radiative recombination of defects and surface states[52], while above-gap emission is attributed to quantum confinement phenomenon in small nanocrystals such as quantum dots (QDs). At present the peak emission wavelengths of the SiC QDs are in the UV-blue-green region, typically between 380 nm and 550 nm[53–56]. This spectral emission region, however, is not ideal for biomedical applications due to the cell autofluorescence in the same spectral band. Additionally, infrared would be desirable for in-depth biological tissue imaging.

Recently the first demonstration of a deep defect within the bandgap has been shown in SiC nanocrystals obtained from 3C polytype[18], showing an emission in the red spectral region (650 nm). This red emission has been demonstrated to emit single photons. Two sources of SiC nanoparticles were explored: commercial 3C SiC nanomaterial with an average

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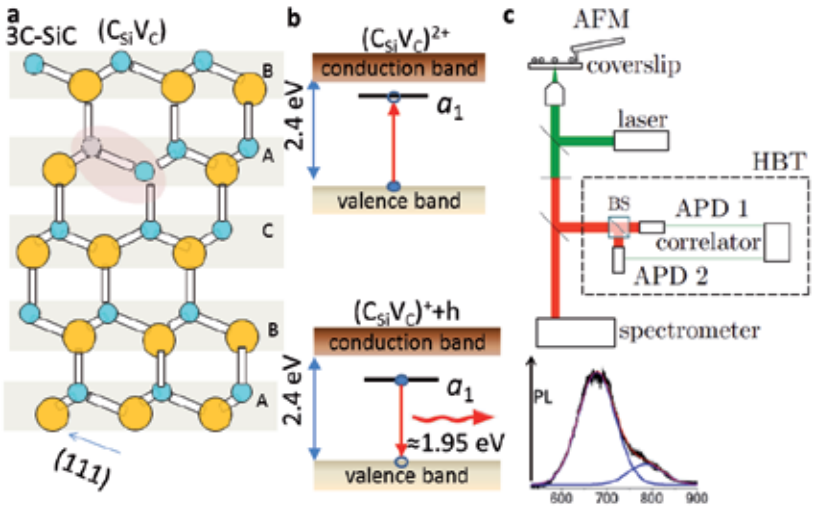

Figure 7. Representation of the atomic structure of the $C_{Si}V_C$ in the 3C-SiC lattice in **a**. **b** Visualisation of the energy levels in the double-positive charge state of the ($C_{Si}V_C^{2+}$) for 3C, where the ground state and excited state are visualised. The defect ZPL is around 648 nm from ensemble measurements (not clearly observed at the single level at room temperature).**c** Experimental set-up used to study the 3C-SiC nanoparticle defect SPS and room temperature PL measured from SPS [18]

size of 45 nm suspended in ethanol and large (size: 200-500nm) in-house synthesised SiC nanocrystals suspended in MilliQ, dried on glass cover slip[57]. A room temperature custom-built confocal microscope combined with an atomic force microscope (Figure 7**c**) was used to correlate the size of the nanocrystals with PL, while photon correlation was used to determine the quantum properties of the PL. Low-temperature Raman spectroscopy and cathodoluminescence were used to aid the study of the origin of the SPS PL in 3C nanocrystals, indicating that the PL was not due to surface defects. A distinctive ZPL was observed at 648 nm at 80 K from ensemble measurements. A CW laser pump at 532 nm was used to excite the samples, while a pulsed 532 nm laser was used to measure the fluorescence lifetime, which results in the range of $(2 \div 5.3) \pm 0.2$ ns, depending on the treatment. Some nanocrystals provided SPSs with partial polarisation in absorption and emission. We tentatively attributed the defect responsible for SPS in 3C to the carbon antisite-vacancy pair by comparing to ensemble low-temperature PL in bulk 3C heavily irradiated sample. This defect has C_{3v} symmetry in 3C-SiC lattice (see Figure 7**a**). Because of the relatively small bandgap of 3C-SiC, the double-positive charge state was considered as possible candidates for the PL. The calculated $(2+ \mapsto +)$ charge transition level is at 1.95 eV which is very close to the ZPL energy of the bulk material defect ZPL.

SPS has also been observed in SiC nanotetrapods[19]. The tetrapod crystal phase structure consists of 3C core and 4H arms. The coexistence of 3C and 4H polytypes in these nanostructures led first to the observation of PL in the spectral region between 650 and 780 nm, not observed before in SiC nanostructures. This has been understood as a new quantum confined system accessible at room temperature. In this case, the quantum confinement and the nonclassical emission originated from the homogeneous heterostructure of 3C core and 4H legs, forming a quantum well in SiC nanotetrapod. The schematic of the SiC tetrapods

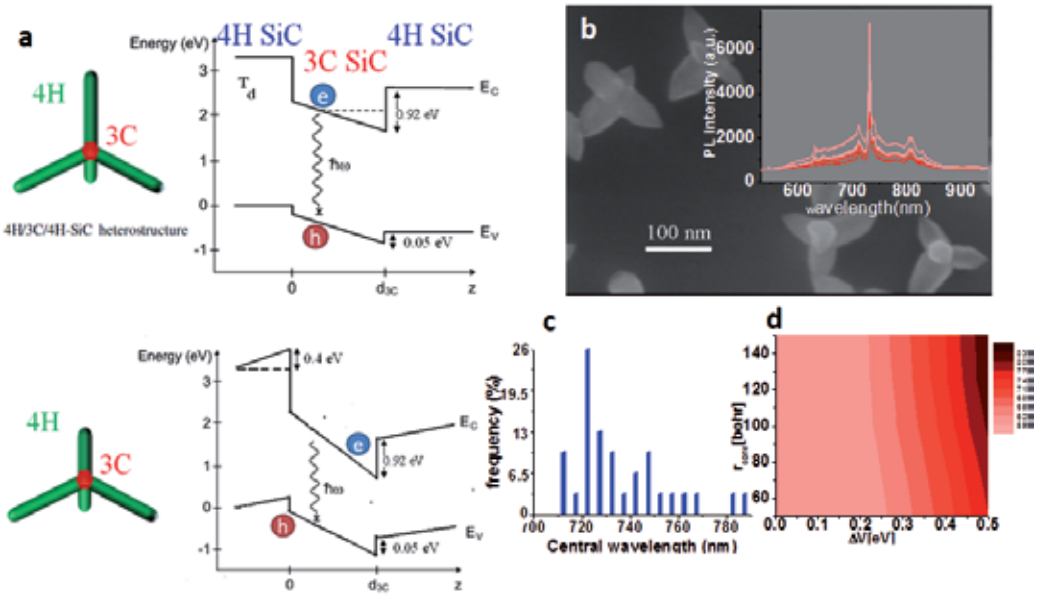

Figure 8. **a** Schematics of the tetrapod structure where the diameter of 3C core is d_{3C}. Top: Band line-up for 4H/3C/4H-SiC heterostructures for the ideal symmetry case T_d. Bottom: Quantum confinement model of SiC tetrapods when an asymmetric structure is considered and a polarisation potential change on both legs is ΔV=0.4 eV. **b** Scanning electron microscope of grown tetrapods. Every tetrapod has an average leg length of $\sim$ 100 nm. Inset: exemplary PL form a single tetrapod corresponding to an SPS.**c** Measured ZPL central emission for SPS in single nanotetrapods. **d** Calculated emission wavelengths from this model where ΔV is the potential difference along the arms and r_{core} is the radius of the 3C core, respectively. The steep potential curve with a height of ΔV arises from the different lengths of the 4H-SiC legs of a tetrapod[19]

is shown in Figure 8, accompanied by a high-resolution scanning electron microscope (SEM) image of the tetrapods. The nanotetrapods were measured to have an average leg length of 100 nm and leg diameter smaller than 50 nm, while the core was estimated as small as several nanometres. The possible band structure in SiC tetrapods is analysed by means of quantum mechanical simulations on a simplified model. The exciton is confined along the quasi one-dimensional potential curve created by 4H(leg)- 3C(core)- 4H(leg) structure. The emission wavelength of the individual tetrapods depends on their geometry, particularly, on their global symmetry, and much less on the diameter of 3C core (Figure 8 **c**). If the length of 4H legs was the same for all tetrapods (global T_d symmetry), then a classical rectangular quantum well forms for the electrons in the conduction band (0.92 eV) and a minor potential barrier for the holes in the valence band (0.05 eV), so that the potential curve does not show any steepness (ΔV = 0) (Figure 8 **a** (top)). The symmetric tetrapods should show no polarisation of light. However, if the length of the 4H legs was different (i.e. not all the legs have the same length) in a SiC tetrapod, then this induces different polarisations of surface charges at the end of 4H legs in these tetrapods, so a steep potential curve ($\Delta V > 0$) both for the electrons and holes in the conduction and valence band edges (Figure 8 **a**(bottom)). This effect creates a triangular potential well for the electron in the conduction band and starts to push the hole away from 3C region.

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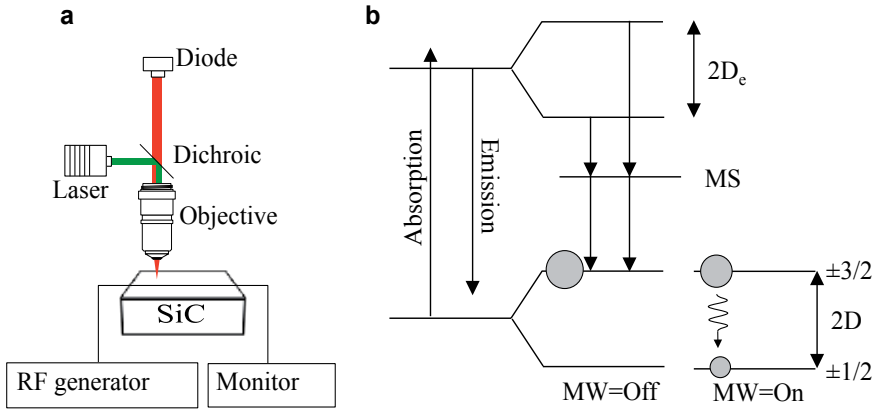

Figure 9. a Schematic of the optical set-up used to measure the ODMR signal. **b** Energy-level diagram of a spin system with a quartet ground state based on the V_{Si} [16, 37]. D and D_e denote the zero-field splitting of the ground singlet state and the excited state, respectively. The population of the spin substate levels is indicated by the grey circles. Further details in the text

5. Optical control of spin state

Spin-dependent luminescence can be used to study magnetic and hyperfine parameters for excited states of defects in SiC. A wealth of knowledge about the atomic origin of defects and their properties has been extracted from such optical measurements. More recently, with the emergence of quantum information processing technologies, optical methods have been developed to coherently control and read out the spin of a defect centre. Figure 9**a** shows a schematic of a basic set-up often used to measure spin-dependent luminescence in SiC by the optically detected magnetic resonance (ODMR) technique. The main components are the excitation laser, a dichroic mirror and a diode to collect the filtered light in the spectral region of interest. A microwave carrying wire lays in close proximity to the probed defects, and an external magnetic field may also be applied. The electron paramagnetic resonance (EPR) spectrum is recorded by monitoring the PL intensity, while the frequency of the applied microwave excitation is varied. Figure 9 **b** shows an example of an energy-level scheme for a defect (based on the V_{Si} [16, 37]). Firstly, the defect is optically excited. In this system, intersystem crossing (MS) causes the higher-lying spin sublevel of the ground state ($m_s = \pm 3/2$) to be preferentially populated. When resonance with an allowed EPR transition occurs on the application of a microwave field, such as $|m_s = \pm 3/2\rangle \rightarrow |m_s = \pm 1/2\rangle$, the steady-state population of the sublevels is redistributed. This leads to an enhanced singlet ground-state absorption and an increase in the PL intensity. Decreases in PL can also be observed depending on the relative values of the populating and decay rates. ODMR has only been observed for a limited number of systems, most notably for single NV centres in diamond [58] and more recently single V_{Si} [16] and $V_{Si}V_C$ [15] centres in SiC which will be discussed further below. Optically induced alignment (polarisation) of the ground-state spin sublevels of the V_{Si} in 4H- and 6H-SiC was observed recently for the first time at room temperature [59, 60]. The alignment schemes vary depending on the crystal polytype and crystallographic position of V_{Si} in the crystal lattice, as well as their zero-field splitting parameters. For 6H-SiC, the zero-field splitting parameter of V_{Si} is 9×10^{-4} cm^{-1} (26.9 MHz for the k-site) and 42.8×10^{-4} cm^{-1} (128.3 MHz for the h-site), while for 4H, it was found

to be 22×10^{-4} cm^{-1} (65.9 MHz for the *h*-site). The spin states of the UD-2 lines have recently been optically addressed and coherently controlled [38, 39]. In this work, with the four UD-2 lines labelled as PL1-PL4, the spin-1 ground state of each line was investigated as well as a pair of defect spin states of unidentified origin (PL5 and PL6). Room temperature Hahn echo measurements of these latter two defects was demonstrated with T_2^* times of 214 ns and 1248 ns, respectively, similar to the V_{Si} defect. The spin coherence times were found to be comparable to those of the NV in diamond[61]. Such measurements have been performed in 3C, 4H and 6H polytypes with defects existing in the as-grown material or those formed by ion implantation [39]. The UD-2 family of PL lines in 6H-SiC also show ODMR signals and are labelled QL1-QL6. The QL1 line is associated with a spin system with a zero-field splitting of 1.299 GHz. In contrast to conventional EPR where the transverse magnetisation of a large spin ensemble is detected, ODMR can have single spin sensitivity due to linking weakly allowed magnetic dipole transitions to highly allowed electric dipole emission processes. Optically addressing and coherently controlling the spin state of single defect is a potential basis for quantum information and nanoscale sensing applications. This has recently been demonstrated [15, 16] by using a range of pulsed ODMR techniques. Many of the detection and pulse sequences developed for EPR can be applied to ODMR experiments with minor modifications. Such measurements have allowed unprecedented insight into the spin of defects at the ensemble concentration level and now to the single-defect level. Figure 10 shows two ODMR modes of operation as applied to a single V_{Si} defect in SiC [16]. For this centre, spin transitions between ground state sublevels are induced by the microwave excitation giving rise to an enhancement of the PL intensity (Figure 10a and b). The line width is 6 MHz and is limited by the inhomogeneous spin coherence time T_2^* with laser and microwave power broadening effects superimposed. Pulsed methods can be used to circumvent this. Figure 10c shows a simple sequence of pulses that can be used to measure the Rabi oscillations, the characteristic signature of a coherent system interacting with an electromagnetic field. Oscillations reflect the behaviour of a population of an excited state as a function of the input pulse area or qubit rotations. The microwave frequency is set to resonance and the oscillation period is proportional to the microwave field strength. The largest Rabi frequency measured was 8.4 MHz ($B_1 = 0.16$ mT), corresponding to a $\pi/2$ rotation in about 30 ns. Interactions of the spin system with its environment cause a relaxation of polarisation and coherence and are characterised by two time constants, the longitudinal time T_1 (spin-lattice relaxation time) and the transverse relaxation time T_2 (spin-spin relaxation time). Long spin coherence is essential for quantum information and sensing applications. Using a Hahn-echo pulse sequence ($\pi/2 - \tau - \pi - \tau' -$projection), Widmann *et al.* placed a lower bound to the spin coherence time of 160 μs and an upper bound of 1 ms, limited by the spin relaxation time. The accuracy was limited by modulations in the signals possibly due to hyperfine coupling to a ^{29}Si nuclear spin close by. These long coherence times collected at room temperature are an indication that SiC is a promising platform for quantum technologies. The main issues are the weak PL intensities (40 kcts/s when integrated with a solid immersion lens) and the poor ODMR contrast ($< 1\%$). Christle et al.[15] report the coherent control of the electronic spin of individual neutral divacancies with emission in the NIR compatible with telecommunication wavelengths. At a temperature of 20 K, a coherence time of 1.2 ms was obtained. The inhomogeneous spin dephasing time, T_2^*, measured by a Ramsey pulse sequence, $\pi/2 - \tau - \pi/2$, was found to be up to 4.4 μs. These were longer than that observed earlier for ensembles [38]. A spin coherence time of 1.2 ms was also deduced for a spin ensemble rather than on a single-defect level owing to

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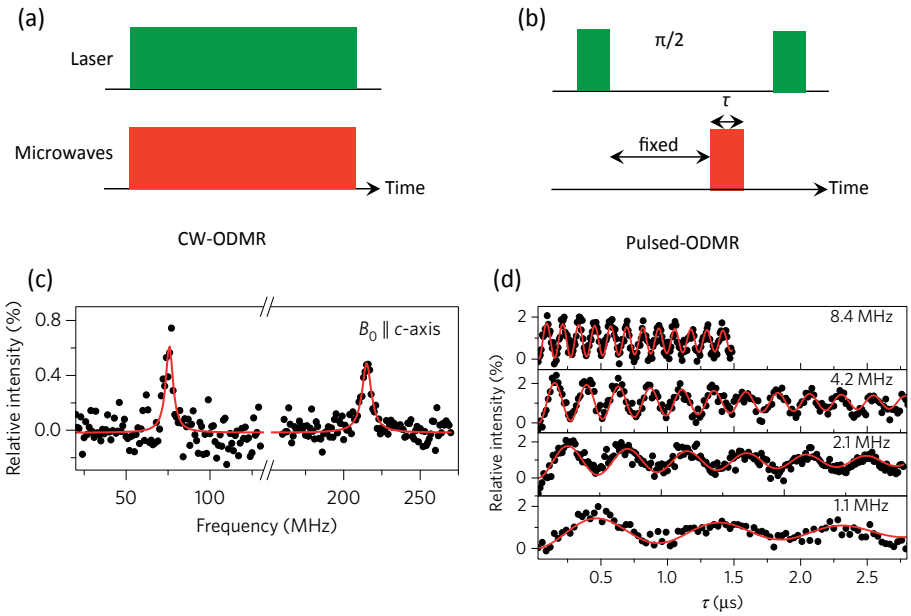

Figure 10. **a** Schematic of the continuous wave ODMR method with the microwave frequency varied while the PL is measured. **b** Pulse sequence used to detect spin Rabi oscillations. **b** ODMR spectrum of the V_{Si} in a magnetic field of 50 G parallel to the c-axis. **d** Spin Rabi oscillations of the $|m_s = +3/2\rangle \rightarrow |m_s = +1/2\rangle$ transition of a single V_{Si} for various field strengths B_1. **c** and **d** reprinted by permission from Macmillan Publishers Ltd: Nature Materials 14, 164, copyright (2015)[16]

limitations in their photon collection efficiency. This duration is remarkably long and much greater than that found for the NV centre in isotropically pure diamond [61]. In addition, still greater spin coherence times might be achieved if the SiC is also isotropically purified [62]. This result may be counterintuitive since the natural abundance of ^{29}Si is greater than ^{13}C. Theoretical calculations attribute this phenomenon to three factors: the longer bond length in SiC, the smaller gyromagnetic ratio of ^{29}Si and the suppression of heteronuclear spin pair flip-flop processes in the strong magnetic field regime [63]. Long-lived spin coherence is essential to implement quantum information and sensing technologies; in SiC, it seems to be a common feature of the spins in all three polytypes. Single-spin coherent control has been achieved for both the V_{Si} and $V_{Si}V_C$ centres. Although the NV centre in diamond dominates this field, SiC shows some advantages being compatible with standard device processing protocols, available in high-quality 3-inch wafers and available in a wide range of polytypes. SiC-based devices in which single spins act as the active device element may be employed in emerging quantum technologies.

6. Photonics nanocavities and micro-cavities

Spontaneous emission from an SPS can be enhanced if the defect or an equivalent 2-level system is placed inside a cavity. The magnitude of the enhancement depends on the coupling (g) between the cavity and the atom's emission modes. The enhancement of the spontaneous emission of a dipole in a cavity is the Purcell factor, given by $F =$

$3/4\pi^2 Q/V(\lambda/n)^3$, where the quality factor $Q = 2\pi\nu_c/k$ is related to the cavity resonance frequency ν_c and the cavity field decay rate k, while V is the mode volume of the cavity. Nanophotonics is recently an expanding area for quantum technologies as it can provide a strong confinement of photons in a tiny space and potential applications such as ultrasmall and integrated photonic chips, slowing and stopping lights, quantum information processing and environmental sensing. Quantum emitters in bulk materials have inherently poor directional emission, prohibiting high collection and coupling efficiencies to fibre networks for long-range communication. One approach is to utilise cavities to enhance coupling to a specific optical mode. Using a photonic-crystal waveguide yields extraordinarily high coupling efficiencies. Similarly, optical microresonators offer the possibility to increase the coupling of quantum emission with the cavity mode. SiC-based nanophotonics is recently an expanding area as it could further improve present technologies based on Si or GaAs. One reason is due to the suppression of two-photon absorption at high input powers, because of its larger bandgap. Additionally, SiC can provide broadband operation, even in the visible range. The ability to construct nanocavities and optical microdiscs in SiC will possibly allow relevant technological advance in room temperature SPSs based on SiC defects and the coupling of multi-emitters to reach strong coupling regime. The main nanofabrication advantage available in SiC is based on its routinely achievable p- and n-doped in different polytypes and in its possibility to be grown epitaxially on a sacrificial silicon substrate; these features allow dopant-selective photoelectrochemical etching[64, 65] and more amenable application of reactive ion etching procedures to nano-fabricate photonics or micro-mechanical structures[21].

6.1. SiC photonics cavities

SiC 2D-photonic nanocavity crystals were initially fabricated on thin SiC-on-insulator wafers, which were specially prepared using the smart-cut technique[66]. The main challenge for 4H and 6H is related to the fact that SiC is much harder than silicon, and therefore, the important challenges here are the preparation of SiC membrane structure and the etching of SiC material as the conventional plasma etching technique for Si cannot be used. The wafers consisted of a SiC (6H crystalline structure) surface layer with a thickness of 180 nm above an SiO_2 layer (680 nm), on top of a Si substrate (300 nm) that was used for handling. Quality factors up to 1,300 were achieved with such crystals, and their resonance tuning from the visible to the infrared can allow the selective enhancement of the SiC SPSs[12]. The PCh cavities were L3 nanocavities with three missing air holes. Designs and realisation based on schematics of air hole-shifted and heterostructured nanocavities[67] showed higher Q factors of 6×10^3 and up to 5×10^5, demonstrating that the design concepts previously used in Si can be applied to the SiC hexagonal polytypes. Regardless these were the first attempts, these PCh nanocavities showed so far the highest Q (see Figure 11). More recently 3C-SiC polytype is used for better integration with Si photonics, by heteroepitaxial growth on sacrificial Si substrate, allowing for direct patterning without ion implantation damage. With this method, an L3 PhC cavity has been fabricated in a thin-film (200 nm) 3C-SiC slab, obtaining Q-factor of 1,000 and modal volume of $0.75(\lambda/n)^3$ over the band between 1250 and 1600 nm in the telecom IR range[22]. The possibility to incorporate colour centres with optically addressable spins similar to NV centres in diamond has been shown by fabricating H1 and L3 PhC cavities in 300-nm-thick 3C-SiC, as shown in Figure 12, with experimental Q of 1,000 for the strongly coupled cavity and $(\lambda/n)^3$ mode volume, tuned to the zero phonon line of the Ky5 colour

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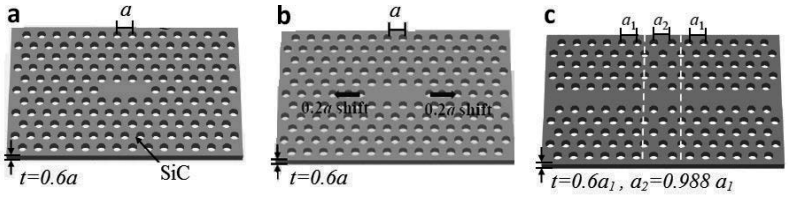

Figure 11. Schematics of **a** SiC-based (L3) nanocavity with three missing air holes and a $Q \approx 1200$; **b** air hole-shifted $Q \approx 6000$ and A**c** heterostructured PCh nanocavity with higher Q obtained in 6H polytype, $Q \approx 500000$. a is the cavity lattice constant related to the holes radius that for NIR range of 1380÷1590 nm is a = 550 nm[11]. Lattice constant as small as a=150 nm was achieved for resonance frequencies at 550-600 nm. Image adapted from ref[11]

centre (emission band 1,100 to 1,300 nm at 20 K), enhancing PL collection up to 10 times[23]. PhC structures made by a square or hexagonal lattice of SiC rods in air have also been proposed for telecom band applications[28], resulting in the confinement of the cavity mode in air, with the aim of reducing modal dispersion and temperature sensitivity. Theoretical modelling of a defect A1 cavity in SiC hexagonal lattice (photonic bandgap, PBG, from 1,380 to 1,850 nm) showed a thermal shift of the cavity TE mode seven times smaller as compared to a Si-based lattice with similar PBG, for a temperature range between 25 and 200 °C, with a maximum Q of 224. The highest Q reported to date of 7.69×10^4 has been achieved using a 45-μm-long 1D PhC nanobeam cavity at 1.5 μm wavelength [29]. It was fabricated on a 280-nm-thick amorphous SiC (a-SiC) film, deposited on an Si substrate by plasma-enhanced chemical vapour deposition (PECVD) in a gas mixture of silane and methane and patterned by e-beam lithography and reactive-ion etching with CF_4/O_2 plasma. The nanobeam was released in KOH with subsequent critical point drying.

6.2. SiC microresonators

High-Q optical microresonators can also dramatically enhance optical fields inside a small volume and are considered relevant in applications to enhance nonlinear optics effects and their implication to quantum optics. In addition, they are important in fields such as cavity optomechanics[68, 69]. In general for microresonators, the materials play a crucial role based on its properties such as linear/nonlinear optical susceptibilities and mechanical property. High-Q microresonators generally exhibit large thermal and mechanical sensitivities, making them desired for practical application. Microresonators are commonly fabricated in disc shapes resting on a central pedestal; however, recently suspended ring resonators have been proposed in order to obtain better waveguide dispersion engineering properties for nonlinear processes[20]. Some materials, such as Si and GaAs, have small bandgaps that limit the operating spectral range. Others, such as lithium niobate and chalcogenide glass, exhibit photorefractive effect or two-photon absorption and strong Raman scattering, making it challenging to handle high optical powers. For microphotonic/nanophotonic applications, it is crucial to search for a material platform with combined superior optical, mechanical and thermal properties. SiC seems to match some of these requirements for an optimal microresonator performance. Since strong coupling between a point defect optical source and the resonant cavity is challenging, due to having to place the defect at the field maximum of the cavity mode, a disc resonator in this respect has the good feature of supporting multiple modes, which cover almost the whole volume of the disc, making overlapping and tuning to

the zero phonon line of the defect easier[26]. The single-crystalline 3C-SiC in Lu et al.[21] was epitaxially grown on a (100) silicon substrate by the two-step atmospheric pressure chemical vapour deposition. A disc geometry was patterned by electron-beam lithography and etched by reactive ion etching with CF_4/Ar plasma, optimised to form the well-defined device structure. The silicon substrate was undercut by XeF_2 to form the supporting pedestal. The intrinsic Q factor is shown to be 6.19×10^3. The damage to the crystal incurred during ion etching can impair the optical efficiency and the spin coherence of the defect sources, so an alternative is sought by low-damage selective chemical etch processes, such as photoelectrochemical etching, exploiting the higher etch rate of n-doped to p-doped material under direct UV illumination in HF or KOH solutions[24]. Epitaxial p-doped SiC on n^+-SiC was patterned by reactive-ion etching (RIE) in SF_6/O_2 plasma using 3 μm alumina microspheres as masking agents; then the p-layer was undercut by KOH etching under UV illumination. Well-undercut microdiscs reached a measured Q-factor of 9,200 at 617.4 nm resonance, with a theoretical maximum of 10^5, limited by light leakage into the supporting pillar. The issue of light loss in the supporting Si substrate was addressed by exploiting the high stiffness of an 860-nm-thick 3C-SiC layer, building a 20 μm radius ring microresonator suspended in air from a central pedestal by 200-nm-wide spokes and by e-beam lithography followed by CHF_3/O_2 RIE[20]. An intrinsic Q factor of 14,100 was measured at 1,543 nm wavelength. PL from 3C-SiC in the visible range was first demonstrated for multi-emitter cavity quantum electrodynamics at room temperature in disc microresonators of 210 nm thickness and diameter below 2 μm, fabricated by two-step chemical vapour deposition (CVD) followed by e-beam patterning, HBr/Cl_2 plasma etching and XeF_2 undercut to form the pedestal[30]. Characterisation by laser scanning confocal microscopy between 650 and 850 nm wavelength evidenced whispering gallery modes with Q-factor up to 2,300 and mode volume around $2 \times (\lambda/n)^3$. The highest Q-factor reported to date for a disc microresonator is 5.12×10^4, obtained at 1,551 nm wavelength with e-beam-patterned heteroepitaxial 3C-SiC on Si, ion etched in CF_4/Ar plasma with subsequent KOH undercut[26]. The resulting disc had a thickness of 700 nm and a radius of 6.25 μm, and simulations showed a strong coupling regime with a cooperativity C=20 and a maximum theoretical radiation-limited Q-factor above 10^8.

6.3. Nonlinear effects

SiC is a non-centrosymmetric material, which means that it has nonzero second-order susceptibility, permitting the observation of nonlinear effects such as second-harmonic generation (SHG), and Pockels effect, which are not available in the more common centrosymmetric materials (SiO_2, SiN_x and others whose molecule's symmetry allows only third-order susceptibility). Differently from other non-centrosymmetric semiconductors and crystals such as $LiNbO_3$, SiC has the ability to house optically active defects for quantum processing. Nonlinear effects in this material combined with colour centres have the potential to increase the applications in other fields such as nonlinear photonic, including all-optical switching, wavelength conversion and harmonic generation. These effects are important for the development of quantum devices based on nonlinear effects[70]. SiC second order, $\chi^{(2)}_{i,j,k}$, and electro-optical $r_{i,j,k}$ coefficients were predicted from ab initio calculations in 3C, 4H and 6H [71] and measured [72–75] in 4H and 6H polytypes. Second-order nonlinear optical coefficients are at the core of the physics of nonlinear optical processes; their knowledge and high values are essential to increase the efficiency of frequency conversion. Hexagonal SiC is

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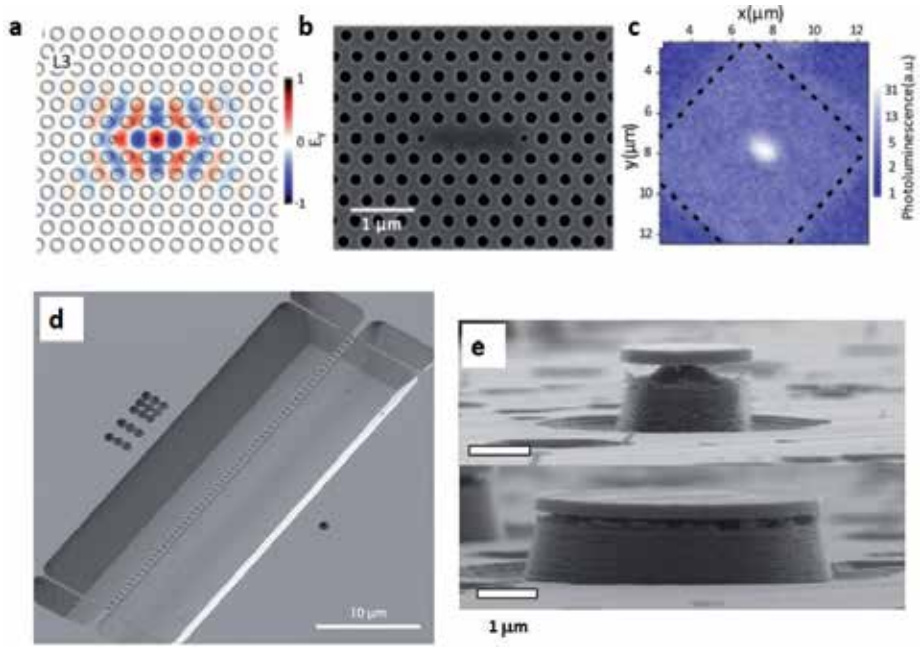

Figure 12. **a** Simulated E_y field distribution, **b** SEM image and **c** PL at 20K from an L3 photonic-crystal cavity in 3C-SiC. The cavity resonance is tuned by size reduction and shift of the neighbouring crystal holes, for 1,060 nm excitation of the embedded Ky5 colour centre[23]. **d** SEM image of a fabricated a-SiC 45-μm-long PhC nanobeam cavity, achieving the highest Purcell factor reported of 10^4 at 1.5 μm wavelength[29]. **e** SEM micrographs of high-Q disc resonators obtained by low-damage photoelectrochemical selective etching of p-SiC over n^+-SiC. Notice the different undercuts achieved by wet etching and the surface porosity of the supporting pillar, which does not affect the etched microdisc[24]. Images reproduced from [23, 24, 29] with Copyright permission 2014-2015, AIP Publishing LLC

characterised by three independent components of the second-order nonlinear optical tensor, recently measured accurately as $d_{31} = d_{32} = 6.7(6.5)\text{pm/V}$, $d_{15} = d_{24} = 6.5(6.7)\text{pm/V}$ and $d_{33} = -12.5(-11.7)\text{pm/V}$ in 6H (4H). The refractive indices and the birefringence are used to determine if phase matching can be realised; they have been remeasured from the visible to the mid-infrared region, and Sellmeier equations for ordinary and extraordinary refractive index in 4H and 6H have been provided[76]. This has led to mid-infrared region laser output tunable from 3.90 to 5.60 μm by phase-matched difference frequency generation in 4H-SiC. In this case, the material can withstand high power and for laser higher outputs in this spectral region. For applications, it is important to enhance SHG in photonics cavities. The first demonstration of SHG in SiC-based nanophotonic structures used a 6H-SiC PhC cavity tuned to 1560 nm with a Q of 10,000, taking advantage of the high refractive index of SiC (2.5) to increase confinement and of the large electronic bandgap (3.0 eV) to extend the operating bandwidth from IR to visible and to suppress two-photon absorption. A conversion efficiency of 2.59×10^{-5} was obtained for 0.17 mW average input power[25]. A high-Q amorphous SiC disc microresonator has been demonstrated for nonlinear applications, with an optical Q of 1.3×10^5 in the 1,550 nm telecom band[27]. With PECVD deposition followed by e-beam patterning and plasma etching, a smooth-sidewall disc with 570 nm thickness and 6 μm radius was fabricated, and its Kerr nonlinearity was characterised with a pump-probe self-/cross-phase modulation scheme using two high-Q

whispering-gallery modes. The resonator was pumped at 1545 nm with sinusoidally modulated light, transferring the modulation on the refractive index due to optical Kerr effect, which was then measured by a weak probe signal coupled at 1,498 nm. This gave a nonlinear coefficient $n_2 = 5.9 \times 10^{-15}$ cm^2/W, higher than any other material in use to generate frequency combs. Recently, SHG microscopy was used as a non-invasive method for imaging and identification of structural defects such as polytype inclusions and stacking faults in SiC epilayers, grown on hexagonal SiC by the vapour-liquid-solid techniques. This technique is competitive with destructive sample preparation and severely limited area of analysis to tens of microns associated instead with high-resolution TEM. By combining the SHG-based imaging with X-ray diffraction and SHG rotational anisotropy, the growth of 3C polytype on the 4H-SiC substrate was confirmed, and the polytype of the imaged defects was identified[77].

7. Other applications

Paramagnetic defects in SiC have been integrated into some devices as a proof of principle demonstration of their electrical control or of their ability to sense changes in strain, magnetic field and temperature. The discovery of single-photon emission and its engineering and isolating single defects with proper transition energy on demand can open a route for an efficient electrical single-photon source, particularly in the IR region, due to the described subgap defects. To fabricate devices, standard semiconductor manufacturing technology in combination with high-energy electron irradiation of the material can allow, for instance, the construction of LEDs with radiative recombination occurring at irradiation-induced intrinsic defects. Such LEDs have been demonstrated with two strong PL emission bands in the visible and near infrared (NIR), associated with two different intrinsic defects, one being the Si vacancy[78]. Selective manipulation of individual defect spin can be achieved. The spin separation required to achieve strong dipolar coupling between spins is of the order of tens of nanometres. Electric fields can be confined on similar length scales; therefore, electrically driven spin resonance methods can be used to manipulate the defect spin state[79]. Divacancy defects in 4H- and 6H-SiC possess a spin-dependent optical cycle, which allows non-resonant laser illumination to polarise first and then read out its ground-state spin. Since the defect PL depends on whether its spin state is $m_s = 0$ or $m_s = \pm 1$, it is possible to control the defect spin dynamics by the measuring differential PL (ΔI_{PL}) between an initial state and one that has been evolved by applying a magnetic or electric field pulses. These ΔI_{PL} measurements, in addition to enabling conventional (magnetically driven) ODMR, can also be used for electrically driven ODMR (EODMR). In Figure 13, we show the electrical control of the QL1 (unknown yet) defect in 6H-SiC with similar spin properties of the neutral divacancies, with ZPL at 1.088 eV and ODMR at 1.3GHz[39]. Ac electric fields are used to drive the Rabi oscillations across a magnetic-dipole forbidden spin transition ($m_s = \pm 2$) of the optically addressable electronic spin. A flow cryostat cools the device illustrated in Figure 13**b** to 20 K, and a permanent magnet is used to provide a static magnetic field parallel to the defect magnetic dipole. QL1 colour centres were produced in 6H-SiC substrates via a carbon implantation and annealing process introducing defects immediately below the surface. The spins were localised within a 400-nm-thick layer immediately beneath the 6H-SiC surface and were optically pumped with a 976 nm laser addressing 10^4 defects in the optical excitation volume. We show in Figures 13 **c** and **d** the effect observed from the application of an electric field via the electrode to the transition corresponding to the

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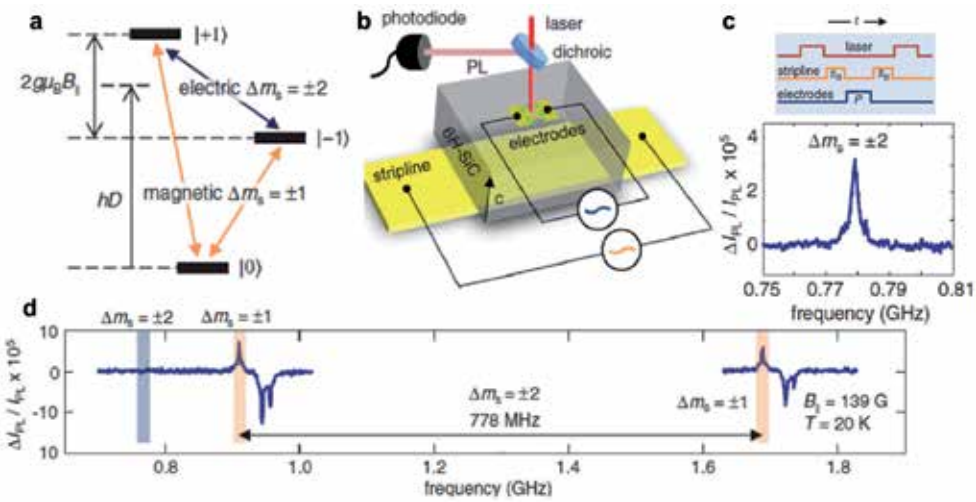

Figure 13. **a** The ground state spin structure of QL1 defect in 6H-SiC, where the spin levels $m_s = 0, \pm 1$ are shown in the presence of a magnetic field $B_{\|}$. The allowed optical transition $m_s = \pm 1$ are in orange, while the $m_s = \pm 2$ in blue are not allowed. **b** Experimental set-up used for PL collection via a dichroic mirror and measured with a photodiode. The spins are driven electrically by the electrodes and magnetically by the stripline directly on the bulk material.**c** A clear EODMR feature is observed at the frequency difference (778 MHz) of the $m_s = |+1\rangle$ and $m_s = |-1\rangle$, indicating population transfer across the two levels. On the top of the panel, the time sequence of the microwave pulse and the electric field are applied to achieve EODMR. The length of P is fixed and its frequency is swept. The electrode power was 0.09 W and the magnetic $B_{\|}$=139 G.**d** ODMR signal when the stripline is driven at $B_{\|}$=139 G. The $m_s = \pm 1$ resonances are shaded orange, and the $m_s = \pm 2$ resonance (at 778 MHz, shaded blue) is not seen in ODMR only. Images reproduced from [79] with Copyright permission 2014 American Physical Society

prohibited optical transition. Another PL resonance appears in the presence of the $m_s = \pm 2$ transition indicating a population transfer between the two-spin states.

Falk et al.[80] state that the spin states of neutral divacancies in 4H-SiC are highly sensitive to electrical and mechanical perturbations of material. The experiments were done in high-purity semi-insulating 4H-SiC wafers, purchased from Cree Inc., where neutral divacancies were incorporated during crystal growth. A 50 μm membrane from the sample was cut and mounted on top of a piezo actuator. The piezo actuation applies tensile strain to the SiC membrane perpendicular to the c-axis. The device was cooled to 20 K. The neutral divacancy's ZPLs were excited optically at 976 nm and monitored. Microwave excitation for electron spin resonance was supplied by waveguide antennae on the chip. A variation of the ODMR signal was observed in the presence of strain. The strain sensitivity is inferred to be $10^{-7}/\sqrt{HzN}$, where N is the number of spins. Also, the electric field response exhibited significant spin-dependent PL, 2-7 times stronger than with NV centres in diamond. Electric field pulses were applied across the SiC membrane, using patterned electrodes that transmit light, and the ODMR signal was monitored. If these techniques were extended to single defects, these properties could be applicable to the nanometre scale, and they could be applied for sensing intracellular electric fields, integrating nanoscale sensing into SiC bioelectronics[81], or coupling spins to SiC nano-mechanical resonators[9]. In another work, the spin resonances of the V_{Si} defect at 128 MHz and 28 MHz associated with the V2 and V3 ZPLs in 6H SiC were used to monitor magnetic field and temperature variation [82].

An important milestone is to achieve the integration of these defects in nanoparticles. The first demonstration of optical spin control of silicon vacancy in 600-nm-size material was achieved in [83]. High-quality, defect-free 6H-SiC bulk material using the well-established sublimation technique in argon atmosphere at a high temperature (2500÷2600 °C) was grown from a specially prepared source pure SiC powder synthesised from silicon and carbon mixture of spectral purity. Macroscopic crystal fragments in the mm range were synthesised and then placed in the central irradiation tube of a TRIGA Mark II nuclear reactor, where vacancies were formed by neutron irradiation followed by annealing, achieving an initial concentration of V_{Si} defects of the order of 10^{15} cm^{-3}. High-energy milling process was used to achieve size from 60 to 600 nm. PL from V_{Si} ($V_{1,2,3}$) was observed in 60 nm and 600 nm crystals at room and cryogenic temperature for comparison to identify the ZPLs. No single-photon emission was observed while V_3 and V_2 from V_{Si} spin resonances were observed at 27 MHz and 127 MHz with positive and negative ODMR contrast, respectively.

8. Summary and outlook

We have summarised SiC paramagnetic defects with quantum properties observed following single-defect creation and isolation. These defects are present in various polytypes, and their variety in different crystal sites increases their space of applications. We also reviewed the state of the art of quantum effects observed in SiC nanostructures. SiC as a host for quantum systems is just at its inception, though the beginning indicates it could be one of the most prominent and rich material to investigate or to employ in the future. A large variety of deep defects were investigated from the point of view of paramagnetic and optical properties in the past, and now other quantum properties have been revealed, providing additional information not available at the ensemble level and novel insights relative to previously known defects. The challenge of engineering a desired defect in a specific location in the material is still an open problem, though it has been successfully demonstrated so far with electron, neutron and ion irradiation. SiC single defects in bulk and in the red part of the spectrum is one of the best SPS operating at room temperature, surpassing in terms of brightness other materials. The properties of these defects are also important for their spin coherent control and their use as spin qubits. The spin coherence time in ensemble and at the single level of intrinsic defects in SiC is very promising and comparable to NV in diamond. Isolation of intrinsic single spin has been achieved. However, for the most interesting spectral region in the infrared, it appears that the emission is not very bright and needs further enhancement via integration of the defects in photonics crystal cavities or microresonator. The spin coherence control still requires cryogenic temperature for the IR emitters. Since both Si and C have spin-free isotopes ($^{28}Si^{12}C$), it is expected that the measured coherence times could be enhanced through the sublimation crystal growth to reduce the abundance of ^{29}Si and ^{13}C isotopes having nonzero nuclear spins. While the challenge of the nano-fabrication of this material seems to indicate its feasibility and viability, for this to be successful, a major challenge needs to be addressed, specifically, the creation of the defects in a specific location close to the material surface within the photonic devices. Another option could be to integrate SiC QDs in hybrid photonics systems. This will require the successful incorporation of the desired defects with high yield in QDs and NPs. Additionally, many other potential defects in the material should be explored, particularly extrinsic defects that could facilitate their on-demand integration in devices. Alternatively for intrinsic defects originated from damage, more precise damage techniques could aid to the accurate location of the defects in

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the lattice. Nanostructures are ready to be integrated with deep optical and paramagnetic defects, though better design of cavities and choice of higher quality material would allow to take full advantage of functionalities related to single-photon emission and spin sensing to further advance their current applications. If all these challenges will be overcome in the next years, we envision the construction of SiC-defect-based LEDs and photonic crystal structures with in-built active quantum systems, for next-generation quantum technology devices.

Author details

Stefania Castelletto[1]*, Lorenzo Rosa[2,3] and Brett C. Johnson[4]

*Address all correspondence to: stefania.castelletto@rmit.edu.au

1 School of Aerospace, Mechanical and Manufacturing Engineering RMIT University, Melbourne, Australia

2 Swinburne University of Technology, Centre for Micro-Photonics (H74), Hawthorn, Australia

3 University of Parma, Department of Information Engineering, Parma, Italy

4 School of Physics, The University of Melbourne, Parkville, Australia

References

[1] C. A. Zorman, A. J. Fleischman, A. S. Dewa, M. Mehregany, C. Jacob, S. Nishino, and P. Pirouz, "Epitaxial growth of 3C-SiC films on 4 in. diam (100) silicon wafers by atmospheric pressure chemical vapor deposition," J. Appl. Phys. **78**, 5136–5138 (1995).

[2] R. Madar, "Materials science: Silicon carbide in contention," Nature **430**, 974–975 (2004).

[3] A. Dzurak, "Quantum computing: Diamond and silicon converge," Nature **479**, 47–48 (2011).

[4] D. DiVincenzo, "Quantum bits: Better than excellent," Nat. Mater. **9**, 468–469 (2010).

[5] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Coherent manipulation of coupled electron spins in semiconductor quantum dots," Science **309**, 2180–2184 (2005).

[6] M. Hofheinz, H. Wang, M. Ansmann, R. C. Bialczak, E. Lucero, M. Neeley, A. D. O'Connell, D. Sank, J. Wenner, J. M. Martinis, and A. N. Cleland, "Synthesizing arbitrary quantum states in a superconducting resonator," Nature **459**, 546–549 (2009).

[7] J. J. Pla, K. Y. Tan, J. P. Dehollain, W. H. Lim, J. J. L. Morton, D. N. Jamieson, A. S. Dzurak, and A. Morello, "A single-atom electron spin qubit in silicon," Nature **489**, 541–545 (2012).

[8] G. Davies and M. F. Hamer, "Optical studies of the 1.945 ev vibronic band in diamond," Proc. R. Soc. Lond., Ser. A **348**, 285–298 (1976).

[9] Y. T. Yang, K. L. Ekinci, X. M. H. Huang, L. M. Schiavone, M. L. Roukes, C. A. Zorman, and M. Mehregany, "Monocrystalline silicon carbide nanoelectromechanical systems," Appl. Phys. Lett. **78**, 162–164 (2001).

[10] C. A. Zorman and R. J. Parro, "Micro- and nanomechanical structures for silicon carbide mems and nems," Physica Status Solidi B **245**, 1404–1424 (2008).

[11] B.-S. Song, S. Yamada, T. Asano, and S. Noda, "Demonstration of two-dimensional photonic crystals based on silicon carbide," Opt. Express **19**, 11084–11089 (2011).

[12] S. Yamada, B.-S. Song, T. Asano, and S. Noda, "Silicon carbide-based photonic crystal nanocavities for ultra-broadband operation from infrared to visible wavelengths," Appl. Phys. Lett. **99**, 201102 (2011).

[13] S. Castelletto, B. C. Johnson, and A. Boretti, "Quantum effects in silicon carbide hold promise for novel integrated devices and sensors," Adv. Opt. Mater. **1**, 609–625 (2013).

[14] S. Castelletto, B. Johnson, V. Ivády, N. Stavrias, T. Umeda, A. Gali, and T. Ohshima, "A silicon carbide room-temperature single-photon source," Nat. Mater. **13**, 151–156 (2014).

[15] D. J. Christle, A. L. Falk, P. Andrich, P. V. Klimov, J. U. Hassan, N. T. Son, E. Janzén, T. Ohshima, and D. D. Awschalom, "Isolated electron spins in silicon carbide with millisecond coherence times," Nat. Mater. **14**, 160–163 (2015).

[16] M. Widmann, S.-Y. Lee, T. Rendler, N. T. Son, H. Fedder, S. Paik, L.-P. Yang, N. Zhao, S. Yang, I. Booker, A. Denisenko, M. Jamali, S. A. Momenzadeh, I. Gerhardt, T. Ohshima, A. Gali, E. Janzén, and J. Wrachtrup, "Coherent control of single spins in silicon carbide at room temperature," Nat. Mater. **14**, 164–168 (2015).

[17] F. Fuchs, B. Stender, M. Trupke, J. Pflaum, V. Dyakonov, and G. V. Astakhov, "Engineering near infrared single photon emitters in ultrapure silicon carbide," Nat. Comm. (2015). doi:10.1038/ncommos8578 .

[18] S. Castelletto, B. C. Johnson, C. Zachreson, D. Beke, I. Balogh, T. Ohshima, I. Aharonovich, and A. Gali, "Room temperature quantum emission from cubic silicon carbide nanoparticles," ACS Nano **8**, 7938–7947 (2014).

[19] S. Castelletto, Z. Bodrog, A. P. Magyar, A. Gentle, A. Gali, and I. Aharonovich, "Quantum-confined single photon emission at room temperature from SiC tetrapods," Nanoscale **6**, 10027–10032 (2014).

[20] J. Cardenas, M. Zhang, C. T. Phare, S. Y. Shah, C. B. Poitras, B. Guha, and M. Lipson, "High Q SiC microresonators," Opt. Express **21**, 16882–16887 (2013).

[21] X. Lu, J. Y. Lee, P. X.-L. Feng, and Q. Lin, "Silicon carbide microdisk resonator," Opt. Lett. **38**, 1304–1306 (2013).

http://dx.doi.org/10.5772/61166

[22] M. Radulaski, T. M. Babinec, S. Buckley, A. Rundquist, J. Provine, K. Alassaad, G. Ferro, and J. Vučković, "Photonic crystal cavities in cubic (3c) polytype silicon carbide films," Opt. Express **21**, 32623–32629 (2013).

[23] G. Calusine, A. Politi, and D. D. Awschalom, "Silicon carbide photonic crystal cavities with integrated color centers," Appl. Phys. Lett. **105**, 011123 (2014).

[24] A. P. Magyar, D. Bracher, J. C. Lee, I. Aharonovich, and E. L. Hu, "High quality sic microdisk resonators fabricated from monolithic epilayer wafers," Appl. Phys. Lett. **104**, 051109 (2014).

[25] S. Yamada, B.-S. Song, S. Jeon, J. Upham, Y. Tanaka, T. Asano, and S. Noda, "Second-harmonic generation in a silicon-carbide-based photonic crystal nanocavity," Opt. Lett. **39**, 1768–1771 (2014).

[26] X. Lu, J. Y. Lee, P. X.-L. Feng, and Q. Lin, "High q silicon carbide microdisk resonator," Appl. Phys. Lett. **104**, 181103 (2014).

[27] X. Lu, J. Y. Lee, S. Rogers, and Q. Lin, "Optical kerr nonlinearity in a high-q silicon carbide microresonator," Opt. Express **22**, 30826–30832 (2014).

[28] J. Boruah, Y. Kalra, and R. Sinha, "Demonstration of temperature resilient properties of 2D silicon carbide photonic crystal structures and cavity modes," Optik - Int. J. Light Electron Opt. **125**, 1663–1666 (2014).

[29] J. Y. Lee, X. Lu, and Q. Lin, "High-Q silicon carbide photonic-crystal cavities," Appl. Phys. Lett. **106**, 041106 (2015).

[30] M. Radulaski, T. M. Babinec, K. Müller, K. G. Lagoudakis, J. L. Zhang, S. Buckley, Y. A. Kelaita, K. Alassaad, G. Ferro, and J. Vučković, "Visible photoluminescence from cubic (3c) silicon carbide microdisks coupled to high quality whispering gallery modes," ACS Photonics **2**, 14–19 (2015).

[31] E. Sörman, N. T. Son, W. M. Chen, O. Kordina, C. Hallin, and E. Janzén, "Silicon vacancy related defect in 4h and 6h sic," Phys. Rev. B **61**, 2613–2620 (2000).

[32] N. Mizuochi, S. Yamasaki, H. Takizawa, N. Morishita, T. Ohshima, H. Itoh, and J. Isoya, "Continuous-wave and pulsed epr study of the negatively charged silicon vacancy with $s = \frac{3}{2}$ and C_{3v} symmetry in n-type $4h - \mathrm{SiC}$," Phys. Rev. B **66**, 235202 (2002).

[33] J. Steeds, G. Evans, L. Danks, S. Furkert, W. Voegeli, M. Ismail, and F. Carosella, "Transmission electron microscope radiation damage of 4h and 6h sic studied by photoluminescence spectroscopy," Diam. Relat. Mater. **11**, 1923–1945 (2002).

[34] N. T. Son, P. Carlsson, J. ul Hassan, E. Janzén, T. Umeda, J. Isoya, A. Gali, M. Bockstedte, N. Morishita, T. Ohshima, and H. Itoh, "Divacancy in 4H-SiC," Phys. Rev. Lett. **96**, 055501 (2006).

[35] T. Umeda, N. T. Son, J. Isoya, E. Janzén, T. Ohshima, N. Morishita, H. Itoh, A. Gali, and M. Bockstedte, "Identification of the carbon antisite-vacancy pair in 4*h*-sic," Phys. Rev. Lett. **96**, 145501 (2006).

[36] J. W. Steeds, "Photoluminescence study of the carbon antisite-vacancy pair in 4h- and 6h-sic," Phys. Rev. B **80**, 245202 (2009).

[37] H. Kraus, V. Soltamov, D. Riedel, S. Väth, F. Fuchs, A. Sperlich, P. Baranov, V. Dyakonov, and G. Astakhov, "Room-temperature quantum microwave emitters based on spin defects in silicon carbide," Nat. Phys. **10**, 157–162 (2014).

[38] W. F. Koehl, B. B. Buckley, F. J. Heremans, G. Calusine, and D. D. Awschalow, "Room temperature coherent control of defect spin qubits in silicon carbide," Nature **479**, 84 (2011).

[39] A. L. Falk, B. B. Buckley, G. Calusine, W. F. Koehl, V. V. Dobrovitski, A. Politi, C. A. Zorman, P. X.-L. Feng, and D. D. Awschalom, "Polytype control of spin qubits in silicon carbide," Nat. Commun. **4**, 1819 (2013).

[40] B. Magnusson and E. Janzén, "Optical characterization of deep level defects in SiC," Mater. Sci. Forum **340342**, 341–346 (2005).

[41] N. T. Son, P. N. Hai, M. Wagner, W. M. Chen, A. Ellison, C. Hallin, B. Monemar, and E. Janzén, "Optically detected magnetic resonance studies of intrinsic defects in 6H-SiC," Semicond. Sci. Technol. **14**, 1141 (1999).

[42] T. Basché, W. E. Moerner, M. Orrit, and H. Talon, "Photon antibunching in the fluorescence of a single dye molecule trapped in a solid," Phys. Rev. Lett. **69**, 1516–1519 (1992).

[43] P. Michler, A. Imamoglu, M. D. Mason, P. J. Carson, G. F. Strouse, and S. K. Buratto, "Quantum correlation among photons from a single quantum dot at room temperature," Nature **406**, 968–970 (2000).

[44] C. Santori, D. Fattal, J. Vuckovic, G. S. Solomon, and Y. Yamamoto, "Indistinguishable photons from a single-photon device," Nature **419**, 594–597 (2002).

[45] C. Kurtsiefer, S. Mayer, P. Zarda, and H. Weinfurter, "Stable solid-state source of single photons," Phys. Rev. Lett. **85**, 290–293 (2000).

[46] A. Tribu, G. Sallen, T. Aichele, R. Andre, J.-P. Poizat, C. Bougerol, S. Tatarenko, and K. Kheng, "A high-temperature single-photon source from nanowire quantum dots," Nano Lett. **8**, 4326–4329 (2008).

[47] R. Kolesov, K. Xia, R. Reuter, R. Stöhr, A. Zappe, J. Meijer, P. Hemmer, and J. Wrachtrup, "Optical detection of a single rare-earth ion in a crystal," Nat. Commun. **3**, 1029 (2012).

[48] C. Santori, F. D., and Y. Yamamoto, *Single Photon Device and Applications* (Wiley, 2010).

[49] J. Fan, H. Li, J. Jiang, L. K. Y. So, Y. W. Lam, and P. K. Chu, "3c-sic nanocrystals as fluorescent biological labels," Small **4**, 1058–1062 (2008).

[50] B. Mognetti, A. Barberis, S. Marino, F. Di Carlo, V. Lysenko, O. Marty, and A. Géloën, "Preferential killing of cancer cells using silicon carbide quantum dots," J. Nanosci. Nanotechnol. **10**, 7971–7975 (2010).

[51] T. Serdiuk, V. Lysenko, B. Mognetti, V. Skryshevsky, and A. Géloën, "Impact of cell division on intracellular uptake and nuclear targeting with fluorescent sic-based nanoparticles," J. Biophotonics **6**, 291–297 (2013).

[52] D. Dai, X. Guo, and J. Fan, "Identification of luminescent surface defect in SiC quantum dots," Appl. Phys. Lett. **106**, 053115 (2015).

[53] X. L. Wu, J. Y. Fan, T. Qiu, X. Yang, G. G. Siu, and P. K. Chu, "Experimental evidence for the quantum confinement effect in 3*c*-sic nanocrystallites," Phys. Rev. Lett. **94**, 026102 (2005).

[54] J. Botsoa, V. Lysenko, A. Geloen, O. Marty, J. M. Bluet, and G. Guillot, "Application of 3C-SiC quantum dots for living cell imaging," Appl. Phys. Lett. **92**, 173902 (2008).

[55] D. Beke, Z. Szekrényes, I. Balogh, M. Veres, É. Fazakas, L. K. Varga, K. Kamarás, Z. Czigány, and A. Gali, "Characterization of luminescent silicon carbide nanocrystals prepared by reactive bonding and subsequent wet chemical etching," Appl. Phys. Lett. **99**, 213108 (2011).

[56] S. Yang, B. Kiraly, W. Y. Wang, S. Shang, B. Cao, H. Zeng, Y. Zhao, W. Li, Z.-K. Liu, W. Cai, and T. J. Huang, "Fabrication and characterization of beaded sic quantum rings with anomalous red spectral shift," Adv. Mater. **24**, 5598–5603 (2012).

[57] D. Beke, Z. Szekrényes, D. Pálfi, G. Róna, I. Balogh, P. A. Maák, G. Katona, Z. Czigány, K. Kamarás, B. Rózsa, L. Buday, B. Vértessy, and A. Gali, "Silicon carbide quantum dots for bioimaging," J. Mater. Res. **FirstView**, 1 (2012).

[58] A. Gruber, A. Dräbenstedt, C. Tietz, L. Fleury, J. Wrachtrup, and C. von Borczyskowski, "Scanning confocal optical microscopy and magnetic resonance on single defect centers," Science **276**, 2012 (1997).

[59] V. A. Soltamov, A. A. Soltamova, P. G. Baranov, and I. I. Proskuryakov, "Room temperature coherent spin alignment of silicon vacancies in 4*h*- and 6*h*-sic," Phys. Rev. Lett. **108**, 226402 (2012).

[60] D. Riedel, F. Fuchs, H. Kraus, S. Väth, A. Sperlich, V. Dyakonov, A. A. Soltamova, P. G. Baranov, V. A. Ilyin, and G. V. Astakhov, "Resonant addressing and manipulation of silicon vacancy qubits in silicon carbide," Phys. Rev. Lett. **109**, 226402 (2012).

[61] P. L. Stanwix, L. M. Pham, J. R. Maze, D. Le Sage, T. K. Yeung, P. Cappellaro, P. R. Hemmer, A. Yacoby, M. D. Lukin, and R. L. Walsworth, "Coherence of nitrogen-vacancy electronic spin ensembles in diamond," Phys. Rev. B **82**, 201201 (2010).

[62] I. G. Ivanov, M. Yazdanfar, B. Lundqvist, J.-T. Chen, J. Hassan, P. Stenberg, R. Liljedahl, N. T. Son, J. W. Ager, III, O. Kordina, and E. Janzén, "High-Resolution Raman and Luminescence Spectroscopy of Isotope-Pure(SiC)-Si-28-C-12, Natural and C-13 - Enriched 4H-SIC," (TRANS TECH PUBLICATIONS LTD, 2014) pp. 471–474.

[63] L.-P. Yang, C. Burk, M. Widmann, S.-Y. Lee, J. Wrachtrup, and N. Zhao, "Electron spin decoherence in silicon carbide nuclear spin bath," Phys. Rev. B **90**, 241203 (2014).

[64] F. Zhao, M. M. Islam, and C.-F. Huang, "Photoelectrochemical etching to fabricate single-crystal sic {MEMS} for harsh environments," Mater. Lett. **65**, 409–412 (2011).

[65] M. M. Islam, C.-F. Huang, and F. Zhao, "Single-crystal sic resonators by photoelectrochemical etching," Mater. Sci. Forum **717-720**, 529–532 (2012).

[66] L. Di Cioccio, Y. Le Tiec, F. Letertre, C. Jaussaud, and M. Bruel, "Silicon carbide on insulator formation using the smart cut process," Electron. Lett. **32**, 1144–1145 (1996), .

[67] B.-S. Song, S. Noda, T. Asano, and Y. Akahane, "Ultra-high-q photonic double-heterostructure nanocavity," Nat. Mater. **4**, 207–210 (2005).

[68] K. J. Vahala, "Optical microcavities," Nature **424**, 839–846 (2003).

[69] T. J. Kippenberg and K. J. Vahala, "Cavity optomechanics: Back-action at the mesoscale," Science **321**, 1172–1176 (2008).

[70] J. L. O'Brien, A. Furusawa, and J. Vučković, "Photonic quantum technologies," Nat. Photonics **3**, 687 (2009).

[71] I. J. Wu and G. Y. Guo, "Second-harmonic generation and linear electro-optical coefficients of sic polytypes and nanotubes," Phys. Rev. B **78**, 035447 (2008).

[72] S. Singh, J. R. Potopowicz, L. G. V. Uitert, and S. H. Wemple, "Nonlinear optical properties of hexagonal silicon carbide," Appl. Phys. Lett. **19**, 53 (1971).

[73] P. M. Lundquist, W. P. Lin, G. K. Wong, M. Razeghi, and J. B. Ketterson, "Second harmonic generation in hexagonal silicon carbide," Appl. Phys. Lett. **66**, 1883 (1995).

[74] S. Niedermeier, H. Schillinger, R. Sauerbrey, B. Adolph, and F. Bechstedt, "Second-harmonic generation in silicon carbide polytypes," Appl. Phys. Lett. **75**, 618 (1999).

[75] H. Sato, M. Abe, I. Shoji, J. Suda, and T. Kondo, "Accurate measurements of second-order nonlinear optical coefficients of 6h and 4h silicon carbide," J. Opt. Soc. Am. B **26**, 1892–1896 (2009).

[76] S. Wang, M. Zhan, G. Wang, H. Xuan, W. Zhang, C. Liu, C. Xu, Y. Liu, Z. Wei, and X. Chen, "4h-sic: a new nonlinear material for midinfrared lasers," Laser Photonics Rev. **7**, 831–838 (2013).

[77] R. Hristu, S. Stanciu, D. Tranca, A. Matei, and G. Stanciu, "Nonlinear optical imaging of defects in cubic silicon carbide epilayers," Sci. Rep. **4** (2014), 10.1038/srep05258.

http://dx.doi.org/10.5772/61166

[78] F. Fuchs, V. A. Soltamov, S. Väth, P. G. Baranov, E. N. Mokhov, G. V. Astakhov, and V. Dyakonov, "Silicon carbide light-emitting diode as a prospective room temperature source for single photons," Sci. Rep. **3** (2013).

[79] P. Klimov, A. Falk, B. Buckley, and D. D. Awschalom, "Electrically driven spin resonance in silicon carbide color centers," Phys. Rev. Lett. **112**, 087601 (2014).

[80] A. L. Falk, P. V. Klimov, B. B. Buckley, V. Ivády, I. A. Abrikosov, G. Calusine, W. F. Koehl, A. Gali, and D. D. Awschalom, "Electrically and mechanically tunable electron spins in silicon carbide color centers," Phys. Rev. Lett. **112**, 187601 (2014).

[81] S. E. Saddow, in *Silicon Carbide Biotechnology*, edited by S. E. Saddow (Elsevier, Oxford, 2012).

[82] H. Kraus, V. Soltamov, F. Fuchs, D. Simin, A. Sperlich, P. Baranov, G. Astakhov, and V. Dyakonov, "Magnetic field and temperature sensing with atomic-scale spin defects in silicon carbide," Sci. Rep. **4** (2014).

[83] A. Muzha, F. Fuchs, N. V. Tarakina, D. Simin, M. Trupke, V. A. Soltamov, E. N. Mokhov, P. G. Baranov, V. Dyakonov, A. Krueger, and G. V. Astakhov, "Room-temperature near-infrared silicon carbide nanocrystalline emitters based on optically aligned spin defects," Appl. Phys. Lett. **105**, 243112 (2014).

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Since the production of the first commercially available blue LED in the late 1980s, silicon carbide technology has grown into a billion-dollar industry world-wide in the area of solid-state lighting and power electronics. With this in mind we organized this book to bring to the attention of those well versed in SiC technology some new developments in the field with a particular emphasis on particularly promising technologies such as SiC-based solar cells and optoelectronics. We have balanced this with the more traditional subjects such as power electronics and some new developments in the improvement of the MOS system for SiC MOSFETS. Given the importance of advanced microsystems and sensors based on SiC, we also included a review on 3C-SiC for both microsystem and electronic applications.

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